A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues

Haksun Lee, Vanessa Smet, and Rao Tummala, *Fellow, IEEE*

***Abstract*—Power module packaging technologies have been experiencing extensive changes as the novel SiC power devices with superior performance become commercially available. This paper presents an overview of power module packaging technologies in this transition, with an emphasis on the challenges that current standard packaging face, requirements that future power module packaging needs to fulfill, and recent advances on packaging technologies. The standard power module structure, which is a widely used current practice to package SiC devices, is reviewed, and the reasons why novel packaging technologies should be developed are described in the following section. The packaging challenges associated with high-speed switching, thermal management, high-temperature operation, and high voltage isolation are explained in detail. Recent advances on technologies, which tries to address the limitations of standard packaging, both in packaging elements and package structure are summarized. The trend towards novel soft switching power converters gave rise to problems regarding package designs of unconventional module configuration. Potential applications areas like aerospace applications introduce low-temperature challenges to SiC packaging. Key issues in this emerging areas are highlighted.**

***Index Terms*—power module, packaging, SiC, silicon carbide**

I. Introduction

MODERN power electronics is facing a substantial demand on improving efficiency while reducing the size and cost of the systems for a broad range of areas, including electric vehicles, renewable energies, industrial motors and generators, and distribution grid applications. The energy consumption of industrial plants in the United States accounted for 955 billion kWh in 2014, which is over a quarter of total electrical energy usage, and is expected to grow by 26% to 1270 billion kWh by 2040 [1]. To keep pace with this projection of energy consumption, it is essential to reduce energy consumption of industrial motors and generators that drive equipment such as fans, pumps, compressors, and conveyor systems by improving the efficiency of power electronics that control the motors and generators [1]. Energy saving needs can also be found in other applications. In electric vehicle application, the efficiency directly affects the performance of a vehicle such as the driving distance. Thus, improving the efficiency, while reducing volume and weight of the powertrain system in electric vehicles would have potential to save a significant amount of energy [2].The amount of electricity provided by renewable resources such as photovoltaic (PV) panels and wind turbines add up to 300 billion kWh in 2017 in the United States [3]. Significant energy gains are expected as the installation of wind turbines and solar panels rapidly grow, and as the efficiency of power electronics in those machines improve [2].

Silicon carbide (SiC), a wide-bandgap semiconductor material, has shown the capability to satisfy higher-performance demands of evolving power electronics in the areas previously mentioned. In the past, silicon (Si) has been the most widely used semiconductor material for a power switching device. However, as Si-based power devices have been approaching to its physical limit, further improving their performance is becoming a great challenge [4], [5]. For example, the blocking voltage and operating temperature are limited to 6.5kV and 175°C, respectively, and the switching speed is relatively slow [5]. Devices made of SiC, on the other hand, have evolved from immature laboratory prototypes to a viable commercial product over the last few decades, and are considered an alternative to Si-based power devices due to its compelling advantages, such as high-breakdown voltage, high-operating electric field, high-operating temperature, high-switching frequency and low losses. In addition to these performance improvements, power electronics based on SiC devices are expected to bring volume reduction of the system by minimizing cooling requirements and passive component requirements, contributing to lowering the overall system cost [1]. These benefits of SiC align well with the requirements and directions of power electronics in future energy conversion applications. Despite their higher cost compared to their Si-based counterparts, SiC devices are going to prevail over Si-based devices, because the potential system advantages they can bring are significant enough to offset the increased device cost [4], [6].

A market survey of SiC device and module makers shows that the advantages of SiC devices are evident in recent commercial products [7]. For instance, per area specific on-resistance of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) is 4 times smaller than that of Si insulated-gate bipolar transistors (IGBTs), and has been showing a decreasing trend of -30% in every 3 years. Compared to Si-counterparts, a 10 to 20 times smaller switching energy is demonstrated, and 20 times higher maximum switching frequency is estimated in the SiC devices [7]. Owing to these merits, significant markets are expected for SiC power devices. The total SiC power device market is expected to

The authors are with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332 USA e-mail: hlee435@gatech.edu, vanessa.smet@prc.gatech.edu, rao.tummala@ece.gatech.edu

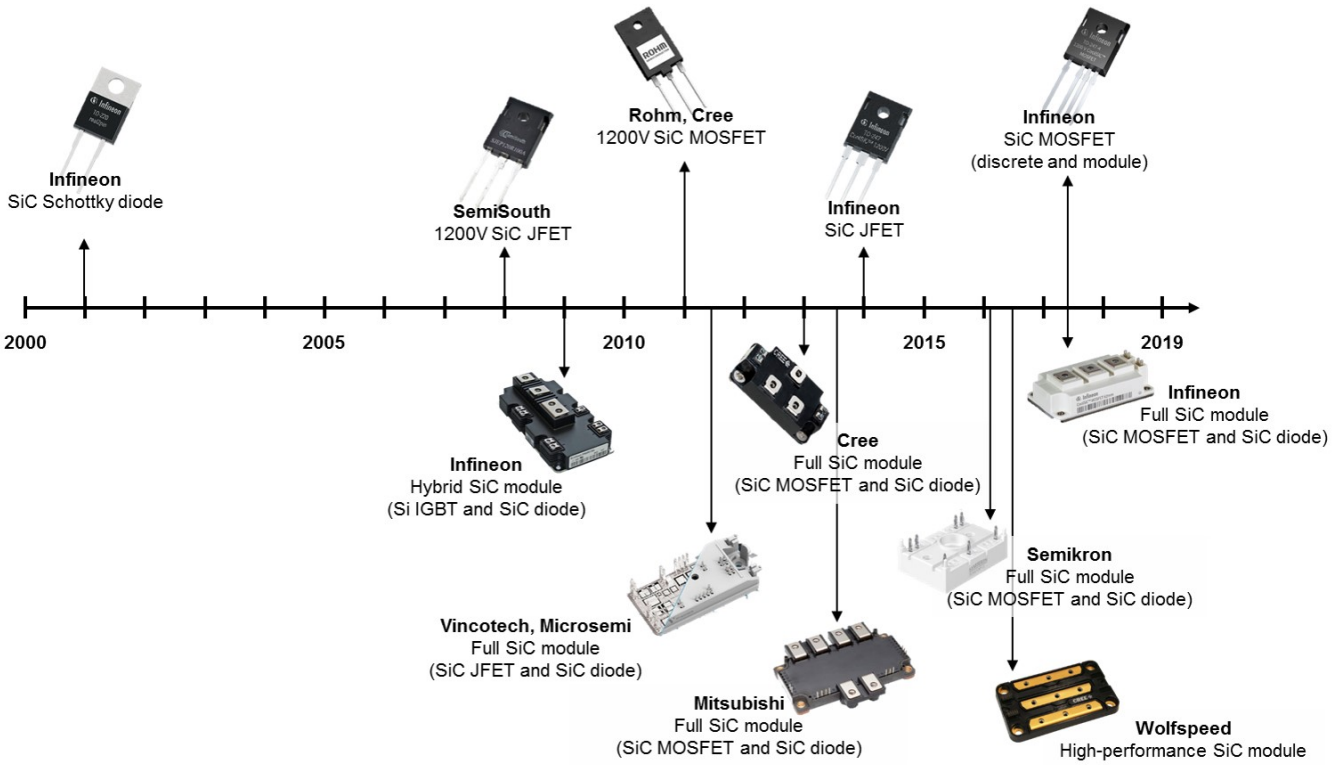

Fig. 1. Development of SiC devices and their packages

grow up to $1 billion by 2022 at a compound annual growth rate (CAGR) of 28%, with the greatest revenue-generating applications expected to be in hybrid and electric vehicles, PV inverters, and industrial motor drive [1], [8], [9].

However, challenges and issues still exist from the device perspective [10]. As the active area of a SiC chip reduces, the short-circuit endurance time tends to decrease. This indicates that there is a trade-off between robustness/reliability and die size [7]. In addition, the field reliability of SiC devices has not been demonstrated in various applications areas. This is one of the main causes of slow penetration of SiC devices into the power electronics market [5], [10].

On the other hand, producing high-quality, low-defect, and larger SiC wafers has been a technical hurdle for SiC device manufacturers. Because of this manufacturing difficulties, the average selling price per Ampere of SiC MOSFETs are 4 to 5 times higher than Si counterparts [7]. Although the SiC material defects have been overcome to a great extent, manufacturing processes need to be improved to make the cost of SiC devices more justifiable [5], [11]. Recently, most major SiC device makers have started production using 6 inch wafers. X-fab, a silicon foundry company, has upgraded its manufacturing resources to accommodate 6-inch SiC wafers, providing services to fab-less companies like Monolith. All these efforts will result in overall cost reduction of SiC devices.

Fig. 1 presents the milestones of development of SiC power devices and their packages. The first SiC device introduced to the market was Schottky diodes manufactured by Infineon in 2001. Since then, other companies like Cree and Rohm continued to release SiC diodes with a variety of ratings. In 2008, SemiSouth produced the first SiC junction gate field-effect transistors (JFETs), and around that timeframe, companies started to integrate SiC Schottky diode bare dies into power modules based on Si IGBTs, producing hybrid SiC power modules. From 2010 to 2011, Rohm and Cree introduced the first SiC MOSFETs with a 1200V rating in discrete packages. As SiC power transistors became commercially available, companies such as Vincotech and Microsemi started producing full SiC modules using SiC JFETs and SiC diodes in 2011. In 2013, Cree introduced full SiC module using SiC MOSFETs and SiC diodes. Since then, other device vendors, including Mitsubishi, Semikron, Fuji, and Infineon, themselves released the full SiC modules. In most of the cases, the SiC devices were first introduced as discrete components, and the implementation of those devices into a module package was developed after a few years following the initial release. One reason behind this is that the manufacturing process of discrete packages is by far much simpler than that of the power module package. The other reason, perhaps, is that the modules that are released have gone through extensive standard JEDEC qualification with a stringent power cycling reliability test, which needs to pass 20 million cycles without failures [12]. The discretes have flexibility in designing the system with lower cost, whereas the modules have strength in higher performance with ease of integration once the products are available.

While the SiC semiconductor technology has been rapidly advancing forward, the power module packaging technology seemed to be relying on the past convention, which is a proven standard. However it is not as up to speed on drawing the

new device's full potential. The packaging of SiC devices has been mostly based on a wire bonding approach on a ceramic substrate, which is a standard method to form interconnects for MCMs (multi-chip-modules), due to its ease-of-use and relatively lower cost [13]. However, this standard packaging method has been pointed out to be a technical barrier in moving to a higher performance system due to its package-inherent limitations. Firstly, the electrical parasitics of the package are too high so that they create unwanted losses and noises during fast switching of SiC devices. Secondly, the thermal resistance of the package is too high, whereas the thermal capacity is too low, which limits the heat dissipation performance of the package both in steady-state and transient. Thirdly, materials and components that make up the package are usually not compatible with high temperature operations ($> 200^{o}$C), deteriorating thermomechanical reliability at elevated operating temperatures. Lastly, the capability to withstand high electrical field is not sufficient for upcoming high-voltage SiC devices. The details of these challenges will further be elaborated in the following sections. In conclusion, not the device itself, but the power module packaging is one of the main limiting factors that prevents the package from fully utilizing the advantages of the SiC components. Therefore, the utmost effort should be put on understanding the features required for future SiC packaging and developing novel packaging technologies accordingly.

The purpose of this study is 1) to review the current practice of standard power modules used to package SiC devices and address their limitations, 2) to summarize the reasons why we need new packaging technologies for SiC devices, 3) to highlight some of the advances and key innovations in power module packaging technologies, and capture the recent trend, and 4) to address emerging packaging challenges and give perspective on future directions.

II. Status of SiC Multi-Chip Modules

A. Current Industry Practice of SiC Packaging

A conventional power module package consists of 7 basic elements, which are power semiconductor chips, insulating substrate, base plate, bonding material, power interconnections, encapsulant and plastic case as depicted in Fig. 2. These elements in the module are composed of different materials ranging from insulators, conductors, and semiconductors to organics and inorganics [14]. Since these different materials are strongly bonded together, it is critical to select proper materials for each element to form a robust package. In this subsection, the roles and popular selections for each of the 7 basic elements and their assembly process will be discussed.

1) Power Semiconductor: Power semiconductors are essential elements in power modules, converting power from source to load by performing electrical on/off switching. The most commonly used type of device in standard power modules are MOSFETs, IGBTs, diodes, and thyristors.

2) Insulating substrate: Insulating substrate provides electrical conduction between semiconductor components and terminals, electrical isolation from other metal parts like the base plate and the heatsink, and dissipation of heat generated from the components. DBC (direct bonded copper) substrates are used for insulating substrate in conventional power modules due to their excellent properties that not only satisfy the electrical and thermal requirements but also the mechanical reliability. Among various candidates, popular materials for the ceramic layer sandwiched between two copper layers are Al_2O_3, AlN, Si_2N_4, and BeO [14].

3) Bonding material: The main function of bonding material is to provide mechanical, thermal, and electrical linkage between the semiconductors, conductor traces, terminals, substrate, and base plate of the power module by attaching each component [14]. Due to their compatibility to the electronics assembly environment, solder alloys, such as SnPb and SnAgCu, are the most commonly used bonding materials for die and substrate attach. Important features to look for when selecting solder alloys for power modules are melting temperature in relation to service temperatures; compatibility with metallization of power chips, insulating substrate, and base plate; high mechanical strength; low elastic modulus; high creep and high fatigue resistance; high thermal conductivity; matching CTE (coefficient of thermal expansion); cost; and environmental impact.

4) Base plate: The primary role of the base plate is a mechanical support for the insulating substrate. It also absorbs heat from the insulating substrate and transmits it to the cooling system [5]. High thermal conductivity and low-CTE (matched with insulating substrate) are important properties required for base plates. Widely used base plate materials are Cu, AlSiC, CuMoCu, CuW.

5) Wire bond: The main role of wire bond is to make electrical linkages between the power semiconductors, conductor traces, and input/output terminals of the module. The most common material used for devices' top-side connection is aluminum wires. In case of power modules with higher power ratings, heavy aluminum wire bonding or ribbon bonding is used to connect the top surface of power devices and metallization of ceramic substrate for lower resistance and enhanced thermal capability.

6) Encapsulant: The primary purpose of encapsulant is to protect semiconductor devices and wire-assembled components from hostile environmental conditions such as moisture, chemicals, and gases. In addition, the encapsulant not only provides electrical insulation between wires and components against increased voltage levels, but also serves as a heat-spreading medium. Materials considered for usage as encapsulant in power module are silicone gel, silicone, polyparaxylylene, acrylic, polyurethane, and epoxy.

7) Plastic case: The plastic case (including the cover) protects the module from mechanical shock and environmental effects. Even though the components, such as power dies and wires, are embedded in an encapsulant material, they can still be broken or damaged by mishandling. The case also mechanically supports the terminals and provides isolation distance between the terminals. Thermoset allyls (DAP), thermoset epoxy, and thermoplastic polyester (PBT) with glass fillers are popular choices for plastic cases.

The manufacturing process for conventional power module starts with soldering power dies on prepared DBC substrate

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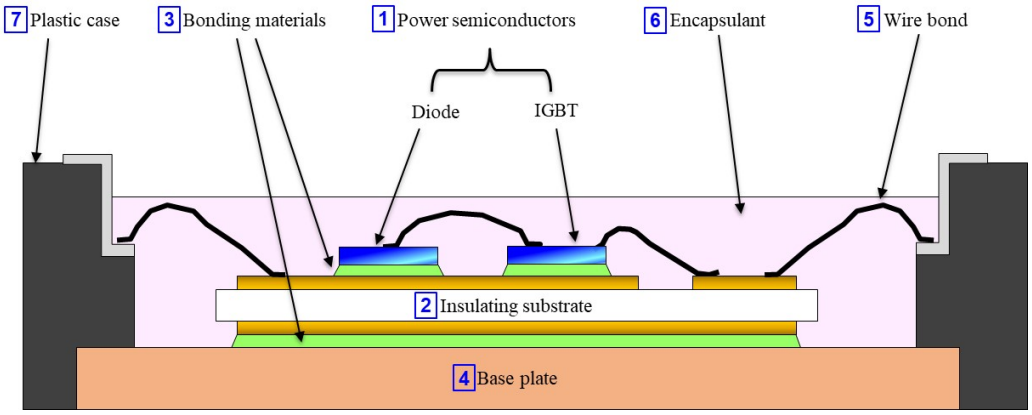

Fig. 2. Cross-sectional diagram of a standard power module structure

using a reflow oven. Multiple of these DBC substrates with the dies attached are then soldered onto a base plate also using the reflow process. On the same base plate, the plastic case where the terminals are framed is attached with either gluing or screwing. Then the connections among the top side of power dies, metallization of DBC, and terminals are made through wire bonding using aluminum wires, as discussed previously. Lastly, the encapsulant material is deposited on top of the components with a dispenser, and the material is cured at an elevated temperature.

The described structure, materials, and series of processes are considered a standard for power module packaging technology, and are still widely used in current practice [15]. Although there has been a continuous demand for novel packaging approaches, which will be discussed in the following sections, the technical changes or adoption have been gradual. This slow acceptance of new technologies can be explained by the following reasons. Firstly, there are concerns on reliability and repeatability associated with the manufacturing of the new packaging approaches [5], which take time to be resolved. Consequently, module manufacturers chose to remain with the proven and well-understood conventional power module packaging technology considering the timely market availability [15]. The second reason is the cost-effectiveness of conventional power modules [13], [15]. Since the manufacturing infrastructure, such as materials and equipment, for conventional power modules are compatible with other electronics packaging environment, it does not require additional cost related to developing new materials and equipment.

Despite these reasons to stick with standard packaging method, it is showing limitations, and faces fundamental challenges as the semiconductor trend is shifting from Si-based devices towards SiC-based devices. The following subsections will discuss why new packaging technologies are necessary for this new device trend, and summarize some of the key directions that future power module packaging need to take into account.

B. Challenges on High-Speed Switching

One of the most important electrical benefits for using SiC devices is the capability to operate at high switching frequencies. The motivation behind pushing towards higher frequencies in power converters is to minimize the overall system size and increase the power density by significant passive size reduction that comes with higher switching frequencies [16], [17]. However, the switching frequency of Si-based devices in high-power electronics is usually limited to few kHz due to losses associated with high-switching frequency. An example in Fig. 3 shows the decrease in efficiency of power converter using Si-IGBTs as the frequency increases, already dropping to 73% at 20kHz [11]. On the other hand, the efficiency is maintained to the much higher value of 92% in the case of SiC-MOSFETs at the same frequency [11]. From this example, it is evident that Si-based devices show limitations in high-frequency operation, while SiC components are capable of handling high energy levels while operating at higher frequencies. More detailed explanation on device mechanisms that enable fast switching of SiC semiconductors can be found in reference [18]. Although SiC devices are superior in switching performances to Si-counterparts, special consideration needs to be taken into account to fully benefit from their fast switching advantages. The fast switching transients lead to issues with device and package-internal electromagnetic parasitics [19], which are becoming fundamental barriers to high performance switching of SiC power modules.

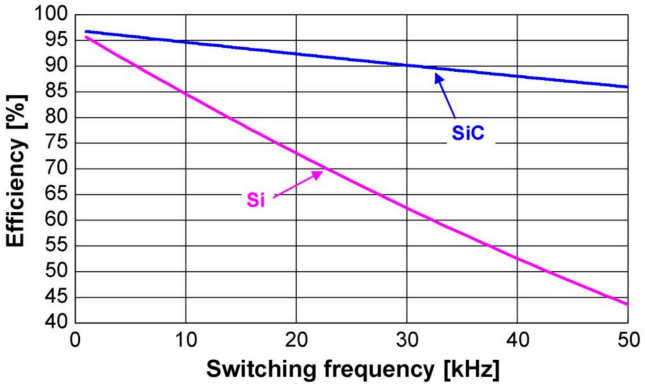

Fig. 3. Efficiency of Si and SiC converters at full power rating and different switching frequencies [20].

A circuit schematic of half-bridge power module, which

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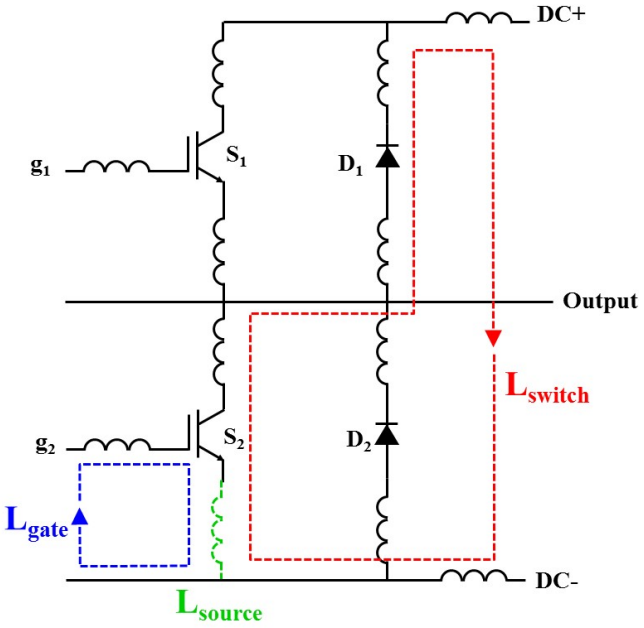

Fig. 4. Circuit schematic of a half-bridge module with three main parasitic inductances indicated as L_{switch},L_{gate}, and L_{source}.

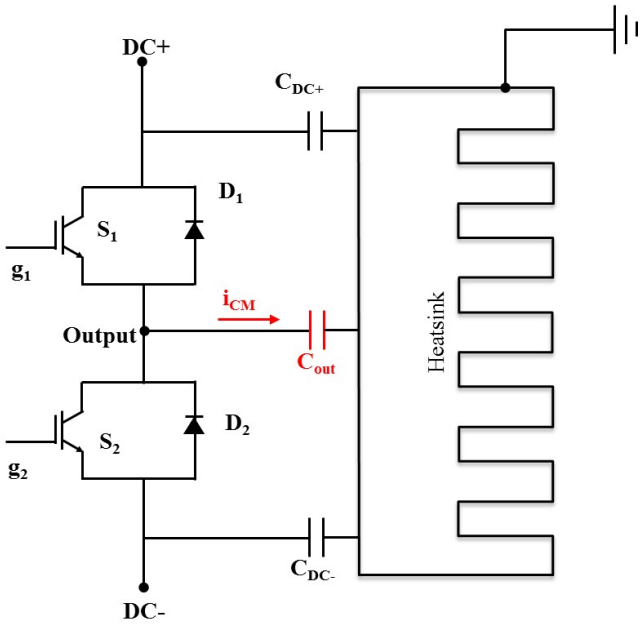

Fig. 5. Circuit schematic of half-bridge module with parasitic capacitance between the package and the heatsink.

consists of a switch and diode pair on high-side and low-side, is presented in Fig. 4, with one set of the most critical parasitic inductances, main switch loop stray inductance (L_{switch}), gate loop inductance (L_{gate}), and common source inductance (L_{source}), indicated in the figure. The main switch loop stray inductance both exist in external power circuitry and the internal package interconnections [18], however, in this literature, only the parasitic stray inductance coming from the internal package interconnections is considered. The impact of external stray inductance on switching performance can be nullified by decoupling capacitors [21], and the integration strategies of these components will be discussed in later sections.

The main switch loop stray inductance(L_{switch}) is formed by the equivalent series inductance between the DC+ bus, freewheeling diode, MOSFET (or IGBT), and DC- bus terminal. It is responsible for voltage overshoot that causes severe stress on devices during turn-off due to current fall [19], switching losses due to slower di/dt caused by negative feedback to disturb charging and discharging current into gate-source [22], increased oscillation in switching waveforms caused by resonance of stray inductance and output capacitance of semiconductor devices, that results in increased EMI emission [23].

The gate loop inductance (L_{gate}) is formed by gate current path, i.e, connections from the driver board to gate contact pad of the device, and the source of device back to the driver board. It reduces the maximum achievable switching frequency by causing delay on the gate-source voltage build-up. It also resonates with the gate-source capacitance of the device and cause ringing in the gate signals. Lastly, in case of paralleling the multiple power chips, if the parasitic inductances for each gate loop are different or asymmetric, the imbalance of transient current can happen during switching [19].

The common source inductance(L_{source}) comes from the coupling between the main switch loop and gate loop inductances [24]. When turning on and off the power device, the di/dt and voltage across this inductance acts as additional (typically opposite [19]) voltage source in the gate circuit, and causes decrease in the slope of di/dt, distorting gate signals and limiting the switching speed. Additionally, the common source inductance may cause false-triggering event, which could damage the device by turning it on at an erroneous timing.

The influence of these parasitic inductances becomes more severe in fast-switching SiC devices. Very high drain-current slope di/dt is generated during switching transients of SiC devices, and voltage spikes and drops in the parasitic inductances discussed above becomes notably larger than that of Si devices. These undesired effects of parasitic inductance results in increased switching energy losses and reduction in attainable maximum switching frequency.

The problems of switching transients not only come from the current slope di/dt, but also from the voltage slope dv/dt. This dv/dt results in displacement current through parasitic capacitance of the package, which is the capacitance between the die and cooling system. Fig. 5 shows a simplified diagram of the parasitic capacitances that exist between the half-bridge module and the heatsink. This undesired current can result in detrimental effects on the reliability of inverter-fed electrical machines [25]. For example, the motor bearing defects in automotive applications caused by electrical discharge machining (EDM) are primary consequence of the noise current [26].

In conventional Si-based devices, due to low dv/dt, which is around 3kV/μs, the current flowing through the parasitic capacitance was considered insignificant [18]. However, the dv/dt of SiC devices rises more than an order of magnitude

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higher than the dv/dt of Si devices up to 50kV/μs [18], [27], making the current through the package capacitance no longer negligible. Comparison studies on EMI generation of Si and SiC devices show that the conducted and radiated electromagnetic interference (EMI) has increases with the use of SiC devices because of the fast-switching speed [25]. In addition to the undesired current through the package into the cooling systems, the capacitive parasitics are also responsible for slowing down the voltage transients, producing overcurrent spikes during switching, and increasing EMI emission by forming resonant circuit with parasitic inductances [19].

Future power modules packages should consider all the complex problems and challenges arise from the parasitics and high frequency transients in SiC packages. Main package-level requirements to address those issues are as follows.

1) The main switching loop inductance needs to be minimized by novel interconnection technologies that replaces lengthy wire bonds, and by optimized layout designs that brings the power devices in close proximity.

2) The gate drive circuity is usually assembled on a substrate board separate from the power modules, due to fabrication incompatibility and safety issues. The gate loop inductance should be minimized by bringing the gate driver circuitry to the power module as close as possible. Also, the layout should be symmetric in case of parallel chips to avoid current imbalance.

3) The problems coming from common source inductance needs to be avoided by separating gate loop current from the main switch loop current. This can be done by providing additional pin such as Kelvin source connections.

4) The current flowing in the parasitic capacitance should be mitigated by reducing the capacitive coupling the output terminal and the grounded heat sink. Some of the strategies include avoiding geometrical overlaps on metal traces of AC potentials.

C. Challenges on Thermal Management

Although current power devices convert power with decent efficiency, heat generation from these devices is inevitable in operating power modules. The switching and conduction losses from power devices create highly concentrated heat flux density around the device and along the whole thermal path from chip to coolant [28]. This heat flux causes performance degradation in power devices and thermally induced reliability problems in device and package. In this period of transition from Si-based devices to SiC-based devices, power module packaging faces unprecedented thermal challenges.

SiC devices can be made in much smaller sizes than the Si devices for the same voltage and current rating, which opens the opportunity for more compact power module designs [18]. Based on the expression of thermal resistance of a die, the shrinkage in die size, e.g, chip edge length, results in a quadratic increase in the thermal resistance [29]. This means that power module packaging for SiC devices requires more emphasis on heat spreading and cooling. For example, Fig. 6 presents the calculation of needed total chip area reduction that comes with chip-to-coolant thermal resistance reduction [28]. This plot in other words indicates that as the chip area decreases, in the case of SiC devices, the required thermal resistance needs to be improved.

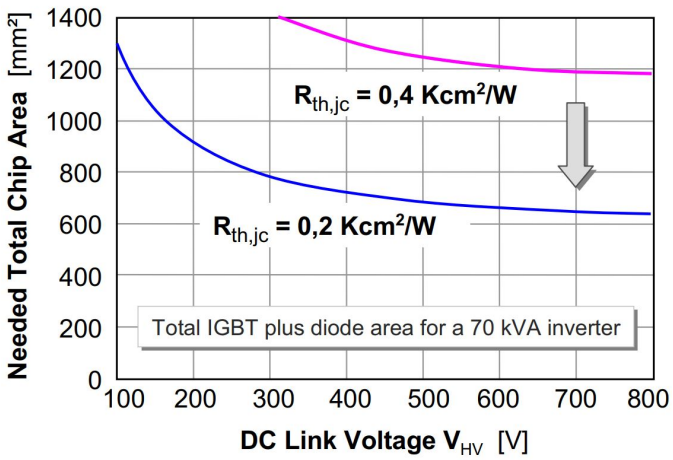

Fig. 6. Calculation of total chip area needed based on the voltage rating and thermal resistance [28].

However, even combined with the most advanced cooling strategies such as directly cooled cold plates with a pin fin structures, the standard power module packaging based on DBC and wire bonds have limited thermal resistance of unit area value typically ranging from 0.3 to 0.4 Kcm^2/W assuming a 70kVA inverter application [28]. In order to meet the future power module performance and cost targets as projected in the study, this value needs to go below 0.2 Kcm^2/W, which can only be achieved by innovative approaches such as double-sided cooling methods [28].

Small chip area also makes it difficult to place a sufficient number of wire bonds, which not only limits the current handling capability, but also limits thermal capacitance [19]. Previous thermal improvement in a standard power module package was mostly focused on steady-state thermal resistance which may not well represent the transient thermal behavior of switching power modules. Since extremely concentrated heat flux densities with fast power pulses are anticipated with SiC devices, not only the reduction of thermal resistance, but also the thermal capacity improvement is needed in order to minimize the peak temperature rise resulting from these fast pulses [30].

The thermal challenges that arise from adoption of SiC devices should be addressed in future power module packages. The following are some of the requirements that future SiC packaging should consider for thermal management.

1) Reduction or elimination of a number of package layers in the thermal path is desired for decreasing the thermal resistance.

2) Heat dissipation needs to be accomplished also from the top-side of the die to enable extremely low-level thermal resistance of a module. This may require changes in the interconnection method to a larger area joint.

3) Advanced materials at the interface of package layers would aid lowering the thermal resistance of the package. For example, materials used in the die attach, and heat spreaders

can be replaced with higher thermal conductivity joints, and carbon-based composites, respectively.

4) Advanced cooling approaches, such as jet impingement, spray, and microchannels [31], need to be incorporated to enhance the heat removal capability.

D. Challenges on High-Temperature Operation

The negative impacts of increasing temperature on both performance and reliability of semiconductor dies are well understood and documented [32]–[34]. Therefore, when the device or environment temperature is too high, active thermal management approaches such as forced air or liquid cooling must be involved, which will add undesired size, weight, cost, and complexity to the overall system. On the other hand, thanks to the advent of SiC devices, this load on cooling systems is expected to be alleviated.

High-temperature electronics that can function at ambient temperature above 150°C without external cooling could greatly benefit a variety of applications such as automotive, aerospace, and energy production industries [33]. The fact that SiC devices are capable of electronic functionality at much higher temperature than Si counterparts has partially encouraged their development [33]. Theoretical studies show that SiC devices can be operated well beyond 500°C [13], [33], indicating they are a highly suited candidate for high temperature electronics.

An example in Fig. 7 compares cooling system for Si and SiC converters, showing the decrease in the cooling apparatus as the device changes from Si to SiC, and as the device junction temperature rises from 150°C to 300°C [20]. The Si converter requires liquid cooling to dissipate the heat coming from the device losses at a given operating conditions, whereas SiC converter can only have heat sink with fans for thermal dissipation due to relatively smaller device losses. The volume of this heat sink in SiC converter can further be minimized by around 50% if the junction temperature of the device is increased from 150°C to 300°C [20]. This study shows that the cooling system size, weight, cost, and complexity can be reduced as a result of increasing the operating temperature of the devices.

High-temperature electronics is also desired in certain applications where the ambient temperature or coolant temperature require operation higher than today's limit of 150°C. In areas including fuel combustion, motor drives using engine coolant, deep-well drilling, and industrial manufacturing processes, the presence of high temperatures well beyond the limit of Si-based electronics is inherent to the operation, making it difficult for conventional Si-based power modules to survive. The SiC power modules are expected to proliferate in these applications once the technology to realize these high-temperature power modules becomes available.

From the above discussions, it is clear that high-temperature power modules using SiC will bring system-level advantages that could enable overall volume and cost reduction of the system. However, there still are challenges that impede the realization of high-temperature power modules [33], [34].

Firstly, the unavailability of mature packaging materials themselves as well as the interfaces between these materials

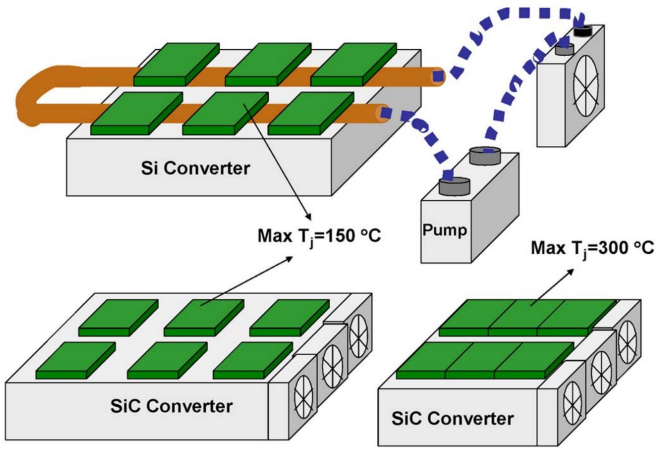

Fig. 7. Comparison of cooling systems for Si and SiC converters [20].

for above 200°C operation is one of the biggest bottlenecks. For instance, the encapsulation materials discussed in previous section are generally soft organic insulating materials designed for conventional Si power modules limited to low temperature up to about 175°C–200°C [15]. Good understanding of these soft encapsulant materials at their upper temperature limit is required. Their electrical behavior as well as long-term aging performance at high-temperature need to be characterized [35]. On the other hand, commonly used die attach materials for conventional power module package are tin-based leaded and lead-free solder alloys. Low melting point of these materials is considered to be a serious problem, preventing them from being used in high-temperature applications [36]. When exposed at high temperatures, these die attach materials tend to form intermetallic phases to a level which endangers the reliability of the interconnect.

Secondly, the large temperature range (-55°C–200°C) cycling that power module encounters increases the stress caused by the CTE mismatch between different materials in the package [33]. This mismatch between the die, die attach, and substrate will create stresses on each package layers. Even slight mechanical stress on the die may cause electrical parameters to shift to an unacceptable level, and thereby it should be minimized [34]. Main failure mechanisms appearing in conventional power module package are wire bond lift-off, cracking or delamination of solder die (or substrate) attach, and chip metallization on the top-side [37], [38]. Increasing the device junction temperature from 150°C to 200°C will exacerbate the major failure mechanisms, and reduce the lifetime under thermal cycle by a factor of 50 based on available power module fatigue/creep degradation models [19].

Thirdly, components that make up the system such as gate driver and passive devices also need to withstand the elevated ambient temperature. As mentioned in previous sections, higher-level of integration of these components into the module package can significantly reduce the distance between the components, and thereby reduce the parasitic inductance. However, the temperature compatibility of these gate drive and passive components need to be verified prior to putting them close together, to prevent hot dies from thermally influencing

the temperature sensitive components. Most of capacitors and magnetic components used in these applications show poor stability, losing their properties rapidly as the temperature is increased above 200°C [34].

In summary, these challenges need to be addressed by novel materials, bonding methods, and components for high temperature applications. The following are summaries of key requirements for high-temperature and high-reliability power module packages.

1) Identifying new materials, such as encapsulant and die attach, for higher temperature operation is necessary. Moreover, their long-term high-temperature stability need to be assessed and verified.

2) Advanced bonding methods that copes with increased stresses is required. Also, the CTE of materials in package layers should be matched as best as possible in order to minimize the stress.

3) Alternatives to gate drive and passive components that can withstand and show minimal performance degradation at temperatures above 200°C is required. This will allow higher-level of integration, and thereby enable compact and highly efficient package.

E. Challenges on High-Voltage Isolation

On top of this high temperature demands, encapsulant materials need to withstand high electrical field and, at the same time, consider their processibility in terms of viscosity, which imposed challenging requirements on the material development.

The SiC devices with high voltage ratings will allow simplification and miniaturization in design of converter topologies for distribution grid applications like solid state transformers which will be discussed in more detail in the next section. The maximum voltage rating of a single SiC die has now reached to 15kV thanks to the advances on WBG semiconductor technologies, and there are activities to scale the rating even higher to 30kV [39]. However, the standard packaging methods cannot withstand this high electric field in a compact form. The electric field strength at the SiC chip edge termination will be more than 3 times higher than Si devices, which requires high strength encapsulation material for the top-side insulation [19]. The presence of wire bondless interconnections which has conductor traces on the top-side of the die in close proximity will require careful design and modeling of field distribution within the module package to prevent dielectric breakdown [19].

Evaluation on recent high-temperature encapsulant materials show dramatic drop in dielectric strength as the temperature range increased from 20°C to 250°C, and as the thermal aging time has progressed [40]. This indicates a lot of effort is still needed to understand and characterize the long-term stability in thermal, electrical, and mechanical properties of the high-temperature and high-voltage encapsulant materials.

To summarize, as the SiC devices with high-voltage ratings are becoming available, the followings requirements should be considered for isolation of SiC power module.

1) Encapsulant materials that cope with increased insulation demand with minimal performance degradation in long-term thermal exposure is critical.

2) The emerging package designs try to bring all the power module elements into a denser package, which endangers the reliability of module under high voltage conditions. New designs should ensure sufficient separation distances between the device, traces, terminals to prevent dielectric breakdown.

III. Recent Advances and Key Innovations

Although most of the commercially available SiC devices are packaged using a standard method, there have been numerous efforts in the last decade to move away from this conventional power module and improve the packaging by addressing some of the challenges discussed in the previous sections. It is worth noted that many of these advances started even before the SiC became prominent, since the technical goals and directions well coincided with the packaging of Si-based IGBTs.

A. Advances in High-Speed Switching

To minimize the effect of parasitic inductance of main switching loop, wire bondless interconnections, innovative 2D and 3D layout designs, and integration of periphery components like bus bars with decoupling capacitors, have been suggested.

Wire bonds require certain loop height to form a reliable connection, as well as an extra space on a conductor trace of the substrate for a wire to properly land. These result in lengthy interconnections which create relatively high parasitic inductance. Many interconnection methods to replace wire bonds have been introduced. For instance, Fig. 8(a) shows a planar interconnect technology using direct deposited copper on the top-side of power dies which reduces the loop area for the module current, resulting in 50% reduction in the stray inductance [41]. Similar planar interconnection methods, such as direct lead frame bonding, double-sided DBC, flexible PCB, and direct copper plating, reported reduction in the parasitic inductance of main switching loop [44]–[48].

Innovative 2D and 3D layout designs reduce the stray inductance as well. The P-cell and N-cell based layout design shortens the physical length of commutation loop [49]. Moreover, instead of the conventional layout configuration which utilizes X-Y plane with the power dies facing upward, making some of the dies facing downward allows current to flow in X-Z plane which has much lower enclosed area of the current loop [45], [50]. 3D stacking of power dies have been proposed to even further minimize the issues related with di/dt. Placing one pair of power dies (a switch and a diode) on top of each other, and creates a vertical current path with extremely low parasitic inductance within the package [30], [51]–[53].

Improvements in the integration of the periphery components like bus bars and decoupling capacitors minimizes the effect of parasitic inductance. Laminated bus bars cancel out the magnetic field by having opposite current paths [54]. Decoupling capacitors are brought close to the module, or

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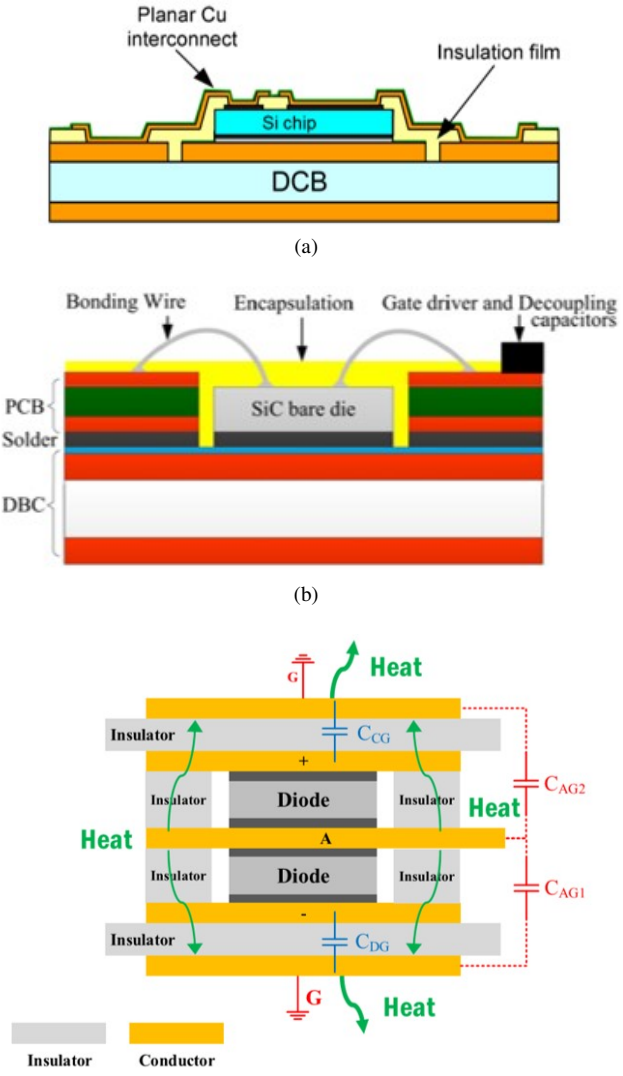

Fig. 8. Advances in packaging for high-speed switching. (a) Planar interconnects [41], (b) Gate driver integrated hybrid packaging [42], (c)3D stacked power modules [43]

even embedded within the module, to nullify the effects of parasitic inductance from the terminals [54], [55].

Shortening the interconnection length between the power device and the gate driver will reduce gate loop inductance which results in increased switching speed. The first approach is based on conventional DBC substrate where the top-side of the package is integrated with a PCB board with cavity, and wire bonds are used to connect the gate driver IC, capacitors, and power dies [42], [56]. Due to the inability of DBC substrate to incorporate low power components with fine features, power stage and drive circuitry were often divided into separate packages preventing high density integration [56]. However, this hybrid packaging method effectively integrates different functional devices into a compact single package platform. A similar integration approach was demonstrated by Infineon [57]. Combining the lead frame and PCB structure, the intelligent power module integrates the driver ICs with 3 phase inverter power stage realizing a miniaturized system with enhanced functionalities [57].

The second method is based on interconnections using direct-plated via process [41], [47], [58]–[60]. In order to form these connections, the power dies and substrate are isolated with polymer dielectric layer, and cavities are drilled on top of terminals on the dies using laser. The cavities are then filled using Cu electroplating process, forming around 150um thick Cu of routing layer. As a base substrate, DBCs or lead frames were used. This method also utilizes the existing power assembly technology, but combines it with standard PCB build up process to realize a power embedding structure.

The active gate drivers have been invented to address the EMI noise of SiC devices more directly. Different from previous methods which attempt to reduce the parasitics related to the gate driver interconnections, active gate drivers control the current and voltage slopes at the turn-on and turn-off transients by adjusting gate resistance, gate source voltage and gate current. This active control of di/dt and dv/dt allows enhanced switching behavior of power devices by optimizing switching losses, reverse recovery current of the freewheeling diode, turn-off overvoltage, switching delay times, and electromagnetic interference (EMI) [61], [62].

Different ways to control and suppress the common mode noise generated by dv/dt during switching using gate drivers or filters have been proposed. However only a small number of work has been published to minimize the effect of common mode noise by minimizing the parasitic capacitance of a power module package. In DBC substrates, the reduction of the overlapping area between the ground plane and a trace or plane that has potential fluctuations, has been suggested. By trimming the copper trace on the top-side of the DBC, the parasitic capacitance is minimized without affecting other layout parameters [63]. 3D power stacking structures also have been suggested to minimize the conducted EMI noise through the parasitic capacitance of the package. By placing the terminal which has the highest voltage fluctuations in the middle of a 3D sandwiched structure, drastic decrease in the parasitic capacitance between the terminal and the heat sink is achieved [43], [52].

B. Advances in Thermal Management

Several alternatives to wire bonding have been introduced for top-side interconnection of power dies to enhance the thermal dissipation of the package. Multiple of Cu posts are soldered or sintered onto the die metallization for improved thermal performances [64], [65]. Larger area joints are demonstrated using lead frames [66]. These types of bonding utilize the whole metallization area of the die using either solder or sintered joints [67]. More recently, there has been a noticeable increase in the implementation of electroplated vias to form the top-side interconnections [47], [59], [68]. These approaches use laser drilling of vias on dielectric layers, and fill them up with Cu with electroplating process to form the connections. These large area contacts provide additional thermal path contributing to the reduction of thermal resistance of the package.

Fig. 9(a) shows a thick lead frame structure which appear in many of the recent power module package solutions as a

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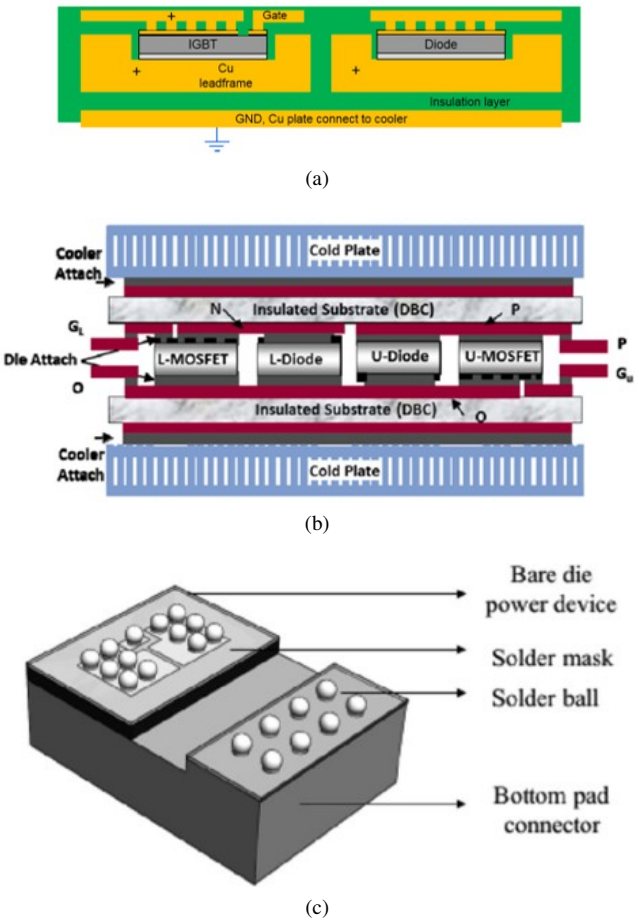

Fig. 9. Advances in packaging for enhanced thermal management. (a) Thick lead frame as a substrates [47], (b) Double-sided cooling with DBC substrates on top and bottom [45], (c)Wire bonless 3D flip-chip package [69].

bottom substrate [47]. The thick lead frame substrate, which is usually made of copper, spreads heat effectively before it passes insulation layers. Also, it simplifies and eliminates some number of package layers, such as heat spreader and solder substrate attach, resulting in reduced junction to case thermal resistance [44], [50], [70].

The double-sided cooling approaches have DBCs or other substrates on both top and bottom side of the module used as a routing layer and a substrate, as shown in Fig. 9(b). Increased contact area on both sides of the die allows more uniform temperature distribution of the structure, reducing the peak temperature as well as the overall package thermal resistance [45], [54], [71]–[73]. Recently, a chip scale package is suggested as an alternative way to achieve double-sided cooling (Fig. 9(c)). A Power die is assembled on a metallic connector with solder balls, and then flip-chip bonded onto a substrate, allowing heat dissipation from both sides of a power die [69].

C. Advances in High-Temperature Operation

Die attach materials proven for standard Si-based module's temperature range (150°C–175°C) have low glass transition temperature that are not suitable for high-temperature operation of SiC-based modules. Moreover, a special attention

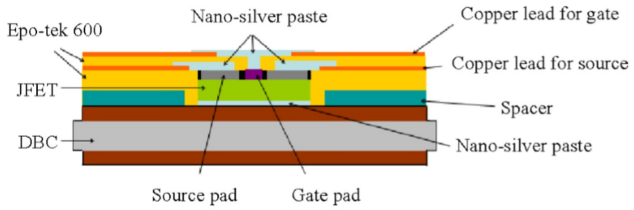

Fig. 10. Demonstration of high-temperature SiC power module [84].

needs to be paid to matching the CTE of die, die attach, and substrate. Many alternatives to conventional solder have been suggested to be implemented in future SiC power modules considering these two aspects [74]. Gold-based solder materials, such as eutectic AuSn, have gained its popularity for high-temperature performance (>280°C), high electrical and thermal conductivity, and easy fluxless soldering [75]. However, they are only suitable for small die applications because of their stiffness property, and high cost. A two-step fluxless bonding process using silver-indium alloy has been suggested for high temperature die attach [76]. This process also is a fluxless bonding method that has low process temperature (206°C), but has high re-melting at around 780°C, making it a viable alternative for high temperature and reliable die attach material. On the other hand, the TLP (transient liquid phase), or SLID (solid-liquid interdiffusion bonding), bonding is considered as a die attach material that satisfies the requirements for SiC modules at a relatively lower cost [77]. Costly SLID method using AuSn was also demonstrated [78], and showed great potential in high power and high reliability die attach applications [78].

Silver sintering is also a bonding method renowned for low temperature process (>220°C) and high melting point (961°C) which has many advantages such as high thermal conductivity and enhanced reliability in thermal and power cycling [79], [80]. There still are challenges, however, to be solved related to complicated and costly assembly process that comes with pressure and surface metallization, and related to the reliability issues such as volatile entrapment in large dies. More recently, sintering interconnections based on nano-copper materials have been introduced [81], [82]. The demonstration of organics-free nano-copper sintered die attach shows improved manufacturability with design flexibility for stress management, making it a promising alternative for high temperature die attach material for SiC devices [82].

Several types of polymers were suggested as a high-temperature encapsulant material [40]. Candidates that have the glass transition temperature (Tg) higher than 250°C include polyimide, Benzocyclobutene, Silicone elastomer [35], [40]. Namics developed a new resin technology with high thermo-stability for SiC power module applications [83]. By innovative formulation incorporating high thermal conductivity fillers, the new encapsulant material has high Tg of 293°C, showing improved performance at high temperature aging tests [83].

Actual operations of SiC module package under high-temperature conditions were demonstrated [84], [85]. The

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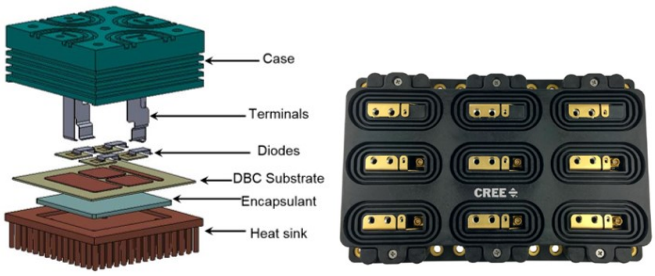

(a) (b)

Fig. 11. Advances in high voltage isolation. (a)15kV power module enabled by a cavity structure [89], (b)10kV power module from Cree [90].

SiC JFETs and SiC diodes are packages on a DBC as shown in Fig. 10, and the top-side connections are made applying multiple layers of polyimide and nano-silver paste for isolation and electrical connection, respectively. Under ambient temperature of 250°C, the I-V characterization of packaged SiC dies was conducted, and reliability assessments such as high temperature storage and thermal cycling with maximum temperature of 250°C were characterized [84]. Other research activities involving gate drivers in high-temperature characterization of SiC modules were presented [86]–[88]. A SiC MOSFET module with integrated SOI (silicon-on-insulator) gate drivers showed the capability to operate the module up to 200°C. Materials used for SiC power module, as well as the components used for gate driver and passives were carefully selected based on their maximum temperature ratings.

D. Advances in High-Volatage Isolation

The most commonly used encapsulant materials for standard power module have dielectric strengths approximately ranging from 10kV/mm to 20kV/mm. Recent dielectric materials developed for high-voltage and high-temperature power modules have dielectric strength from 35kV/mm to 46kV/mm [91]. However, as previously mentioned, these materials need to be improved and assessed for long term aging at elevated temperatures [40]. Modification of DBC substrates to enable 15kV rating power modules have been demonstrated [89], [90]. A cavity structure was cut underneath the DBC substrate, and reduction in the maximum electric field was demonstrated [89]. Increasing the thickness of ceramic layer and changing its material properties also was effective in increasing the level of isolation. Wolfspeed has demonstrated a 10kV SiC module package (Fig. 11(b)) by changing the substrate thickness and its material properties [90].

E. Advances in Packaging Elements

This section is to see how each packaging element technology has progressed, and to capture some of the technology trends that were not mentioned in previous sections.

Interconnection technologies have been improving from Al wire bonds to methods that can increase reliability, have higher current handling capability, and shorten the length as presented in Fig. 12. For the power modules that have existing system designs, wire bonds have not been replaced, but rather have been enhanced. Cu wires and ribbons were introduced to lower the resistivity of wires and improve power cycling performances [92], [105]. The transition from Al to Cu, however, required modifications in metallization on the top surface of the dies as a consequence, which changed the process and cost considerably. Wire bonds made of Al/Cu composite (Al-clad Cu) was suggested to combine the benefits of both materials [93]. Excellent thermal and electrical properties of Cu with softness and good bonding characteristics of Al resulted in reliable joints without any additional metallization processes [93]. For more revolutionary top-side interconnection designs, several alternatives to wire bonding that were discussed in previous section are shown in Fig. 12.

Several variations of DBC substrate technology have been used depending on the specific needs for the package. Considering the thermal conductivity and CTE matching characteristics of the ceramics, Al_2O_3, Si_3N_4, AlN, and AlSiC materials were selected. BeO has the highest thermal conductivity, however, are often avoided due to its toxicity during the process. The DBA (direct-bonded aluminum) substrate, which has aluminum metallization replacing the copper, was proposed to alleviate the thermo-mechanical stress and increase the reliability at the cost of lower thermal conductivity [106], and its structural variations are suggested in [107]. The aforementioned variations are related to material changes based on similar structure where the ceramic layer is sandwiched between two metal layers. On the other hand, different stack of the substrate layers such as IMS (insulated metal substrate) and thick film technology are introduced [15], [108]. IMS consists of insulating resin sheet with thick copper foils that enables low cost fabrication with high reliability performances. In thick film technology, either thick conductive paste or thick conductive paste with thick metal foil is bonded with ceramic substrate. This approach has advantages in temperature cycling reliability and integration with IC and passive components to form hybrid modules [108]. More recently, substrates based on thick lead frames with thin film insulation layer were developed which simplified the stacked layers [44], [109]. The thick conductor layer acts as a heat spreader, reducing the thermal resistance significantly. This structure also allows low thermal impedance, which is beneficial in the case of short power pulses [44].

Noticeable trends on top-side interconnection, substrate, and die attach technologies were observed. Firstly, recent packaging solutions on the top-side interconnection are moving away from wire bonds, due to numerous advantages that flat and large area joints can bring. Secondly, there were attempts to simplify the package layers in substrate technologies. The functions of each layers are combined into the reduced number of layers. In addition, the metallization of substrate became much thicker to handle higher current, and to improve the heat spreading. Thirdly, the die attach technology is shifting from solder alloys to sintered joints in order to achieve higher temperature stability and higher thermal conductivity. Demonstrating those features with simple and cost-effective processes, and evaluating them in field reliability would be a valuable future direction.

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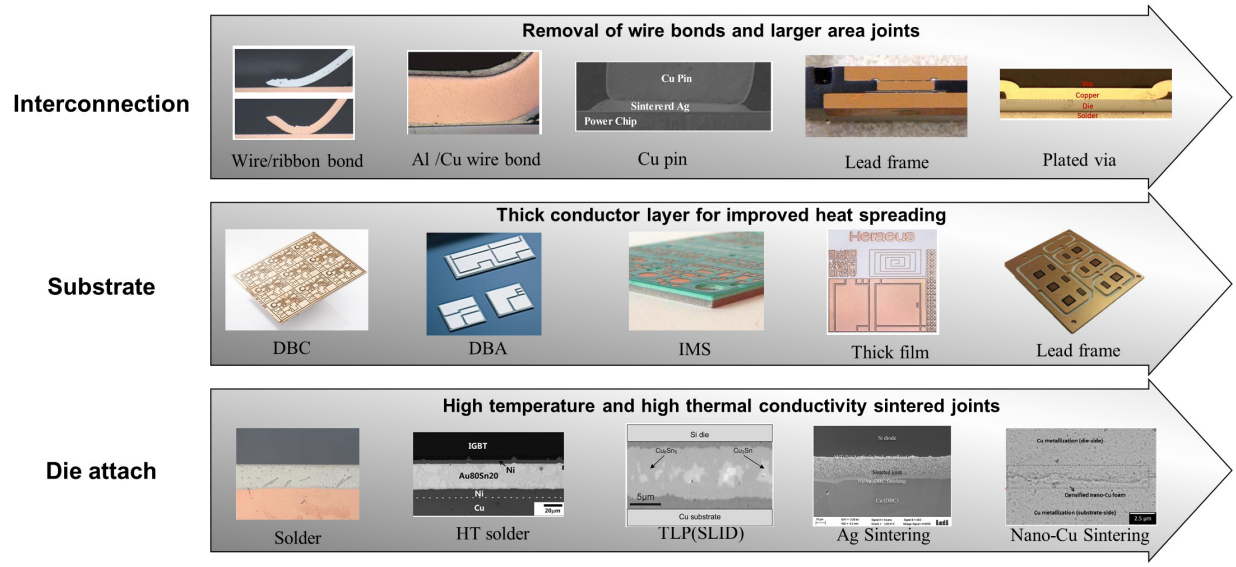

Fig. 12. Advances in packaging elements. Interconnection technologies have progressed from wire and ribbon bonds to Al/Cu composite, Cu pin, lead frame, and electroplated via [59], [92]–[95]. Substrate technologies have progressed from DBC to DBA, IMS, thick film, and lead frame [47], [96]–[99]. Die attach technologies have progressed from solder to high-temperature(HT) solder, TLP(or SLID), Ag sintering, and nano-Cu sintering [100]–[104].

F. Advances in Packaging Designs

Leveraging the advances in the packaging elements, innovative package structures and designs have been derived from the standard power module. Some examples show only minimal change in the packaging elements, but the impact of the replacement to the overall package performance is not trivial. Although it is difficult to group them, the recent advancements in package designs are classified into four categories based on their similarity in the module structure and design purpose. Fig. 13 presents the evolution of each category, which are overmold, double-sided DBC, component integration, and 3D power integration.

The overmold structures are lead-frame based power modules where power dies are directly attached to the lead frames, and overmolded with epoxy molding compounds. The wire bonds on the top-side of dies for power terminals are replaced with lead frames and solder forming a larger area joint. In most of the existing overmold structures, however, the gate terminals are still connected using wire bonds. Studies on overmold structures demonstrated drop in package internal inductance, decrease in power loss, improvement in thermal resistance, and longer power and temperature cycling life time [44], [50], [70], compared to the standard designs. The reduction in inductance and power loss is attributed to the flat and short electrical length and arrangement of lead frame interconnections. Considering the top-side heat spreading in addition to the bottom-side, the thermal resistance of this structure decreases significantly compared to the standard alumina DBC substrates. Increased contact area of the die and the lead frame allows more uniform temperature distribution of the structure, reducing the peak temperature, and consequently the induced stress on the dies. This reduction in stresses is reflected to the improvement of life time under power cycling reliability conditions [70].

One remarkable advantage of the overmold structure is the enhanced modularity. These structures usually comes with thin profile, reduced footprint, and low weight. Converters using multiple of these repetitive structures simply by stacking them would result in dramatic improvement in power density of the system including cooling management [114]. Volume and weight constrained applications such as EV/HEV would benefit the most from overmold structures with the enhanced modularity.

The double-sided DBC structure shares very similar features with the overmold structure. The removal of wire bond offers very low package inductance and reduction in thermal resistance enabled by double-sided cooling. In order to compensate for the different thicknesses of dies, metal posts are often inserted between the die and top-side DBC. The advantages of double-sided DBC structure over the standard module, such as low-loss, improved thermal performance, and cost-effective manufacturing are demonstrated [45], [54], [71]–[73].

The component integration structures aim to combine multiple functional components into one package module. The main motivation of this structure is to integrate gate driver ICs and/or decoupling capacitors with the power devices in a compact module, and thereby enable fast-switching package. As mentioned before, shortening the interconnection length between the power device and gate driver will reduce gate loop inductance which results in increased switching speed. Moreover, decoupling capacitors will remove the effect of parasitic inductances of bus bars or connectors outside of the package. Thus, it is desirable to package these components as close as possible with power dies for efficient power conversion.

The 3D power integration structures go one step further in improving the package integration density to solve the fast-switching transient issues. This unique configuration takes advantage of the third dimension, shortening the interconnection length of main switch loop, and shows extremely low parasitic

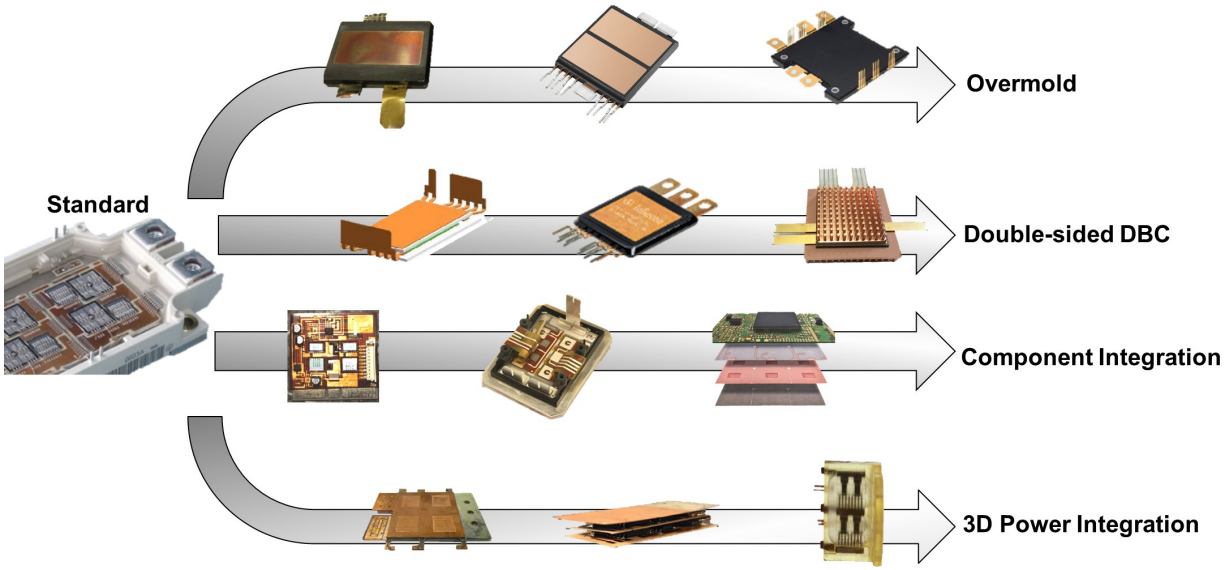

Fig. 13. Advances in packaging structures. Overmold structures show compact and flat form factor which strengthens the modularity [44], [95], [110]. Double-sided DBC structures allow heat dissipation from both top and bottom side of the module [71], [72], [111]. Component integration structures combine heterogeneous functions into the module to enable fast-switching [46], [112], [113]. 3D power integration structures have power dies stacked in vertical direction which alleviates the di/dt and dv/dt issues [30], [51], [53]

inductance. The output terminal, which is the main source of conducted EMI noise, is placed in between the positive and negative terminal, isolated from the heatsinks that are electrically grounded. This configuration eliminates a direct path for the common mode currents to conduct, resulting in minimizing the dv/dt issue of parasitic capacitance that exist in conventional DBC based packages [52]. Combining components other than power dies such as decoupling capacitors [51], gate drive ICs [53], and heatsinks [30] into the 3D module has been demonstrated, which shows the capability and flexibility to incorporate heterogeneous functions into the package. Due to the challenges in maintaining the temperature uniformity of the module, studies emphasized the need for increased thickness of conducting layer [51], or increased heat capacity of the module [30], for higher thermal performances.

IV. Emerging Issues

A. Novel Converter Topologies and Need for Current Switch Modules

As an alternative to hard switching, which suffers from high di/dt and dv/dt associated with fast switching (as mentioned in previous sections), soft switching was introduced [115]–[120]. Soft switching converters are usually claimed to have reduced switch stresses and switching losses, better device utilization, reduced size of filtering elements, higher power density, and reduced EMI, which alleviates the difficulties with fast switching transients [121]. However, the effectiveness of soft switching should be assessed in relation to specific applications considering the additional complexity and cost from components, since it may not always offer the benefits mentioned above [121].

Current source-based converters using current switches, which consists of series connected switch and diode, are widely used in applications such as high-power industrial motor drives [122], renewable energies [123], and solid-state transformers (SST) [124], [125]. These current source converters are well suited for zero-current and zero-voltage based soft switching, and are predominantly employed with soft switching in the previously mentioned emerging applications [126]. The advent of SiC devices are expected to scale up the voltage and power, while further reducing the volume of these emerging converters.

The current switch module has an unconventional configuration, in which the series diode is connected with a regular active switch to enable the reverse blocking. Fig. 14 shows a few combinations of these current switches that can be used in soft-switching current source converters [127]. Except for the reverse blocking IGBT, which is a single die that has limited options of manufacturers, most researchers are forced to use series connected discrete switches to form a current switch as shown in Fig. 15 [127]. In such an arrangement of discrete components, bond wires and bus bar create unwanted parasitic inductances in the circuit, which leads to increased turn-off duration and losses, and are usually considered as the primary cause of malfunctioning packages [127]. This packaging structure also comes with inherent challenges associated with high voltage stresses that are considerably larger than regular switches with the same ratings [126]. Thus, the design of current switch module packaging requires an understanding of these unconventional challenges under the effect of overall switch operation and accurate physics-based optimization.

To sum up, the soft switching schemes with the combination of high-performance SiC devices provides further reduction in losses at higher frequencies, making the current switch modules an extremely competitive building block of power electronics for the emerging converters over conventional voltage source converter topologies. However, the inherent package challenges need to be addressed in design and fabrication of

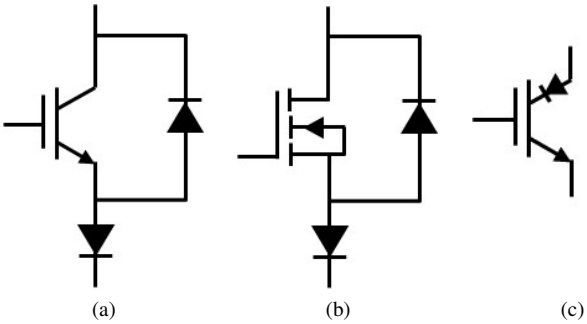

Fig. 14. Possible options for current switches. (a) IGBT and diode, (b) MOSFET and diode, (c) Reverse–blocking IGBT.

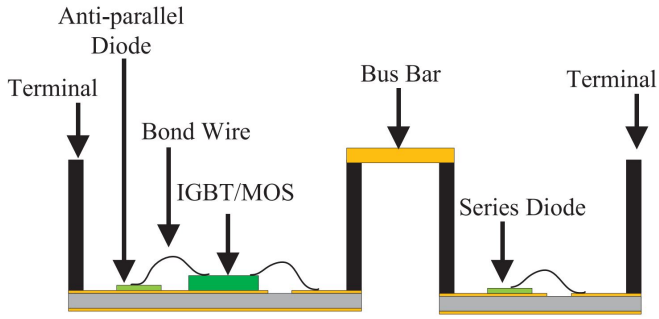

Fig. 15. Package configuration for a current switch. Discrete modules are connected in series with a bus bar [127].

high-voltage current switch modules to take full advantage of the SiC devices and novel soft switching topologies.

B. Low-Temperature Challenge in Space Explorations

SiC devices can potentially be used in aerospace applications where extremely wide temperature range is expected. For instance, the electronics used in missions to the moon or mars need to survive wide ambient temperature cycling of -180°C to 125°C, and -120°C to 85°C, respectively [128]. Since most electronics in these space explorations are packaged based on earth-like ambient, they are kept in warm boxes to maintain their operation at extremely low-temperature. As SiC devices are being evaluated for these conditions, and are showing promising results [129], packaging technologies that are compatible with these harsh environment without the use of warm boxes, are need to be developed. One of the biggest challenges associated with the low-temperature is the large stress on die attach interfaces induced by large CTE mismatch from the thermal cycling. Also, materials that are flexible and compliant in room temperature, such as silicone gel, can become rigid at -180°C, creating significant stress levels within the package [130]. Therefore, the future directions for SiC packaging in aerospace applications would firstly be developing and evaluating substrates that closely match the CTE of the die to minimize the stress. Secondly, the other direction should be developing die attach materials that remain malleable at extremely low-temperature. In recent research activities, the properties of SiN and Indium solder, as a substrate and a die attach, respectively, are evaluated and characterized at the extreme temperature range of -180°C to 125°C [128], [130].

V. Summary

The proliferation of SiC devices and their potential performance benefits are witnessed in many areas of power electronics. Recent commercially available SiC power modules, however, are packaged in standard method that are used to package Si-based devices, preventing these novel SiC devices to fully take advantage of their potential benefits.

The shift from Si to SiC requires four main packaging challenges to be addressed in future power modules, namely, fast switching transients, thermal management, and high-temperature operation, and high-voltage isolation. The technical features and requirements associated with those challenges were discussed in this study.

Innovations on power module packaging technologies that addresses the challenges were reviewed. The advances on the basic packaging elements as well as packaging structures were highlighted, and common features of each category was captured to see the trend in advanced power module packaging. Upcoming issues associated with the novel soft switching converter topologies, and related to space exploration applications are introduced.

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