

A Non-Random Exploration based Method for the Optimization of Capacitors in Power Delivery Networks

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Abstract—This paper proposes a non-random exploration based method to optimize the response of power delivery network (PDN) using the minimum number of capacitors. Unlike previous optimization methods which are based on either full search or random exploration (machine learning etc), the present method requires few simulations to converge to the minimum decoupling capacitor solution. The results show that the proposed method is more robust based on comparisons.

Keywords—Decoupling capacitor, target impedance, power delivery network (PDN).

I. INTRODUCTION

Designing a robust power delivery network (PDN) has become challenging with the increase in operating frequency and current load in ICs that have low voltage requirements. A typical technique to minimize impedance of PDNs is by using decoupling capacitors (decaps). The level of voltage fluctuation below the threshold level at the IC port can be guaranteed by assigning proper decaps that reduce the self-impedance below the target impedance in the frequency range of interest. However, as system sizes continue to shrink, using a minimum number of decoupling capacitors in the PDN to meet the target impedance is becoming critical due to space constraints. We therefore discuss a method in this paper to meet this objective.

Numerous methods have been proposed to optimize decap design in PDNs. Stochastic optimization methods such as genetic algorithm and particle swarm optimization have been utilized for the selection and placement optimization of decaps [1], [2]. In [3], [4], a reinforcement machine learning technique is proposed to obtain optimal decap designs. However, these methods are based on random exploration; therefore, a large number of PDN simulations are required to find the optimal design especially when the target impedance is difficult to achieve.

In this paper, we propose a method to optimize PDNs with the minimum number of capacitors. During the iterative process, the decaps are chosen through several steps, thereby optimizing the PDN to meet the target impedance in the frequency range of interest. Compared to full search, machine learning (ML), and commercial tools available, the method discussed in this paper provides for fast convergence with significantly fewer PDN simulations.

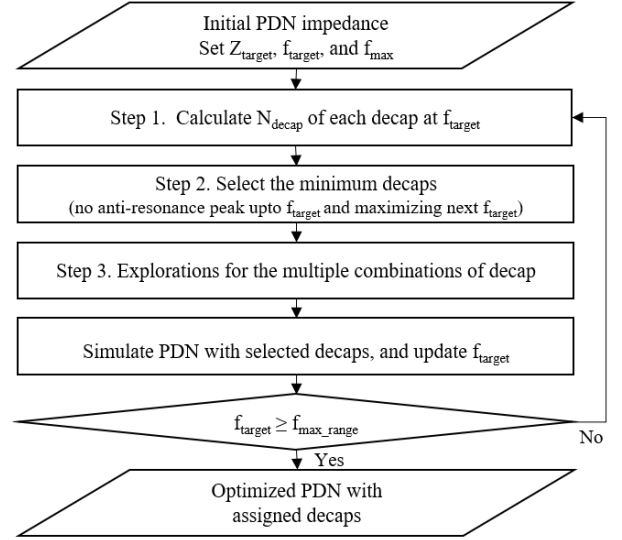


Fig. 1. Flowchart of the proposed decoupling capacitor optimization method

II. PROPOSED METHOD

A. Details of the Technique

The proposed method is based on an iterative process with three steps per cycle, as shown in Fig. 1. In each cycle, decaps are chosen from a decap library and assigned to the PDN. The lowest frequency at which the self-impedance at the IC port is greater than the target impedance is set as the target frequency, f_{target} where this parameter is updated after a decap is assigned in each cycle. For PDN analysis in this section, we use the PDN equivalent circuit shown in Fig. 2. Here, the decap is represented using a capacitor with equivalent series resistance (ESR), inductance (ESL), and surface mount inductance.

In step 1, the number of each decap required to decrease self-impedance below the target impedance at f_{target} is determined using the equation:

$$N_{decap} = \left\lceil \frac{|Z_{decap}(f_{target})|}{Z_{target}} \right\rceil \quad (1)$$

where $Z_{decap}(f_{target})$ is the impedance of each decap at

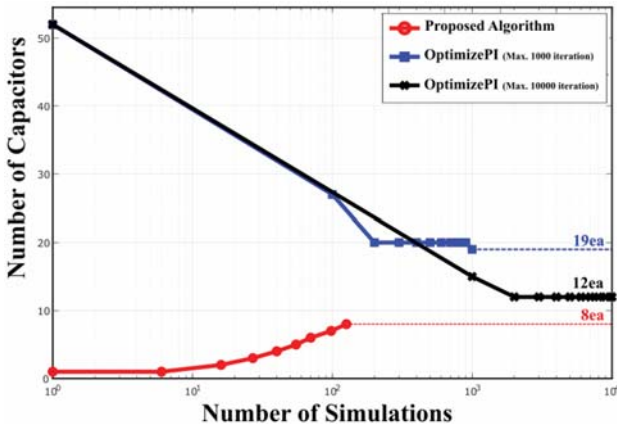


Fig. 5. Convergence comparison for the proposed method and the optimization function when Z_{target} is 0.15Ω in the frequency range up to 45 MHz

B. Test Results

Using the proposed algorithm, the decap solution that meets the target impedance over a frequency range up to 70 MHz can be obtained, as shown in Fig. 4. Here, the minimum number of decaps are selected in each cycle from the decap library consisting of 83 different decaps to satisfy the target impedance of 0.03Ω . Note that f_{target} is always increased after each cycle is completed, and the iterative process for the optimization is terminated when f_{target} exceeds 70MHz. To achieve this decap solution, the proposed method only requires 85 PDN simulations.

To verify the performance of the proposed method, the results obtained using the proposed method are compared with those of full search and ML (deep Q-network, DQN) based method for several target impedance cases. The results are summarized in Table I. Here, 35 different decaps in the decap library are considered for the selection. Using the proposed method, the same number of assigned decaps can be achieved as the optimal decap solutions that can be obtained by the full search and DQN based method. To obtain the decap solution using the full search and DQN-based method, a large number of PDN simulations are required, but the proposed algorithm requires less than 100 PDN simulations. This demonstrates the advantages of the proposed algorithm in terms of computing time for PDN optimization.

III. ON-BOARD PDN OPTIMIZATION

We apply the proposed method where data is gathered using a commercial tool (Sigriy OptimizePI) [5] for on-board PDN optimization and compare the result with the decap optimization function provided in the tool. Unlike the case of the PDN equivalent circuit model, Z_{decap} in (2) is unavailable in step 1 because of the parasitic L and R between the cap node and IC port. Therefore, to obtain N_{decap} for each decap in step 1, we use the self-impedance at f_{target} when each decap is assigned to the designated cap node. Here, we assume that the decap placement priority is determined in the order in which it is close to the IC port.

TABLE II. OPTIMIZED DECAP RESULTS WITH THE PROPOSED METHOD AND THE OPTIMIZATION FUNCTION

$Z_{target} = 0.15 \Omega$, $f_{max} = 45$ MHz		
Method	Number of Simulations	Number of Decaps
Proposed method	126	8
Optimization function	1,000 (Max. setting)	19
Optimization function	10,000 (Max. setting)	12

Using the proposed method and the provided optimization function from the tool, we optimize a four-layer PCB board consisting of VRM, power planes, and the target IC. The optimized decap results are provided in Fig. 5 and Table II. Two results from the optimization function in the tool are obtained by setting the different maximum number of PDN simulations, 1,000 and 10,000. As the simulations continue, the optimization function provides fewer number of decaps, and the number of decaps converges to 19 and 12, respectively. Using the proposed method, the decaps keep being assigned until the target impedance is satisfied in the frequency range of interest. The result obtained by the proposed method shows that only 126 PDN simulations are required to obtain the final decap solution, and the number of decaps of the solution is fewer (8 decaps) compared to the optimization function.

IV. CONCLUSION

This paper proposes a non-random exploration based method to minimize the number of decaps for PDN optimization. During the iterative process, the minimum decaps are assigned to the PDN in each cycle to increase the frequency range where the PDN meets the target impedance. For verification, the proposed method is applied to various examples. The results show that the proposed method provides the optimized decap solution with significantly fewer number of PDN simulations compared to full search, ML-based method, and a commercial tool. Our conclusion is that an algorithm based on domain expertise is sufficient for addressing this problem as compared to more sophisticated methods.

REFERENCES

- [1] J. Y. Choi and M. Swaminathan, "Decoupling capacitor placement in power delivery networks using mfem," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 10, pp. 1651–1661, 2011.
- [2] P. Kadlec, M. Marek, M. Štumpf, and V. Šeděnka, "Pcb decoupling optimization with variable number of capacitors," *IEEE Transactions on Electromagnetic Compatibility*, 2018.
- [3] H. Park, J. Park, S. Kim, D. Lho, S. Park, G. Park, K. Cho, and J. Kim, "Reinforcement learning-based optimal on-board decoupling capacitor design method," in *2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*. IEEE, 2018, pp. 213–215.
- [4] L. Zhang, Z. Zhang, C. Huang, H. Deng, H. Lin, B.-C. Tseng, J. Drewniak, and C. Hwang, "Decoupling capacitor selection algorithm for pdn based on deep reinforcement learning," in *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+ SIPI)*. IEEE, 2019, pp. 616–620.
- [5] OptimizePI. [Online]. Available: https://www.cadence.com/en_US/home/tools/ic-package-design-and-analysis/si-pi-analysis-point-tools/sigriy-optimizepi-technology.html