Design And Demonstration of 1µm Low Resistance RDL Using Panel Scale Processes for High Performance Computing Applications

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***Abstract*— This paper presents for the first time the latest challenges and solutions to enable electronics packaging redistribution layer (RDL) scaling to 1µm and beyond. The focus on RDL scaling for this paper is on how to scale semi-additive processing (SAP) for next generation high performance computing applications such as 2.5D Interposers. This paper combines novel next generation photoresist materials developed by Tokyo Ohka Kogyo Co., LTD. (TOK) and process innovations to the traditional SAP process. Traditionally, challenges in scaling SAP are related to seed layer etching and photoresist materials selection. This paper address both of these challenges by exploring various seed layer metals and the potential impact they can have on the SAP process flow for enabling SAP scalability as well as novel photoresist development with TOK. Scaling dry films to have similar performance to a matching liquid photoresist is demonstrated in this paper. The 3D Systems Packaging Research Center remains one of the leaders in package RDL scaling and this paper discusses at length recent advancements that have been made to enable silicon like RDL scaling on glass panels.**

Keywords- RDL, High Performance Computing, Interposers

I. INTRODUCTION

Driven by emerging markets that are focused around the Internet of Things (IOT), 5G, artificial intelligence, cloud computing and autonomous driving high performance computing is experiencing unprecedented growth and demand. Increasing the logic to memory bandwidth as well as reducing power consumption at low cost are the key performance metrics for technology advancements in this area. To enable increases in logic to memory bandwidth critical dimension (CD) of the RDL traces must be reduced to meet these demands. For reducing power consumption high aspect ratio traces are required to offset power losses due to capacitive impacts. Traditional approaches to reducing CD are to leverage back-end-of-line (BEOL) technologies to reach on chip like dimensions [1]. However, utilizing this technology results in a low aspect ratio that is prone to high RC losses in the package. To reduce power consumption BEOL processing tries to leverage low dielectric constant materials to reduce capacitive losses and high numbers of traces to distribute line resistance. However, these types of dielectrics at packaging feature CD's can be expensive due to time of deposition and loss in reliability due to mechanical instability. Traditionally packaging has struggled to scale low-cost high performance processes as shown in figure 1. The goal of this paper is to demonstrate that the materials and processes are in place to support next generation chipsets that have CD's of 7nm and below. In this figure there is a clear RDL gap that exists between what package foundries are traditionally capable of and what wafer foundries are traditionally capable of.

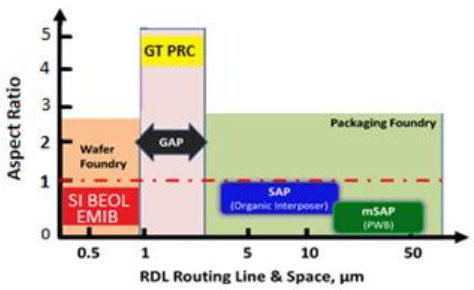

Figure 1. Gap between Si BEOL and Packaging RDL

II. SAP SCALING

Traditionally in electronics packaging the process by

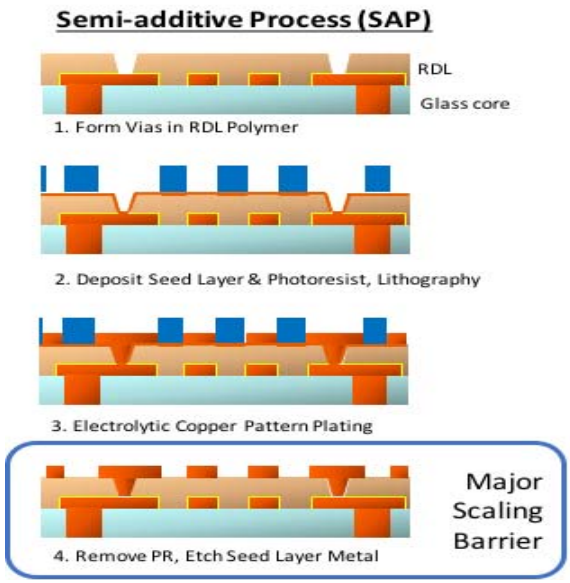

Figure 2. SAP Process flow with critical scaling barrier highlighted in blue.

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which RDL are fabricated is through Semi-Additive Process (SAP). This process flow is shown in figure 2 with the limiting process step highlighted. As the demands for high performance computing applications continue to increase the requirement of RDL critical dimension (CD) continues to be pushed. Seed layer etching and photoresist processes remain the critical barriers to scaling the SAP process for next generation electronic packaging architectures. As the CD of RDL is pushed to 1µm and below seed layer etch remains an increasingly complex problem. Traditional seed layers are approximately 100 – 200 nm for sputtered seed and up to 500 nm for electroless seed layers traditionally deposited onto polymers such as ABF and other polymers used in electronics packaging [2]. This remains a problem because during the seed layer etch removal process to ensure that the entire seed layer is removed one must target a thickness greater than that of the seed layer that was deposited. Traditionally it hasn't been a problem as the CD is large enough that the thickness of the seed layer is <10% of the final CD of the line. However, as the linewidth approaches 1µm (and <1 µm) RDL continues the seed layer thickness exceeds 10% and can be as high as 20% of the final CD target. At 1µm, the seed layer etch process often results in the lines to flop over due to undercut from the seed layer etch. It has also been demonstrated that the etch chemistries remove the seed layer faster than they remove the plated copper likely due to the grain structure differences between the plated copper and the sputtered as deposited copper. The second most critical scaling parameter for electronics packaging is the photoresist itself. The only technology capable of fabricating line and spaces of 1µm and below is back-end-of-line (BEOL) copper damascene processing. This process from a materials standpoint uses ultra-thin chemically amplified liquid resists on the wafer scale to etch fine line and spaces into the dielectric material, usually SiO_2. This process does not have a seed layer etch problem nor does it have a resist scaling problem due to the nature of the process flow. To scale SAP to match the CD capability of BEOL processing photoresists that are required need to be thicker and still maintain performance. In conjunction with this material requirement the lithographic tooling must also be able to meet a minimum resolution of 1µm or below [3]. However, scaling numerical aperture (NA) causes a loss in depth of focus (DOF) which makes maintaining CD throughout the thickness of these resists difficult for electronics packaging fabrication. Ultimately, without key innovations in technology for SAP processing the tradeoffs must be weighed from photoresist requirements, to seed layer etching technologies and the lithographic tooling requirements. The remaining sections of this paper discuss and explore various approaches that can be explored to compensate for critical transitions required to scale SAP to 1µm[4].

III. SAP PROCESS FLOW

This section describes in detail the process flow that was utilized for all the experiments that will be discussed throughout the remainder of the paper unless otherwise specified.

(1) Dielectric Film Lamination

The glass is precleaned with acetone, IPA, methanol and O2 plasma. A vapor silane is applied to the surface prior to lamination. The 10 µm T61 is laminated on a glass panel using a vacuum hot press laminator. The temperature of lamination is 130 °C and is cured at 180 °C.

(2) Metallization

A conductive metal seed of 50 nm thick titanium and 150 nm copper is deposited using sputtering. Additionally, samples that have other seed metals such as chromium are deposited in thicknesses of 200 nm.

(3) TOK Photoresist Processing

TOK photoresists are then spin coated or laminated onto the top of the conductive seed metal. All the films were optimized to be deposited with a thickness of 7 µm. TMMR®P-W1000T which is a non-chemically amplified liquid resist was spin coated and then pre-baked. The other films used in this study were a PC series developed by TOK. This PC series is a chemically amplified photoresist that is available as a liquid and dry film. The PC-0471W-F8 (PC dry film) as received has a thickness of 8µm and after a pre-bake step it shrinks to 7µm. The PC-0471W (PC Liquid) photoresist is spin coated to achieve a thickness of 7µm and is also pre-baked. All these films are ready for exposure after the completion of their pre-bake steps.

(4) Exposure and Post-Bake:

After the photoresist has been pre-baked they are then exposed in various photolithographic steppers. Each stepper is used to deliver a range of exposure doses across the surface of the panel. These exposure doses are varied based on the recommendations from TOK. This provides a wide range of exposure doses across each of the panels to minimize the possibility for panel to panel variations. Following the exposure, the photoresist is subjected to a post-bake step.

(5) Development

The development process used was puddle development where the wafers are coated in 2.38% TMAH and then spun two times for 30s each.

Any changes to the process flow or additional data that is presented in this paper will be discussed in detail in the later sections.

IV. Results and Discussion

In the following section, discussion will be dedicated to, A) the photoresist material selection and discussion, and B) the overall process with a focus on seed layer.

The first aspect of this paper is photoresist material selection and discussion. For the purposes of this paper a small photoresist matrix was selected. Based on scaling requirements and understanding of fundamental transition points in electronics packaging three photoresists were selected. The first is a positive non-chemically amplified liquid photoresist by TOK called TMMR®P-W1000T. The next is PC-0471W which is a new photoresist material developed by TOK which is a positive chemically amplified photoresist that is available in liquid and dry film formats. This matrix allows us to examine when the limit for non-chemically amplified photoresists is reached as well as dry film photoresists. For the dry-film a positive tone chemically amplified photoresist was selected as opposed to the more traditional negative dry-film due to inherent swelling challenges that exist for negative tone dry-films. These photoresists typically, in the semiconductor industry, are shown to have a poor

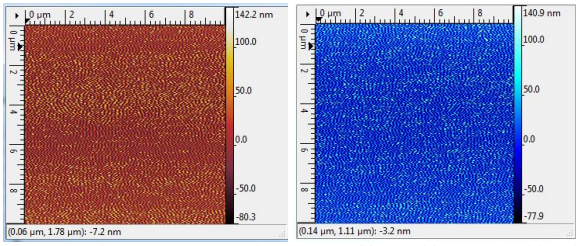

Figure 3. Surface AFM scans of a) PC Dry film and b) PC Liquid resist after pre-bake conditions

resolution. To make sure that each of the photoresists could be compared accurately, and more specifically the liquid and dry-film photoresists, certain process optimizations were performed. The liquid photoresist was spun on using traditional spin coating processes. The dry film was vacuum laminated onto the surface of the conductive seed metal using 0.3 MPa of force at a slightly elevated temperature. It was expected that due to the nature of processing the photoresist into a dry-film that the surface roughness should be greater compared to the liquid version of the resist. To examine this potential difference in surface topography various methods were investigated, however AFM surface roughness measurements performed using a Veeco Dimension 3100 Atomic Force Microscope (AFM) are shown in Figure 3. The AFM was run in both tapping and contact mode however, tapping mode was chosen based off initial results that suggested contact mode was smearing the photoresist. However, after pre-bake it was observed that the surface roughness for the dry film was reported with an arithmetical mean deviation of the assessed profile (R_a) of 35.7nm. While for the liquid film the measured R_a value was found to be 34.2nm. As a result, we found that while there was a difference between the two films of 1.5nm overall the difference was not significant enough to produce performance differences for the two versions of the film. Additionally, the root mean squared (R_q) surface roughness values were also recorded. For PC dry film the R_q value was recorded to be 42.1nm and for PC liquid it was recorded to be 40.4nm for a difference of 1.66nm between the two versions of the film. This difference was deemed to be insufficient in dictating any type of performance difference between the two films. This proves that from a processing standpoint that liquid photoresists are capable of being converted into dry film formats that are traditionally used in electronics packaging specifically for large panels. Ultimately, for large panel processing dry film photoresists show known inherent challenges, from a physical aspect, in terms of scaling panel based RDL.

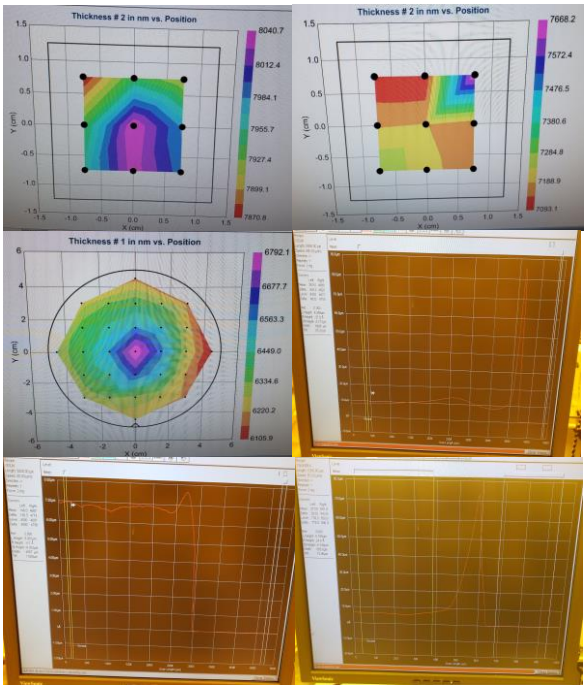

Figure 4. Ellipsometry scans of a) PC liquid b) PC Dry and c) TMMR®P-W1000T as well as profilometry scans to validate thickness of d) PC Liquid e) PC Dry and f) TMMR®P-W1000T

The second piece of the photoresist that had to be optimized was the thickness of the resist for the PC liquid as well as the TMMR®P-W1000T resist. The PC dry film was only available in 8µm as received and needed to be measured after pre-bake to see the final thickness. A target height of 7µm was selected for each of the photoresists, the PC dry film, PC liquid and TMMR®P-W1000T. The reason behind this selection was because the goal of scaling RDL using SAP on large panels is to have similar density but higher performance than silicon BEOL RDL. A height of 7µm gives plenty of tolerance for electroplating of copper of up to 6µm in thickness. This means that panel based RDL is much higher aspect ratio, while maintaining high density, ultimately lowering the resistance of the RDL traces by a factor of 4x when compared to the 1:1, width to height, RDL traces that have been demonstrated even in the most advanced silicon packages. To validate the thickness of each of the films both ellipsometry and profilometry were used. Ellipsometry measurements were conducted using a Woollam M2000 Ellipsometer and for profilometry a Tencor P15 Profilometer as shown in figure 4. The ellipsometry scans for the liquid films were repeated multiple times and the representative 7µm profilometry scans are shown. PC Liquid series ellipsometry and profilometry scans figure 4a and 4d allowed for optimization in the spin speed to be carried out to ensure that the final thickness of the PC liquid after pre-bake was 7µm. The PC dry film representative scans are show in figure 4b and 4e. PC dry film after pre-bake shows a final thickness on profilometer scans of 7µm this is consistent with the ellipsometry scans except for some areas where there were high spots likely due to processing variability at Georgia Tech and not due to the film quality itself. Finally, TMMR®P-W1000T ellipsometry and profilometry scans are shown in figures 4c and 4f, and verify that this film was also 7µm in thickness. This optimization was done to make sure that when comparing the three-photoresist matrix there is no performance differences induced from differences in surface roughness or thickness.

The three photoresists were patterned using a FPA-5510iv Stepper tool by Cannon with a NA of 0.18 at i-line wavelength. The three photoresists are show in figure 5 at optimum dose. The optimum dose was selected by examining top down CD-SEM images for the photoresists at doses varying to 20% plus or minus outside of the recommended dose from TOK. After varying the dose for each of the photoresists and examining them from top down CD-SEM the optimum dose was then cross sectioned. A FEI Nova Nanolab 200 FIB/SEM was used to perform the cross sectioning of the photoresist. A Pd/Au seed was deposited at low power and over a long time to ensure that no damage was induced to the photoresist. After which a 1nA cut is performed to clear out the bulk of the photoresist. After this cut a 0.7nA cleaning cut is performed. Finally, a 0.3nA cleaning cut is performed in order to remove any residue and to cross section the photoresist with little to no melting from the ion beam. As can be seen in figure 5 both the chemically amplified liquid and dry photoresists performed better than that of the non-chemically amplified photoresist. The CD change from bottom to top of the non-chemically amplified resist at optimum dose, which is substantially larger than the optimum dose for the chemically amplified films, was 800nm. While for the chemically amplified films the CD change from bottom to top was between 200 and 400nm. For scaling RDL processing on panels to 1µm and beyond due to CD broadening a chemically amplified photoresist is required. The photoresists reported in this paper provide much better CD control and a reliable 1µm CD resolution of across large panels.

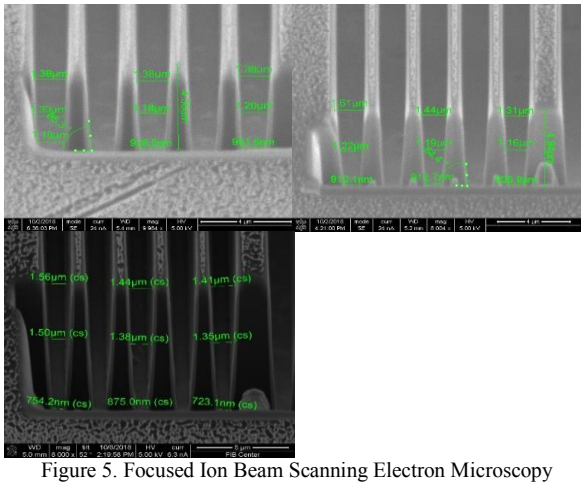

Figure 5. Focused Ion Beam Scanning Electron Microscopy (FIB/SEM) Cross sectional images of a)PC dry film b) PC liquid resist and c) TMMR®P-W1000T

	370nm	385nm	405nm
Cr	33.92%	23.22%	25.77%
Ti/Cu	47.17%	44.91%	46.49%

Table 1. Reflectance values of the seed layer as a function of wavelength

Previously discussed in this paper is the challenge of seed layer and its impact on scaling of SAP as a process to 1µm and beyond. From a tooling standpoint it is feasible to imagine that companies who make seed layer etch tools are working on technological developments that would allow for better control over the etching of the seed. However, the problem remains that unless the seed in the bulk can be selectively etched without impacting the seed layer under the traces than the physical challenges will always be present. Seed layers of up to 200nm are required in order to have low enough resistance for electrolytic plating of the copper traces. If the seed layer physically can not be shrunk to ensure electrolytic plating can take place than other solutions need to be explored. One of the aspects that is studied in this paper but that is not readily studied in literature is the impact of seed layer reflectance on photoresist performance. The changing of the seed layer to an entirely different material can provide ways to preferentially etch the seed metal in the bulk layers that is no longer desired after plating has taken place. For the purpose of this study chromium was selected as an alternative seed metal to the traditional titanium, copper seed layer that is used in electronics packaging today. To measure the reflectance values of the conductive seed layers at the litho tool exposure wavelength, a NanoSpec 3000 Reflectometer was used. The i-line wavelength that was used for the exposure of these photoresists is 365nm however, due to the limit of the reflectometer 370nm wavelength light was chosen to measure the reflectance of these seed layers reliably. As the wavelength is increased to h-line the seed layer reflectance delta between chromium and a titanium copper seed layer has a difference ranging between 13 – 21% as shown in table 1. A 150 nm thick Copper layer on top of a 50 nm Titanium seed layer is layer is compared to a 200nm chromium only seed layer. Surface AFM scans were performed to ensure that the surface of the seed layers was comparable. The AFM roughness scans for the conductive seed layers are shown in figure 6. The measured R_a and R_q value for the titanium and copper seed layer was measured to be 3.4 and 4.3nm respectively. For chromium the R_a value was measured to be 0.8nm and the R_q value was 1.0nm. While these values are different, since both measured values are below 5nm it is reasonable that the roughness of these seed layers will not have any significant impact on photoresist performance.

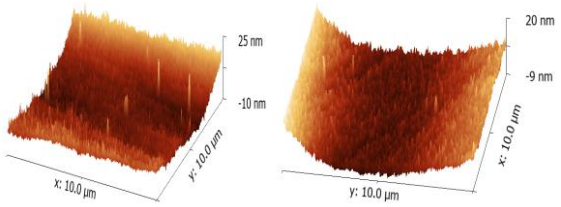

Figure 6. AFM roughness scans on blank a) Ti/Cu and b) Cr

After the conductive seed layer reflectance values were collected and the surface scanned with an AFM the photoresist was processed. The photoresists were spin coated or laminated in the same fashion that they were on the titanium copper seed. The photoresists were then exposed on the same Canon 0.18 i-line stepper tool and developed using the same process. The corresponding cross-sectional FIB images are shown in figure 7. When looking first at the PC dry film images and CD measurements for the two different seed layers it was observed that the minimum CD for the dry film was slightly larger on the chromium seed layer. However, an inverse effect was observed for the PC liquid where the CD profile was narrower on the chromium seed as compared to the titanium copper seed. For the TMMR®P-W1000T photoresist the mid and top height CD's were similar but the bottom CD for TMMR®P-W1000T was wider on chromium than it was on the titanium copper seed layer. Regardless of which seed layer was utilized the minimum CD that was able to be reached was 1µm. Thus, a pathway to differential chemical etching is presented for the first time in this paper. This technology would theoretically allow for scaling of SAP as a process to 1µm and beyond for electronics packaging. This is assuming that a chemical etch is available for the different seed layer that is used in the SAP scheme moving forward.

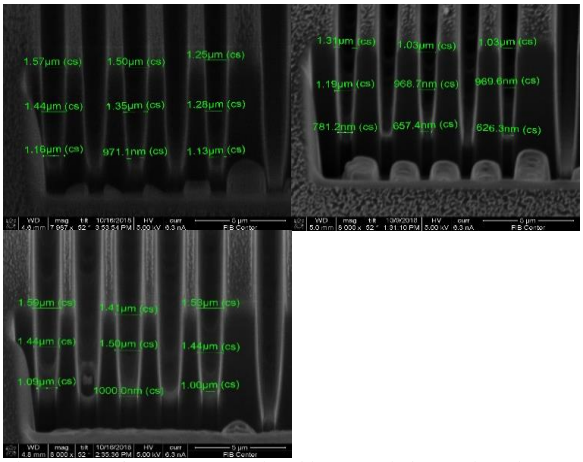

Figure 7. FIB/SEM Cross sectional images of photoresist spin coated on a 200nm chromium seed at optimum dose for a) PC dry film, b) PC-liquid resist and c) P-W1000T

V. SUMMARY

In summary, there is a demand for maintaining traditional electronics packaging fabrication process in the supply chain for next generation RDL. Historically the only process capable of fabricating RDL that have a CD of 1µm are below is silicon BEOL processing. This process scheme utilizes ultra-thin liquid positive tone chemically amplified photoresists that are processed and transferred to a SiO_2 like dielectric. However, the aspect ratio is usually limited to one and due to the inherent nature of silicon as a core material the loss of these traces can be very high. To run signals across large body size packages on a substrate like this will require areas of the package devoted to repeaters to ensure that the signal arrives at the receiver without degradation in the signal quality. This paper demonstrates the feasibility and manufacturability of high density, low loss RDL traces with a focus on two critical process. The first being the photoresist as a material. Materials developed by TOK demonstrated that 1µm CD are possible in electronics packaging fabrication process schemes. These photoresists are available in liquid and dry film formats which is extremely beneficial to the packaging industry which has historically utilized dry-film exclusively. However, these dry films have been demonstrated to have performance similar to that of liquid photoresists allowing for scalability of SAP as a process using either liquid or dry film. The second aspect of this paper was to examine a potential processing scheme change to overcome the seed layer scalability challenges that exist in electronics packaging. This paper presented for the first time that by using a different conductive seed metal than copper the photoresist could still be placed onto the conductive seed layer with no degradation in photoresist performance in achieving a CD of 1 µm.

VI. ACKNOWLEDGEMENTS

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