Multiphysics challenges with Heterogeneous Integrated Voltage Regulator based Power Delivery Architectures

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***Abstract*—Heterogeneous integration of power delivery circuits provides for a system-scaling opportunity in the post-Moore era. However, the integrated voltage regulator (IVR) poses complex design challenges. In this paper, the fundamental challenges and benefits, arising from the IVR-based power delivery system, in the electrical, thermal, and electromagnetics domains are analyzed. To verify the analysis, a comparison study of the regulator architectures with and without heterogeneous integration is considered. Also, metrics for the IVR design space are provided as measures to address its integration complexity and figure-of-merit.**

***Keywords*—Heterogeneous integration, integrated voltage regulator, power delivery, thermal management, and conducted EMI.**

I. Introduction

During the Moore's law regime, we witnessed continuous scaling of the logic circuits. Now, with the Moore's law of transistor-scaling slowing down, system-scaling has become a key enabler. Power delivery circuits, hitherto considered extraneous to the logic, have become crucial in improving system performance in the post-Moore era. The traditional power delivery circuits such as voltage regulator modules (VRM) are bulky, located on-board, and far away from their loads, e.g., microprocessors. If the power delivery circuits are heterogeneously integrated as an integrated voltage regulator (IVR) and moved closer to the logic either on-die or on-package, compact and high-performance power delivery architectures are possible.

The IVR-based compact power delivery architecture yields multiple benefits at the system-level. For example, Joule heating or I^2R loss is lower in the IVR than the VRM-case, as the IVR-case typically features compact interconnects with low parasitics and high input voltage with low current intake. But the benefits of the IVR-based power delivery can come at a cost of its design complexity, as it calls for heterogeneous integration of the miscellaneous components such as fast-switching power transistors like GaN [1], temperature-sensitive embedded passives for the LC filter, and high-heat generating loads like SoC. Their proximity poses complex multiphysics design challenges like thermal coupling and electromagnetic interference (EMI). In this context, we present a cost-benefit analysis of the heterogeneous integrated power delivery architecture. The major multiphysics domains considered in this paper for a switching regulator based power delivery include electrical, thermal, and electromagnetic issues, as shown in Fig. 1. Figures-of-merit in each of these domains are evaluated for the power delivery architectures with and without heterogeneous integration, considering the material, interconnect, device, and circuit-level limits.

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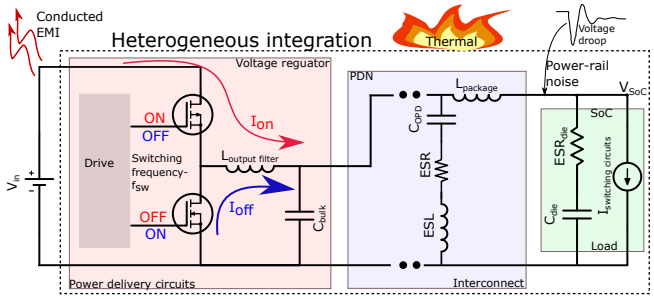

Fig. 1. Heterogeneous integration of power delivery and the multi-physics involved: electromagnetic interference, thermal stability, and electrical noise

The rest of the paper is organized as follows. Section II presents the fundamental multiphysics analysis. Section III verifies the analysis by computationally evaluating two architecture test cases, VRM-on-board and IVR-on-package, using the augmented PEEC method [2]. Discussion of the results and conclusions follow in sections IV and V, respectively.

II. Multiphysics in power delivery architectures

System-scaling by heterogeneous integration of the power delivery architecture fundamentally calls for high-switching frequency and compact interconnects. The impact of compact interconnects on the electrical and thermal domains is presented in sections II-A and II-B, while the impact of high-switching frequency on the EMI is covered in section II-C.

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A. Electrical power delivery

Ideally, any power delivery architecture has to deliver stable voltage to the SoC, independent of the current drawn by the SoC. However, if the voltage is not stable, or it droops, the performance of the SoC or CPU is adversely affected [3]. So the voltage droop due to a current step pulse drawn by the SoC is a critical figure of merit for a power delivery network (PDN). The simple PDN representation, in Fig.1, allows us to analytically estimate [4] its 1st voltage droop, for the case of a small ESR_{die}, from eq. 1 below.

$$V_{droop} \approx I_{peak}\ Z_0 = I_{peak}\ \sqrt{\frac{L_{loop}}{C_{die}}} \tag{1}$$

where I_{peak} is the step current amplitude, Z_0 is characteristic impedance of the PDN, and $L_{loop} = L_{pkg} + L_{ESL}$. L_{pkg} is package inductance and L_{ESL} is ESL of the on-package decoupling (OPD) capacitor.

Since the integration of voltage regulator brings the power delivery circuits closer to the SoC, the package PDN interconnect is generally shorter in IVR than in VRM architecture. Since inductance is proportional to interconnect length, the package inductance, L_{pkg}, is lower for IVR than VRM. So, from eq. 1 above, considering the PDN interconnect alone, we can infer that the voltage droop is generally lower for an SoC powered by IVR than that of VRM.

$$V_{droop,IVR} \leq V_{droop,VRM} \tag{2}$$

B. Thermal management

The temperature of SoC is considered as the thermal figure-of-merit, since the junction temperature impacts both performance and reliability. For the VRM and the vertically stacked IVR architectures shown in Figs. 2a and 2b, the SoC die temperatures can be known from the eqs. 3 and 4 respectively. Notice that for the stacked IVR case, the power loss in IVR also contributes to the heat flux through the SoC.

$$T_{die,VRM} = P_{SoC}\ R_{th} + T_{ambient} \tag{3}$$

$$T_{die,IVR} = (P_{SoC} + P_{loss,IVR})\ R_{th} + T_{ambient} \tag{4}$$

where P_{SoC} is the thermal design power of the SoC, $P_{loss,IVR}$ is the power loss in IVR, $T_{ambient}$ is ambient temperature, and R_{th} is the thermal resistance seen by the SoC die to the ambient.

The power loss in an IVR majorly consists of switching and conduction losses, as given by eq. 5 below. The conduction loss is due to the I^2R loss in its power transistors and inductors. The electrical resistance is temperature-dependent. As Copper and GaN power transistors have positive temperature coefficients, the conduction loss increases with temperature.

$$P_{loss,IVR} = P_{sw} + P_{cond}(T_{sw}, T_{inductor}) \tag{5}$$

Since the power loss in an integrated voltage regulator, $P_{loss,IVR}$, is practically non-zero and positive, we can infer from the eqs. 3 and 4 above that the SoC die temperature is higher in an IVR-system than that of VRM-based, given the same thermal resistance and cooling solution applied to them.

$$T_{die,IVR} > T_{die,VRM} \tag{6}$$

C. Electromagnetic compatibility

Switching step-down voltage regulators that typically power high-performance processor CPU or SoC, draw pulsed currents from its input. Such current pulses, shown as I_{in} in Fig. 1, are of trapezoidal shape. Fourier analysis on this pulse waveform gives a frequency spectrum enveloped at two corner frequencies, with -20dB/decade and -40dB/decade roll-off respectively. The fundamental and the two corner frequencies are given by eqs. 7, 8, and 9 below:

$$f_o = F_{sw} \tag{7}$$

$$f_{c,1} = \frac{1}{\pi\tau} = \alpha\ F_{sw} \tag{8}$$

$$f_{c,2} = \frac{1}{\pi\tau_r} \tag{9}$$

where τ is pulse duration and τ_r is its rise time. α is the voltage conversion ratio, $\alpha = \frac{V_{in}}{V_{SoC}}$ and F_{sw} is the switching frequency of the voltage regulator.

Levels of conducted and radiated EMI from a switching voltage regulator depends on the frequency spectrum of its switching signals. Since IVR generally operate at a higher switching frequency and lower duty cycle than the multi-stage voltage regulators modules on board, its EMI envelope gets shifted to higher frequencies than VRM.

$$EMI_{f,IVR} \geq EMI_{f,VRM} \tag{10}$$

where EMI_f is the magnitude of EMI spectrum at a frequency, f.

D. Metrics for system-scaling and integration complexity

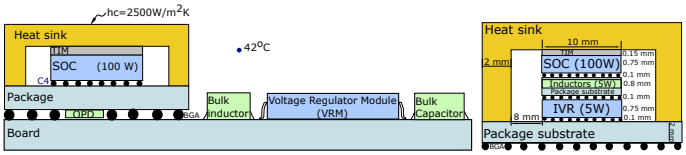
The above analysis shows that the system-scaling of a power delivery architecture fundamentally benefits electrical domain while worsening thermal and EMI. Substituting eq.5 in eq.4, a linear relation between the temperatures of SoC die, inductor, and switching power transistor can be seen. Since IVR co-locates these components, their thermal coupling can cause thermal runaway, so thermal management is critical. EMI, on the other hand, can be managed by an appropriate EMI filter or grounding the metal heat sink. So, the integration complexity can be measured by the thermal complexity, as given below.

$$\gamma_{Thermal} = \frac{q_{die,IVR}}{q_{die,VRM}} = \frac{q_{die,IVR}}{1W/mm^2} \tag{11}$$

where q_{die} is the heat flux density at the SoC die.

Similarly, a dimension-less metric can be defined as a measure for the system-scaling, based on the input voltage and switching frequency parameters of a voltage regulator as follows:

$$\gamma_{Scaling} = Log_{10}\left(\alpha\ \frac{F_{swIVR}}{F_{swVRM}}\right) \tag{12}$$



(a) (b)

Fig. 2. Power delivery architectures: (a) on-board discrete voltage regulator module (VRM) and (b) on-package integrated voltage regulator (IVR)

III. Results

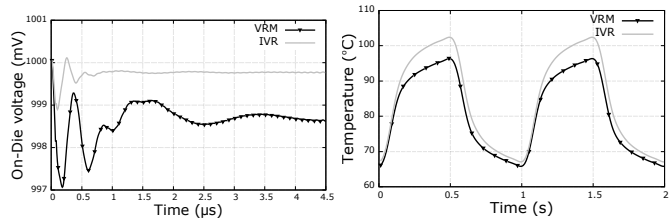
Two architectures, as shown in Fig. 2, are taken as test cases to verify the analysis of section II. They are 48V-to-1V switching voltage regulators, delivering 100A of current to the load, SoC. Considering their typical PDN, the respective droop results are extracted [2] for a 1A, 1ns rise time current pulse excitation. For thermal analysis [2], power cycling loading conditions of 1s period under boundary conditions, as shown in Figs. 2a and 2b, are applied. Differential-mode conducted EMI analysis [5] is performed, considering switching frequencies as 10MHz and 500KHz for the IVR and VRM respectively. Fig. 3 shows these results. Finally, integration complexity metrics of two commercial IVRs [6] [7] are compared against the cooling limits [8], as shown in Fig. 4.

IV. Discussion

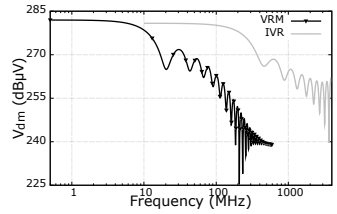
The results of Fig. 3 confirm the trends analyzed in section II. IVR's voltage droop is one-third of the VRM, 3 mV vs. 1 mV, as shown in Fig. 3a. So for electrical power delivery, IVR performs better than VRM due to its shorter interconnect. From the thermal perspective, the junction temperature in the IVR system is 6^oC higher than VRM, 102^oC vs. 96^oC, as seen in Fig 3b. Similarly, conducted EMI at high frequencies is worse for IVR compared to VRM, as shown in Fig. 3c. The conducted EMI-levels are high because of the low duty cycle of 2% needed for the 48V to 1V conversion. This duty cycle is small enough to draw sharp currents (due to the small width) from the input and generate high-frequency components. To reduce radiated EMI, the heat spreader or sink, as shown in Fig. 2, can be electrically grounded in the package. But grounding the heat sink can provide an additional thermal conduction path from SoC into the package. This can pose thermal problems for the embedded inductors in the package, adversely increasing their resistance, thereby reducing the IVR's electrical power efficiency. This example highlights the inter-dependence of the thermal, EMI, and electrical domains of an IVR-based power delivery architecture.

V. Conclusion

Integrated power delivery architecture is a multiphysics, multidimensional design optimization problem. Analysis in this paper shows the interdependence of the domains. System-scaling optimizes electrical power delivery but complicates thermal and EMI due to its dense functional integration and high switching frequency. Optimizing for EMI, on the other hand, can compromise the thermal integrity of the embedded passives. Also, a positive correlation exists between thermal complexity and system-scaling metrics. So holistic design approach is needed for an IVR-based power delivery architecture.



(a) (b)



(c)

Fig. 3. Multiphysics evaluation of power delivery architectures: discrete on-board VRM vs. integrated on-package IVR (a) voltage noise at SoC, (b) the temperature of SoC, and (c) conducted EMI differential mode noise at the input of the voltage regulator.

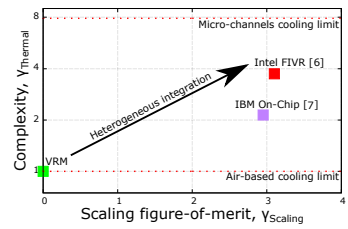


Fig. 4. Design space exploration of power delivery architectures, showing the impact of heterogeneous integration on performance and design complexity

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