Thermal Management of Glass Panel Embedded Packages: Package Architecture vs. Power Density

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***Abstract*—This paper presents a first analysis of the thermal management and performance of glass panel embedded (GPE) packages, a novel fan-out packaging technology recently demonstrated for heterogenous integration, beyond the capabilities of emerging wafer level fan-out (WLFO) packages. In this package architecture, a glass substrate carrier is used, onto which cavity-embedded devices are attached. The active sides of these devices are exposed to enable formation of high-density multi-layered redistribution layer (RDL) wiring and direct board attach of the embedded package, providing two separate paths for heat dissipation – through the board and through the backside glass carrier. There are concerns on the ability of such a package architecture with glass materials notoriously considered as thermal insulators to handle high heat flux densities. To address this challenge and better understand the thermal performance of GPE packages, a parametric modeling study was carried out in ANSYS, considering a 10mm × 10mm logic chip embedded in a glass substrate. In summary, this paper establishes the thermal management and cooling strategy of innovative GPE packages with innovations in package architectures and simple solutions to enable direct chip cooling with integrated heat spreaders so as to handle the high heat fluxes associated with future electronics.**

Keywords—High Density Fan-out, Panel Fan-out, Glass Panel Embedding, Heterogeneous Integration

A. Motivation

Since the advent of this technological age, the desire for more robust and powerful computing has driven the race for increasing device density and miniaturization – arising from new and improving materials, tools, processes, and design methodologies. As a result, electronic devices and their applications have been among the fastest advancing fields, reflected by the ever-shrinking dimensions of devices from the microscale down into the nanoscale within the past few decades [1]. Many of these devices are currently operating with critical dimensions in the range of 7 - 14 nm, with minimum feature sizes of 5 nm targeted for next-generation technology nodes. At the same time, new approaches at die and package integration levels such as embedding and stacking are emerging as potential means of increasing performance without relying on reduced feature scaling alone [1]. Fig 1. outlines the evolution of some exemplary packaging architectures as they incorporate increasing levels of integration [2]. However, these technological advancements are also creating new thermal challenges that can ultimately limit their effectiveness and implementation.

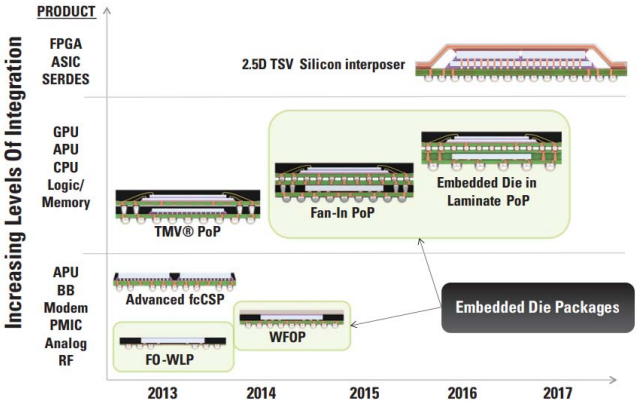

Fig. 1. Evolution of Packaging Architectures

Through the miniaturization and densification of transistors and other integrated circuit devices, it has been possible to improve performance but at the cost of increasing power dissipation. For instance, in high performance computing applications, some modern processor modules can reach upwards of 100 W/cm^2. Even in more consumer-oriented applications such as laptops and smartphones, these modules can reach around 10 W/cm^2 [3]. As this trend continues towards smaller sizes – through higher device densities and more heterogeneous integration – this power problem becomes even more pronounced. Thermal management is an important element to electronic packaging, in that device performance is significantly influenced by its temperature. Without optimal thermal management, device lifetime can be decreased drastically due to thermomechanical stresses that are very detrimental to longevity and reliability. Therefore, there is a need for novelty in packaging architectures that can address the requirements of increasingly power-dense devices.

B. Concept

The concept of glass panel embedded (GPE) packaging was recently designed and demonstrated as a promising candidate architecture for advanced high-density, heterogeneous integration [4].

With its many outstanding properties and superior performance, glass is one of the prime materials for wafer-level fan-out (WLFO) packaging technologies. It is a common practice to employ epoxy mold compounds (EMCs) as the fan-out substrate in WLFO packages. However, such WLFO

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packages suffer from limitations in scalability due to its inherent material characteristics – cure shrinkage, excessive surface roughness, and poor signal integrity [4]. In comparison, the smooth surface and high-dimensional stability of glass enable high-density redistribution layers (RDL) even on large panels. Furthermore, the coefficient of thermal expansion (CTE) of glass can be tailored to more closely match that of the devices or other packaging materials, thereby improving thermomechanical reliability and enabling direct mounting onto boards. Glass also possess lower dielectric losses compared with most epoxy mold compounds, as well as high electrical resistivity and excellent moisture resistance [4].

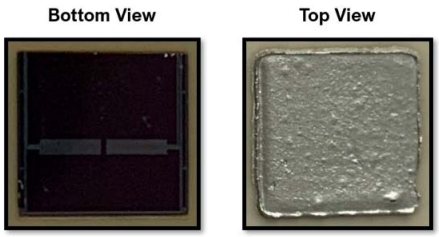

Fig. 2. Overview of Embedded Devices

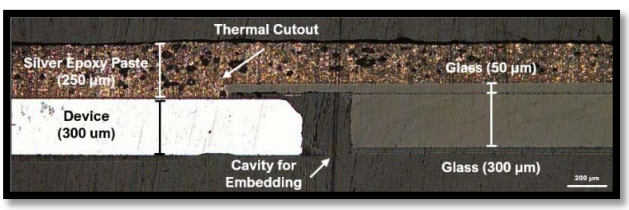

Fig. 3. Cross-Section of Glass Panel Embedded Package

In a new demonstration of glass panel embedded packages, test vehicles were fabricated as seen Fig. 2 and 3. This architecture features devices embedded within cavities of glass substrates, with both sides of devices exposed to enable formation of high-density multi-layered wiring and integrated heat spreaders. From the bottom view of the embedded devices in Fig. 2, the active side is emphasized to highlight its exposed pads for wiring and routing directly to the board. Such an architecture achieves ultrashort interconnects for minimization of parasitics. By this direct mounting onto boards, it is possible to achieve more miniaturization while ensuring superior electrical performance [4]. From the top view of the embedded devices in Fig. 2, the focus is the integrated heat spreader formed from silver epoxy paste. These various layers in the stackup are demarcated in the cross-sectional view of Fig 3. There are two primary pathways for heat dissipation – through the board and through the backside thermal cutout. However, these limited thermal pathways raise concerns on the capabilities of such a package architecture to handle high power densities, especially with the thermally insulative nature of glass.

C. *Process Flow*

The process flow for the fabrication of glass panel embedded packages is outlined in Fig. 4. This process begins with the lamination of through-cavity glass to bare glass to form blind-cavities. By laminating a bare glass panel onto a glass panel with

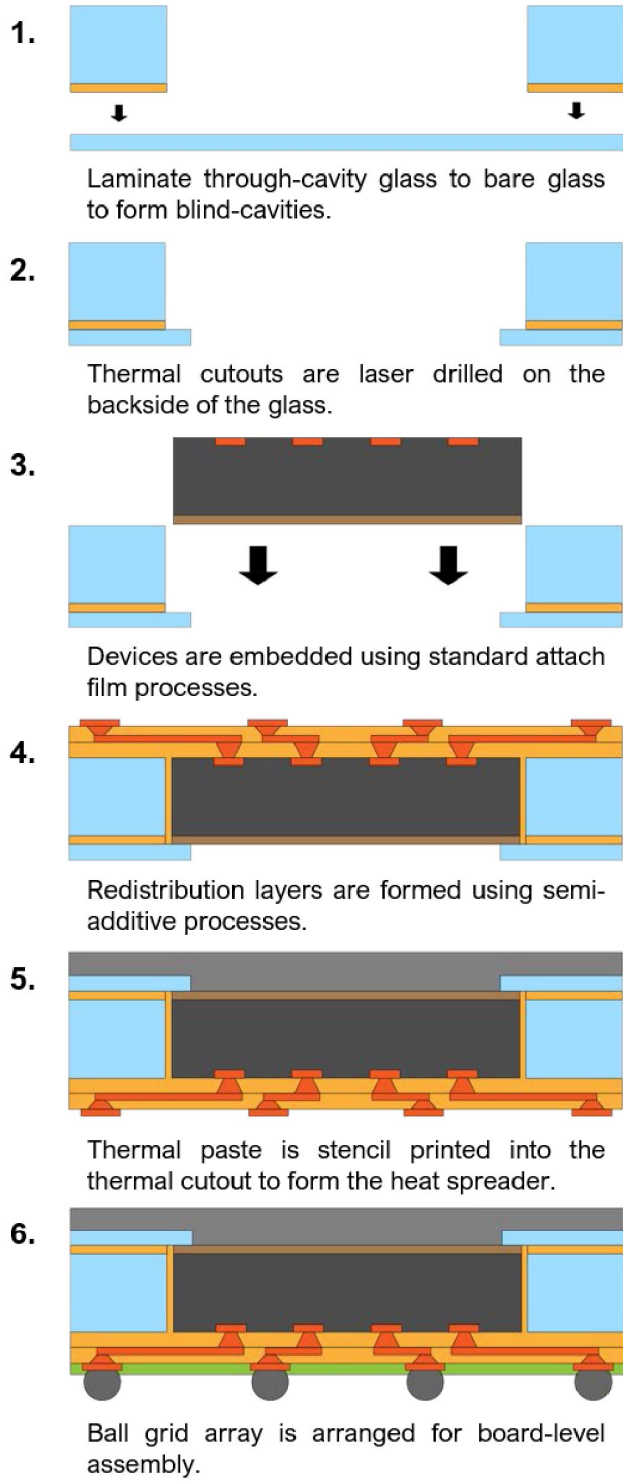

Fig. 4. Process Flow for Glass Panel Embedded Package

through cutouts using an adhesive polymer, cavities are created for device embedding. Devices are embedded using a precision pick-and-place tool system with standard attach film processes. Thermal cutouts are drilled onto the backside of the glass using

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a femtosecond laser. These cutouts can be adjusted and tailored for different heat spreader sizes, providing variable coverage of the backside area. Redistribution layers are formed using standard semi-additive processes including electroless deposition of seed layers, photolithography, electrolytic plating. These processes are followed by stencil printing of silver epoxy paste to form the integrated heat spreader, although this thermal material can be varied for performance and reliability. For board-level assembly, a ball grid array is arranged.

II. Results

A. Finite Element Analysis

Panel embedded packages provides a unique solution to advanced high-density, heterogeneous integration. However, such packages suffer from limited thermal pathways. This problem becomes even more pronounced in integrating devices with high power densities. Therefore, finite element analysis serves as a tool to better understand the thermal behavior of such packages for new insights into their design and optimization for more reliable and robust performance.

In order to better understand the behavior of glass panel embedded packages, and to ultimately address the thermal challenges of such packages, a parametric modeling study was carried out in ANSYS. The focus of this study was a 10 mm × 10 mm logic chip surrounded by a 100 µm cavity and embedded in a 13.4 mm × 13.4 mm glass substrate, with the standard geometric and material parameters outlined in Table I and II. It was analyzed in steady-state conditions, as representative of the worst thermal scenarios of constant power output.

TABLE I. Parameters for Glass Panel Embedded Package

Device			Core			Redistribution Layer	Backside	Heat Spreader		
[mm]			[mm]			[µm]	[µm]	[µm]	[W/mK]	[W/m^{2}K]
x	y	z	x	y	z	z	z	z	k	h
10	10	0.1	13.4	13.4	0.1	50	50	50	400	5

TABLE II. Thermal Conductivities of Packaging Materials

Material		Thermal Conductivity	
Layer	**Material**	k_{xy} [W/mK]	k_z [W/mK]
Device	Silicon	148	148
Cavity	Dielectric	0.15	0.15
Core	Glass	1.1	1.1
Redistribution Layer	Copper in Dielectric	25.2	0.29
Backside	Glass	1.1	1.1
Heat Spreader	Copper	400	400

Two different architectural approaches to glass panel embedded packages were explored – closed and open backsides. A comparison of these architectures, or configurations, and their respective stackups is illustrated in Fig. 5.

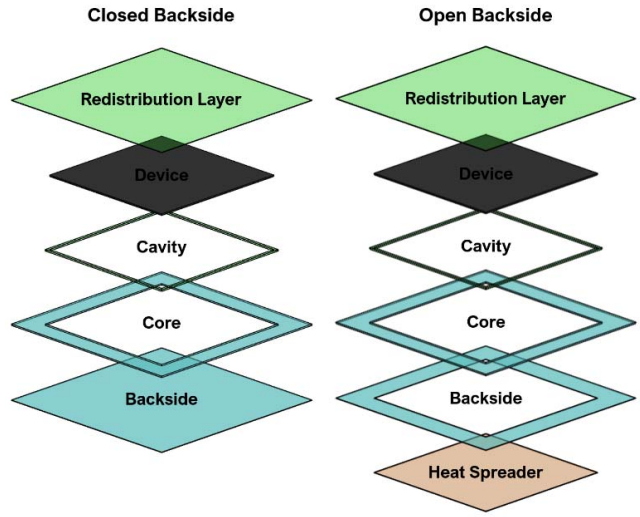

Fig. 5. Comparison of Configurations for Glass Panel Embedded Package

For the closed backside configuration, the backside of the device remains fully enclosed by the glass substrate as represented by the schematic in Fig. 6. Therefore, this thermal pathway through the backside of the device must travel through glass.

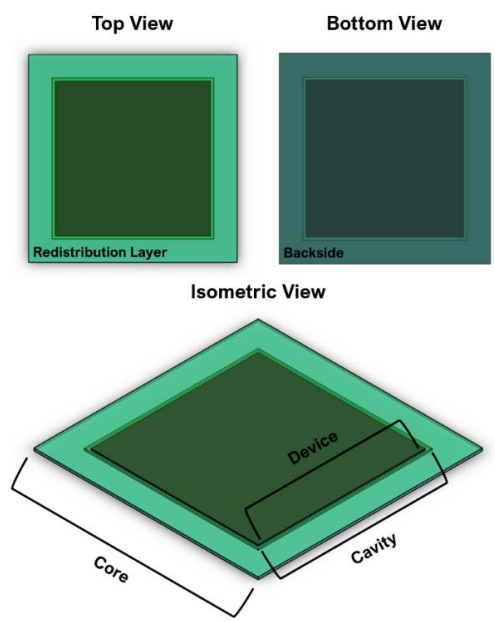

Fig. 6. Schematic of Closed Backside Configuration

For the open backside configuration, the backside of the device is opened by thermal cutouts such that heat spreaders be

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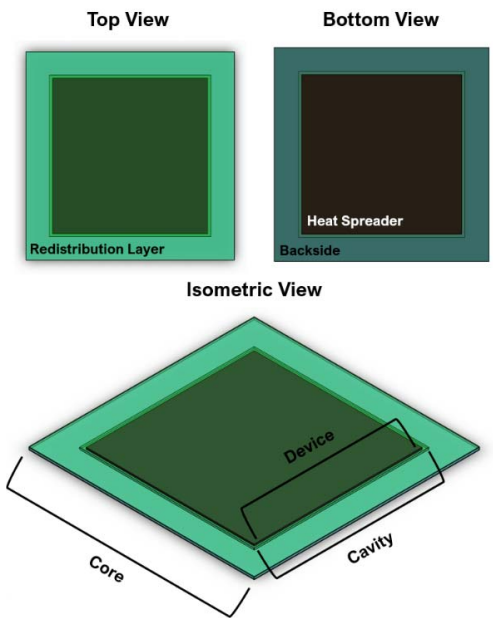

Fig. 7. Schematic of Open Backside Configuration

integrated directly onto the device as represented by the schematic in Fig. 7. It has the advantage of a more conductive material as a thermal pathway, although it introduces new challenges from fabrication, performance, and reliability standpoints.

Many different parameters were considered in this parametric modeling study to craft a comprehensive view of their effects. Geometric parameters were varied such as the thickness of the backside glass substrate (10 – 500 µm) for the closed backside configuration and the thickness of the heat spreader (10 – 500 µm) for the open backside configuration. Material parameters were also varied such as the thermal conductivity of the heat spreader (1 – 1,000 W/mK) in the open backside configuration. Different thermal management solutions were also considered for backside cooling in both configurations, through the glass substrate or heat spreader (1 – 10,000 W/m^{2}K). It ranged from passive air cooling at 10 W/m^{2}K, forced air cooling at 100W/m^{2}K, up to more advanced liquid cooling above 1,000 W/m^{2}K.

For the thermal model, the active side of the embedded device was implemented as a surface heat source with varying wattage. Through this variation in wattage, it is possible to represent a range of power densities from different devices and their applications for glass embedded packages. Fig 8. highlights

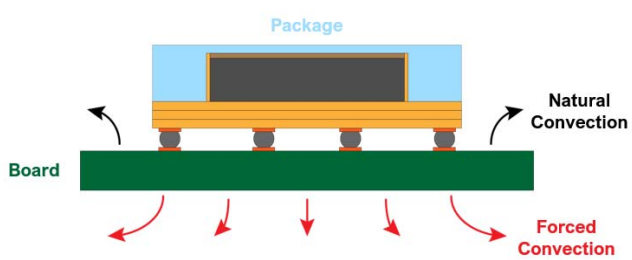

Fig. 8. Boundary Conditions for Thermal Model

the essential boundary conditions for the thermal model inclusive of the entire assembly – package and board. It is important to consider all the possible thermal pathways, both through the package and board. For computational efficiency in a more compact thermal model, the contributions from the board and the attaching solder balls can be simplified and represented as an effective heat transfer coefficient [5]. Fig. 9 illustrates this simplified, compact model with an effective heat transfer coefficient of 1,000 W/m^{2}K to represent the various thermal pathways from typical convections in a board.

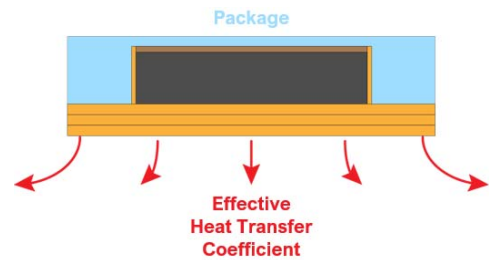

Fig. 9. Simplification of Thermal Model

B. *Thermal Modeling*

Both closed and open backside configurations of glass embedded packages were subjected to a parametric modeling study to determine their respective cutoff points in power density to reach a critical temperature of 100°C in the device. For a direct comparison, the same geometric and material parameters were applied in both configurations as outlined in Tables I and II.

As summarized in Fig. 10, the open backside configuration is much more effective at thermal management in that it is able to remain at operational temperatures with higher power densities due to the integrated heat spreader. Even with simple solutions such as passive (10 W/m^{2}K) or forced air cooling (100 W/m^{2}K), the package is able to dissipate 10.3 up to 19.7 W/cm^2. With more advanced solutions such as liquid cooling (1,000 – 10,000 W/m^{2}K), the package is able to dissipate 33.6 up to 70.3 W/m^{2}K. For comparison, the closed backside configuration dissipates 7.0 W/cm^2 (10 W/m^{2}K), 8.2 W/cm^2 (100 W/m^{2}K), 13.3 W/cm^2 (1,000 W/m^{2}K) and 34.8 W/cm^2 (10,000 W/m^{2}K) for the different levels of thermal management solutions.

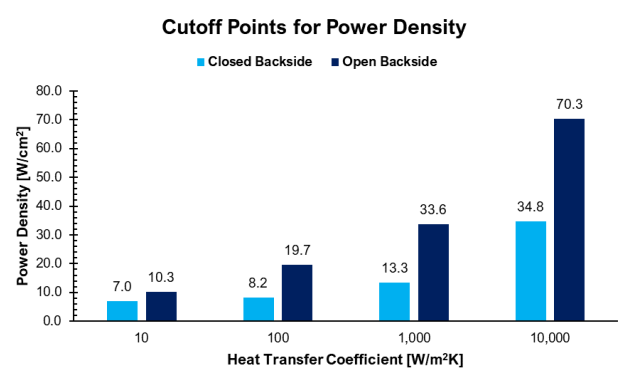

Fig. 10. Cutoff Points for Power Density

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Examples of temperature distributions for the closed and open backside configurations of glass embedded packages are seen in Fig. 11 and 12. There is a clear disparity in the power dissipations of the different configurations. For the closed backside configuration, there is a minimal power dissipation on the device, as demonstrated by the large thermal concentration at the center in Fig. 11. For the open backside configuration, there is a more uniform, gradual temperature gradient in Fig. 12. It can therefore be understood that the integrated heat spreader contributes towards more effective thermal management, with lower package temperatures as well.

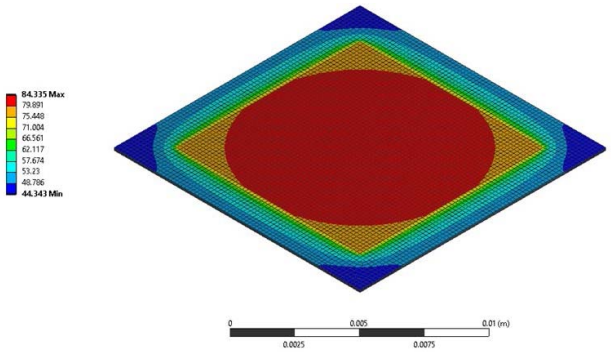

Fig. 11. Temperature Distribution for Closed Backside Configuration

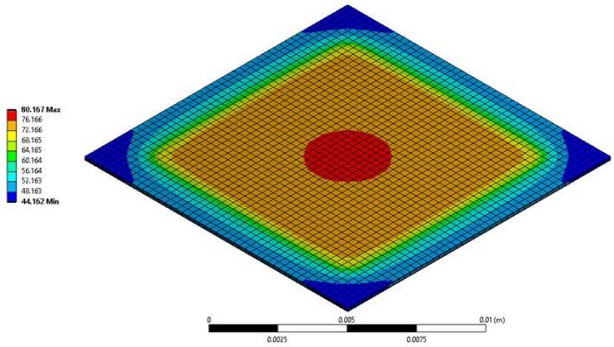

Fig. 12. Temperature Distribution for Open Backside Configuration

Although the thermally insulative nature of glass can seem detrimental to the overall thermal management of the package, its properties can be leveraged for thermal decoupling between multiple devices as demonstrated through Fig. 13. Temperature difference refers to the temperature difference between the device and its surrounding substrate, representing the extent of lateral heat spreading within the package. Therefore, it can be interpreted that the higher the percentage in temperature difference, the more effective the thermal decoupling between multiple devices in a lateral plane.

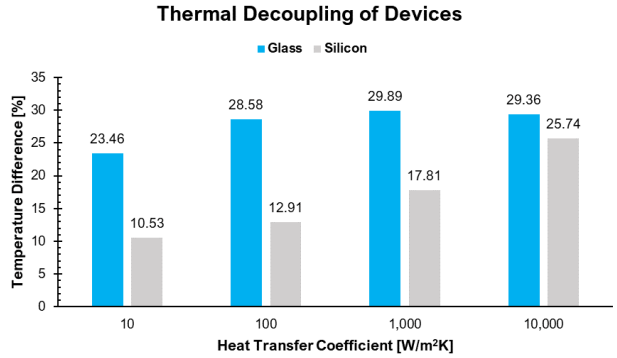

Fig. 13. Thermal Decoupling of Devices

From the parametric modeling study, response surfaces were generated to explore the relationships between the different parameters as seen in Fig. 14 and 15. It is insightful to compare

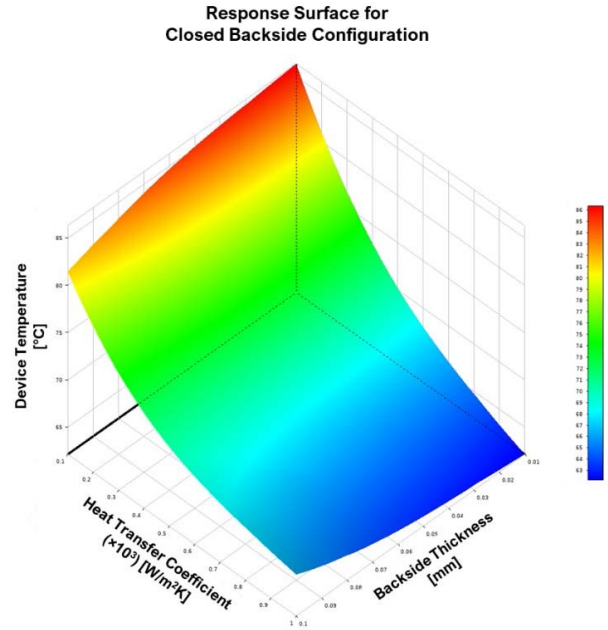

Fig. 14. Response Surface for Closed Backside Configuration

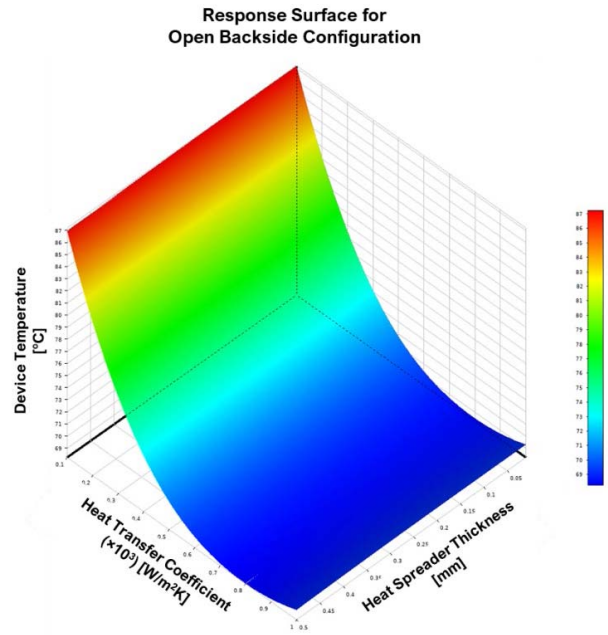

Fig. 15. Response Surface for Open Backside Configuration

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the response of parameters such as geometry and cooling in that their relative importance can be evaluated. For instance, it is demonstrated in both Fig. 14 and 15 that the particular thermal management solution for backside cooling has the greatest effect on device temperatures. Device temperature varies more as a function of heat transfer coefficient than as a function of backside thickness. Other trends for minimizing device temperatures include thinner backside thickness for lower thermal resistance, thicker heat spreader thickness for more effective heat spreading, and higher heat transfer coefficients. For the response surface of Fig. 16, it focuses specifically on the geometric and material parameters of the heat spreader in the open backside configuration. It is demonstrated that the heat spreader thermal conductivity has the greatest effect on device temperatures, over that of heat spreader thickness. Device temperature varies more as a function of heat spreader thermal conductivity than heat spreader thickness. Therefore, it emphasizes the importance of material development and innovation towards higher thermal conductivities.

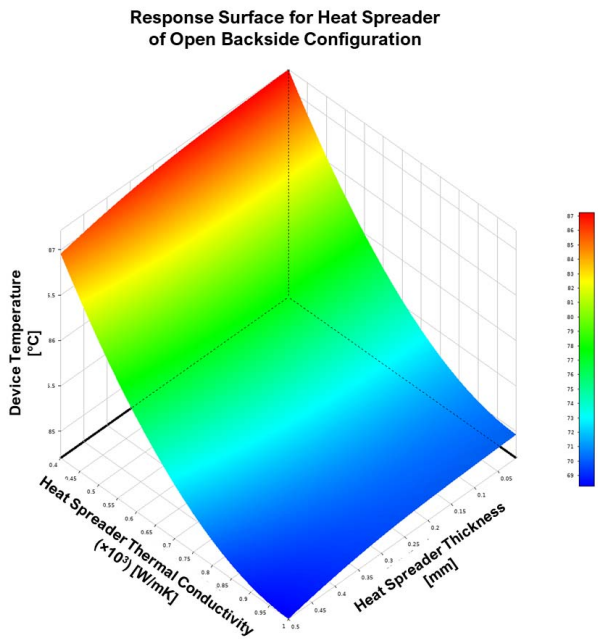

Fig. 16. Response Surface for Heat Spreader of Open Backside Configuration

III. Discussion

A. Comparison of Packaging Architectures

In comparison of the different architectural approaches, or configurations, to glass embedded packages, it was demonstrated that the open backside configuration has higher capabilities for thermal management. Although the closed backside configuration was viable at power densities up to 7.0 W/cm^2 with passive air cooling, it begins to exceed recommended operational temperatures of 100°C for most logic chips. Even with more advanced liquid cooling, the closed backside configuration was limited to maximum, operational power densities of 34.8 W/cm^2. Therefore, there is a need for further innovation in glass embedded packages to overcome their thermal limitations. A promising approach was explored in the form of integrated heat spreaders for more direct thermal management, by exposing the backside of devices for further scalability in power. In this new architecture, a heat spreader made of a high thermal conductivity material such as copper is envisioned as directly deposited onto the exposed backside of the device to minimize thermal contact resistance. Even with simple thermal management solutions such as passive air cooling, power densities are sustainable up to 10.3 W/cm^2 with a heat spreader thickness of 50 µm. With more advanced solutions such as liquid cooling, it is possible to achieve even more pronounced improvements, and raise the power densities up to 70.3 W/cm^2 within the operational temperature range of 100°C.

For applications in advanced high-frequency, wide-bandgap devices such as gallium nitride (GaN) and gallium arsenide (GaAs) with higher operational temperatures, power densities can be pushed further as these integrated heat spreaders exhibit the largest improvements in scalability at higher power densities and temperatures.

Another advantage of this innovative architecture yields in the thermal decoupling between multiple embedded devices within packages. Due to the low thermal conductivity of glass, temperature-sensitive devices such as memory stacks can be easily thermally isolated and decoupled from heat-generating devices while minimizing the spacing necessary for optimal electrical performance. For instance, glass facilitates lower substrate temperatures by around 20% as compared to silicon, and this innovative package architecture with integrated heat spreader allows for efficient directional heat transfer.

B. Design Optimization of Embedded Packages

From the parametric modeling study of the different architectures for glass embedded packages, a set of design guidelines can be established for thermal management. For the closed backside configuration, thinner backsides are recommended for lower thermal resistances. For the open backside configuration, thicker heat spreaders recommended for more effective heat spreading and lower temperature gradients. In both configurations, device temperature varied more as a function of heat transfer coefficient than as a function of backside or heat spreader thicknesses. Therefore, it is important to optimize the package for its interface with thermal management solutions in backside cooling. For the integrated heat spreader, thermal conductivity has a greater impact than thickness. Device temperature varies more as a function of heat spreader thermal conductivity than heat spreader thickness. Therefore, it is important to pursue material development and innovation for advancements in thermal management.

For future studies, it is crucial to consider the thermomechanical behavior of glass embedded packages and the effects of these parameters. Especially with the integration of heat spreaders, there are challenges for design and optimization from fabrication, performance, and reliability standpoints.

IV. Summary

In summary, this paper establishes the thermal management and cooling strategy for novel glass embedded packages through innovative package architectures to enable direct device cooling

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with integrated heat spreaders so as to handle the high heat fluxes associated with future electronics.

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