Design and Demonstration of Single and Coupled Embedded Toroidal Inductors for 48V to 1V Integrated Voltage Regulators

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***Abstract*—High-efficiency High-Voltage Integrated Voltage Regulators (HV-IVR) will allow the next generation of data centers and servers to operate with higher efficiency while delivering more computing power. High-density embedded inductors operating at frequencies over 10 MHz allows the miniaturization of power modules enabling their integration closer to the SoC. However, single stage 48V to 1V IVR present new challenges that are not seen in low voltage converter such as 3.3V or 1.7V to 1V. In this work, a novel expandable interleaved toroidal inductor cell with vias-in-slot thru magnetic sheet is presented. In addition, we present a new metric for magnetic material and inductor technologies to describe their efficiency under different duty cycle conditions. Using the analysis of two available magnetic sheets with permeability 50 and 150 at 10MHz, we present the magnetic properties of a magnetic sheet to obtain 95% of inductor efficiency, an inductance density of 113 nH/mm^3 at 10 MHz, a saturation current over 2.5A, and DC resistance around 20 mΩ. These inductor requirements are given by the possible power stage topologies that can be used to achieve 48V to 1V, where some of them use single inductor while others use coupled or tapped inductors. The efficiency conditions for the inductor presented in this work must be matched by the power stage topology, leading to a co-design between power inductor and the power stage topology. In this work we present why the duty cycle must be extended by a factor of 4 in order to obtain a 95% efficiency in the inductor. We provide a process for the fabrication of these inductors. Finally, a test inductor is fabricated that shows an inductance density of 77 nH/mm^3 and correlates well with the simulation model. This allows to predict with good accuracy the inductor performance with the proposed inductor design and magnetic sheet properties.**

I. Introduction

Traditional architectures for power delivery networks in servers and data centers require several down conversion stages to convert the AC grid voltage, ranging from 85V to 265V, to 1V required by systems on chip (SoC) and processors (CPU). This includes stages of power factor correction that convert the grid voltage to 400 V_{DC}, a buck converter from 400 V_{DC} to 48V, and then several stages to convert from 48V to 1V [1]. This last power delivery system - from 48V to 1V - has several points that contribute to losses, decreasing drastically the overall efficiency of the power supply chain. The losses can be reduced if a single stage integrated voltage regulator (IVR) from 48V to 1V or 12V to 1V are integrated in the SoC package, as shown in Figure 1.

We can identify three main power distribution system configurations: a) a multi-stage down conversion network with onboard 48/12V and 12/1.7V voltage regulators and a 1.7/1.0V IVR, b) a two-stage down conversion with onboard 48/12V voltage regulator and a 12/1.0V IVR, and c) a single-stage 48/1.0V IVR.

With the reported efficiencies in [2], [3], the configuration (a) can show a system efficiency of 81%, but it can be reduced to 75% due to PDN losses. For configuration (b) the system efficiency could be greater than 87.3%, but again due to PDN losses the efficiency can decrease to 87.1%. For the configuration (c) the efficiency could be 90%.

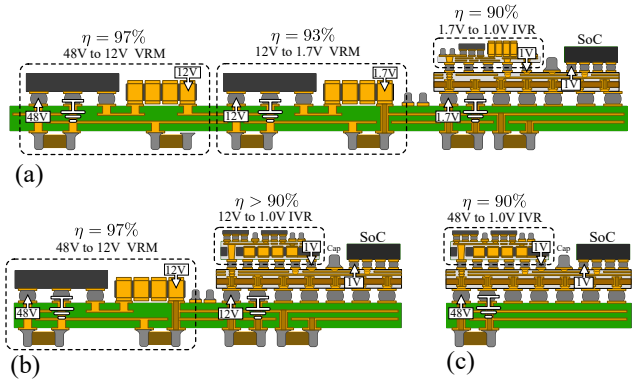

Figure 1: Different power distribution networks. (a) Multi-stage 48V-12V-1.7V with 1.7V-1.0V IVR down conversion, (b) Two-state 48V-12V with 12V-1.0V IVR down converter, (b) single-stage 48V-1.0V IVR.

The use of IVRs can improve the system efficiency and, as they use switching frequencies in the range of 10 MHz to 100 MHz, the converter has higher bandwidth allowing a faster transient response [4].

However, for IVRs it is challenging to fabricate ultra high-performance inductors where, for example, chip inductors tend to have very high DC resistance greater than 100 mΩ and low inductance in the range of 10 nH [5], [6]. Other proposed surface inductors for IVR show very low DC resistance of less than 20 mΩ with inductance greater than 20 nH and high saturation current greater than 8A, but they occupy a large lateral area greater than 12 mm^2 [6], which reduces the integration and current density. Three air core package inductors are shown in [7] with inductance densities (at 140 MHz) of 1.4 nH/mm^3, 3.0 nH/mm^3, and 6.4 nH/mm^3 with DC resistance of 7.1 mΩ, 12 mΩ, and 36 mΩ, respectively. These technologies make it difficult to scale up the inductance while keeping a DC resistance around 10 mΩ. This suggests that chip inductors are not suitable for high power density and that air core inductors do not provide enough inductance while keeping an ultra low DC resistance.

To increase the integration and power density of an IVR, it is then required to use substrate embedded inductors with magnetic core and with closed magnetic path as shown in Figure 2. Open loop inductors, such as solenoids, can lose both inductance and

Q factor by more than 35% when they are embedded and placed between conduction planes. On the other hand, closed magnetic path inductors, such as toroids, only lose 4% of inductance. Toroidal inductors also show higher inductance density, lower DC resistance, but with a penalty in the saturation current [8].

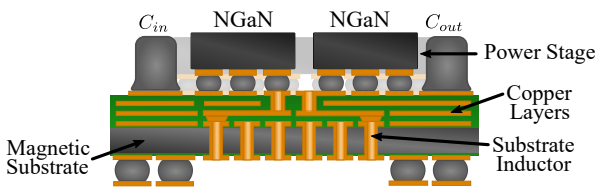

Figure 2: IVR Dielet stack-up.

II. Review of Power Stage Topologies

As shown in [8], [9], the main source of active losses is produced by the output capacitance (between source and drain) and by the gate charge (charge required to turn the device on/off) of the transistors. Even when GaN MOSFETs are used, the active losses are still too high for 48V to 1V at 10 MHz and above.

A series capacitor power stage topology [10] uses switched capacitors with inductors to reduce the voltage stress over the MOSFETs, but still at 10 MHz the system efficiency is around 72% and limited to less than 81% at lower frequencies (due to high current ripple) [9]. The topology presented in [11] combines a series capacitor along with tapped or coupled inductors to build a resonant tank between the capacitor and leakage inductance of the tapped inductor, so the MOSFET can be soft switched, reducing their losses. Another hybrid topology [12] combines the series capacitor [10] with the tapped inductor [11] to further provide an ultra-high conversion ratio.

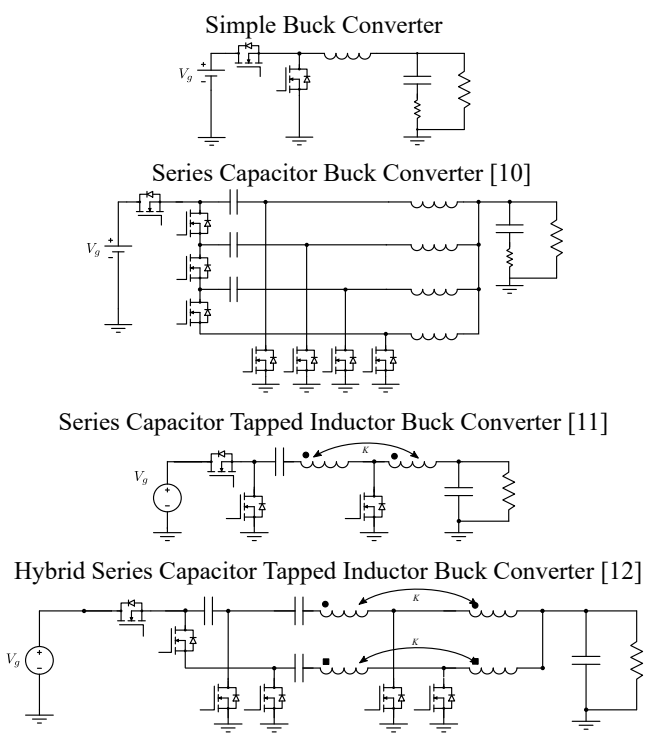

Figure 3: Review of Power Stage Topologies.

The basic principle of the series capacitor [10] topology is to use the capacitors as storage elements to reduce the potential energy (voltage) and supply each phase with a lower voltage. In the hybrid series capacitor with tapped inductors [12], the capacitors reduce the potential energy (voltage) to half and the coupled inductor reduces the kinetic energy (current) to half or less. As a result, all these structures require a duty cycle extension (in order to supply the required power demanded by the load) and provide a reduction of the active losses. But only the topologies that use coupled inductors can achieve soft switching eliminating the output capacitance losses.

For the next analysis, the inductance requirements are expressed as the total inductance L in a simple or series capacitor buck converter, which is also equivalent to the magnetizing inductance $L_{ms} = L$ referred to the secondary of a coupled or tapped inductor for the hybrid topologies. In the last case, the total inductance would be $L_{total} = L_{ms}\left(\frac{n_p+n_s}{n_s}\right)^2$ where n_p and n_s are the number of turns ratio of the primary and the secondary, respectively. If $n_p/n_s = 1$, then $L_{total} = 4L_{ms} = 4L$.

III. Target Inductor Requirements

In a buck DC to DC converter, the inductor goes through stages of energizing and draining. When the inductor is energized, its current increases as it stores energy. When it is drained, its current decreases as it releases energy. This process in the inductor leads to the build-up of a DC current equal to the current consumed by the load, plus an AC current ripple as result of the storage/release of energy. The typical current waveform is shown in Figure 4,

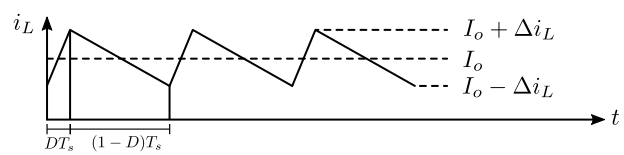

Figure 4: Inductor current waveform.

where I_o is the output load current, Δi_L is the current ripple and is given by (1), D is the energizing duty cycle, and $T_s = 1/f_s$ is the switching period.

$$\Delta i_L = \frac{V}{2L}(1-D)T_s \tag{1}$$

We can express the inductor losses due to the DC and AC current as given by equation (2), where $R_{acx}(D, f_s)$ corresponds to the effective AC resistance per inductance with dimension Ω/nH and is a function of the duty cycle and frequency, R_{DC} is the inductor DC resistance, and $L(f_s)$ is the inductance at the switching frequency.

$$P_L = I_o^2 R_{DC} + \Delta i_L^2\, L(f_s)\, R_{acx}(D, f_s) \tag{2}$$

We can determine the minimum requirement that an inductor needs to meet in order to have a $\eta = 95\%$ of efficiency. In this analysis, we consider a DC/DC converter with $I_o = 2.5$A of output current, output voltage $V = 1$V, and frequency $f_s = 10$ MHz. This means the inductor losses would be,

$$P_{loss} = I_o\, V\left(\frac{1}{\eta} - 1\right) = 131.6\,\text{mW} \tag{3}$$

Expression (2) can be rewritten as follows by replacing the current ripple expression,

$$P_L = I_o^2 R_{DC} + \frac{V^2}{4Lf_s^2}(1-D)^2\, R_{acx} = 131.6\,\text{mW} \tag{4}$$

Keeping the DC loss to be equal to the AC loss, and if $R_{DC} \approx 10\,\mathrm{m}\Omega$, the AC loss should be $P_{L,AC} = 69.1$ mW, we obtain the next condition

$$\frac{(1-D)^2}{4Lf_s^2} R_{acx} = 69.1\,\mathrm{mW} \tag{5}$$

The two inductor parameters from the previous expression are L and R_{acx}. The duty cycle D is set by the application conversion ratio and is fixed, and we can set the parameter $f_s = 10$ MHz as a design choice. This leads to the next relation between R_{acx} and L,

$$\frac{R_{acx}}{L} = 0.0691 \frac{4f_s^2}{(1-D)^2} = M(kD, f_s) \left[\frac{\Omega}{\mathrm{H}}\right] \tag{6}$$

so the inductance L and the resistance per unit inductance R_{acx} are related by the constant $M > 0$ by the following expresion,

$$R_{acx} = M(D, f_s)\, L \tag{7}$$

In Figure 5 different values of R_{acx} and Δi_L are plotted versus the inductance L for the conversion ratios of $D = k/48$, with value of $k = 1, 2, 4$. The parameter k corresponds to the duty cycle extension provided by the converter.

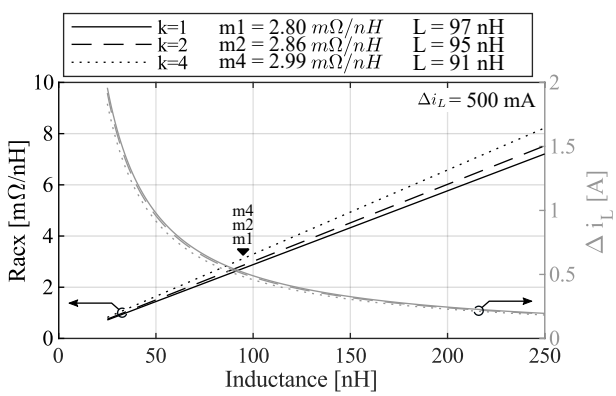

Figure 5: R_{acx} for $D = k/48$ and $k = \{1, 2, 4\}$.

We observe that if a duty cycle extension by a factor of 4 is provided, with an inductance of 91 nH at 10 MHz the current ripple would be 500 mA and the effective AC resistance must be less than 3 mΩ/nH. The same analysis shows that for a conversion ratio from 1.7V to 1V at 50MHz the required inductance is $L = 8$ nH and effective AC resistance is $R_{acx} = 32.6$ mΩ/nH. This shows the difficulty in achieving 48V to 1V compared to low voltage converters. With the converter delivering 2.5A of current we should allow the inductor to have a saturation current of 3.5A. These numbers set the requirement of a total inductance $L = 91$ nH in a single inductor configuration or the magnetizing inductance in the secondary of a tapped inductor. If the tapped inductor has the same number of turn in both sides, then the total inductance in this topology should be $L = 364$ nH.

IV. Magnetic Materials

Two low frequency magnetic sheet materials were analyzed: Panasonic HPE1 and Kemet RM4A. Figures 6 and 7 show the reference and measured permeability of these materials.

Figures 8 and 9 shows the measured quasi-static M-H curve, where M and H are related by $B = \mu_0(H+M) = \mu_0(1+\chi_{m0})H$.

From Figure 8 we see that the HPE1 material starts to saturate at a magnetic field of H = 4.5 kA/m and from Figure 9 we obtain

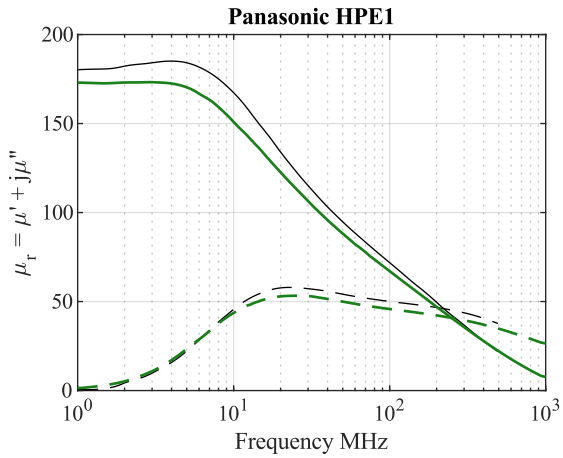

Figure 6: Permeability of Panasonic HPE1, reference (black) and measured (green).

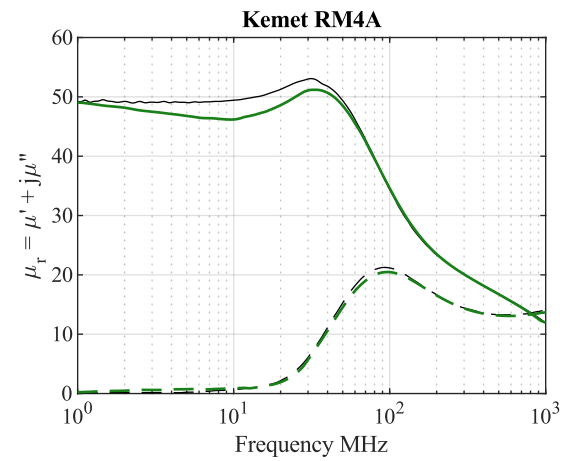

Figure 7: Permeability of Kemet RM4A, reference (black) and measured (green).

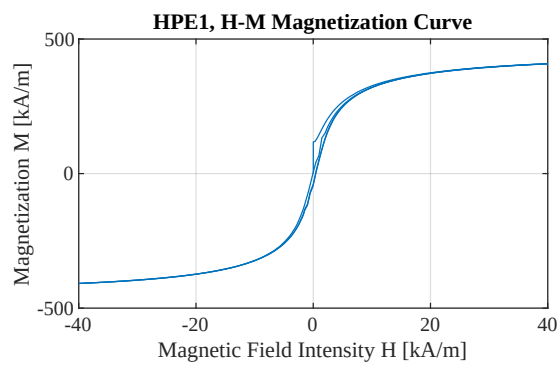

Figure 8: M-H curve of Panasonic HPE1.

that material RM4A starts to saturate at H = 20 kA/m. We see that HPE1 is almost hysteresis-less and RM4A has a much larger B-H hysteresis window. But with a current ripple of 500mA, the H field span is less than 1.5kA/m which still produces very low core losses in both materials.

V. Inductor Design

As shown in [8], for an inductor to be effectively embedded in a package, it needs to have a closed magnetic path which means that all the magnetic field must go through the magnetic material and not air. If the inductor does not meet this requirement, like

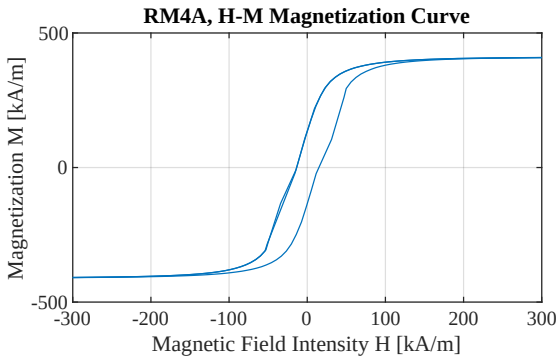

Figure 9: M-H curve of Kemet RM4A.

a solenoid, it can lose more than 35% of its inductance and quality factor. Figure 10 shows the basic cell of a novel inductor structure [13] where the magnetic field is produced by the vias and is shaped to look like an elongated toroidal inductor.

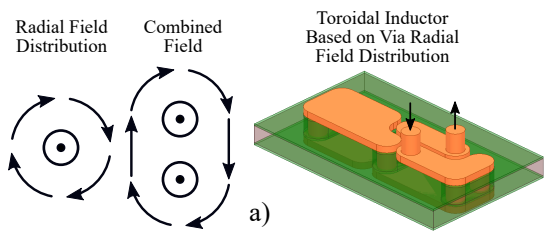

Figure 10: Basic toroidal inductor cell.

This construction cell can be used to create larger inductors that increase the self and mutual inductance, as shown in Figure 11.

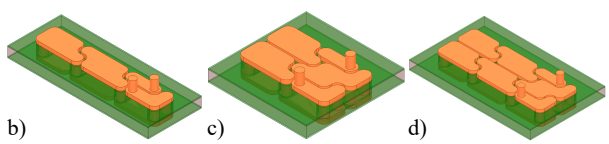

Figure 11: Extensions to the toroidal inductor cell.

Figure 12 shows another important property, the magnetic field is not only a closed path (contained within the magnetic substrate) but is also confined to the inductor structure even when the magnetic sheet is much larger.

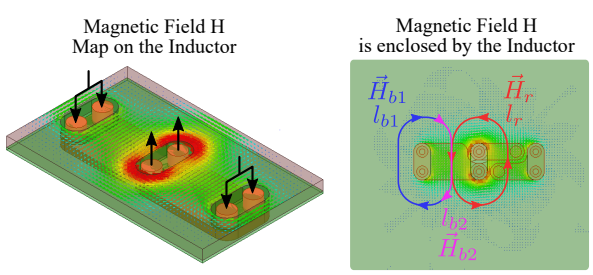

Figure 12: Inductor magnetic field distribution.

From Ampere's law, we have $\oint \vec{H} \cdot dl = Ni$, where N is the number of enclosed vias and i is the current through the via. With H constant on the integration path we have,

$$\begin{aligned} \vec{H}_r &= \frac{2i}{l_r} \\ \vec{H}_{b1} l_{b1} + \vec{H}_{b2} l_{b2} &= i \end{aligned} \tag{8}$$

but $\vec{H}_{b2} = \vec{H}_r$ in the center of the inductor. Using this and combining both previous equations we obtain,

$$\vec{H}_{b1} l_{b1} = i \left(1 - 2\frac{l_{b2}}{l_r}\right)$$

If we assume that $l_{b2} \approx l_r/2$ we get that $2l_{b2}/l_r \approx 1$ and therefore $\vec{H}_{b1} l_{b1} \approx 0$. Then we can estimate that outside the inductor the magnetic field $\vec{H}_{b1}$ is close to zero. This has the important implication that with this design we can integrate all the required inductors in the same magnetic substrate.

VI. Inductor Efficiency Analysis

The current through the inductor is not purely sinusoidal, instead it is a ramp or triangular wave. The inductor current waveform shown in Figure 4 can be expressed as a sine Fourier series as follow,

$$i_L(t) = I_o + \sum_{n=1}^{N} \frac{2\Delta i_L}{D(1-D)} \frac{\sin(n\pi D)}{(n\pi)^2} \sin\left(2n\pi \frac{t}{T_s}\right) \tag{9}$$

from where we can also express the power loss as a sine Fourier series as shown in equation (10) using the previous current expression,

$$P_{L,AC} = \frac{2\Delta i_L^2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} R_L\left(\frac{n}{T_s}\right) \tag{10}$$

Comparing equation (10) with equation (2) we can obtain an expression for the parameter R_{acx} as shown in the expression (11) in terms of the inductor frequency response.

$$R_{acx} = \frac{2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} \frac{R_L(n/f_s)}{L(f_s)} \tag{11}$$

The inductor configuration (d) as shown in Figure 11 with dimensions $3.6 \times 1.9 \times 0.33$ mm^3 along with the material properties for materials HPE1 and RM4A as shown in Figures 8 and 9 were used to simulate and obtain the inductor frequency response for both its inductance and AC resistance, as shown in Figure 13.

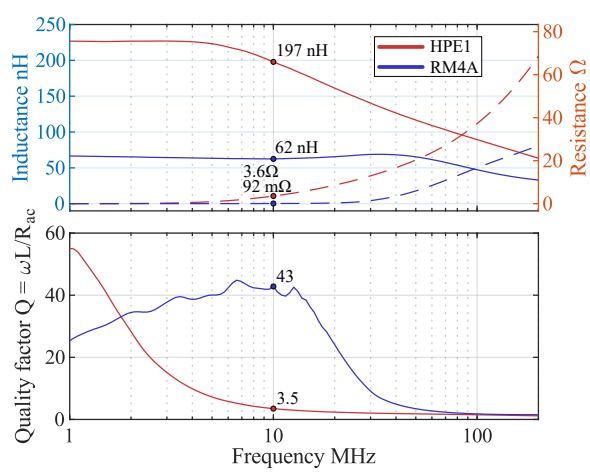

Figure 13: Inductor configuration (d) (from Figure 11) frequency response.

The inductor technology's effective AC resistance R_{acx} with materials HPE1 and RM4A is shown in Figure 14. We observe that even with a very low loss material like the RM4A, it is difficult to meet the resistance requirement, marked with X, for

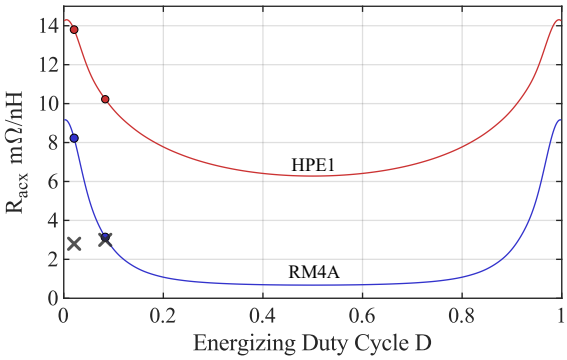

Figure 14: Inductor technology's effective AC resistance density R_{acx}.

duty cycles of 1/48. But with a duty cycle extension by a factor of 4 the material RM4A can, barely, meet the requirement.

Despite the analysis showing that the material RM4A could work for 48V to 1V provided a duty cycle extension is given, the inductance density is too low. As is shown in Figure 13 it has an inductance of 62 nH in a volume of $3.6 \times 1.9 \times 0.33$ mm^3 = 2.26 mm^3. As mentioned previously, the target total inductance should be 364 nH which requires RM4A material to have 6 times the volume, with a significant increase in lateral area and DC resistance.

For 48V to 1V to work we need a material with a permeability somewhere between HPE1 and RM4A, with the low losses of RM4A, and the hysteresis curve of the HPE1.

VII. Required Magnetic Material Properties

From a trade-off between saturation current, inductance density, and DC resistance, the material should have a permeability around 90 and a loss tangent less than 0.033 at 10MHz and stable up to 50MHz. The permeability was modeled using the Lorentz and Landau-Lifshitz-Gilbert shown in [14] with an extra $\gamma\omega_s$ term. The equation is given by

$$\mu_e = 1 + \frac{\omega_d^2 \chi_{d0}}{\omega_d^2 - \omega^2 + j\beta\omega} + \frac{(\omega_s + j\alpha\omega)\omega_s \chi_{s0}}{(\omega_s + j\alpha\omega)^2 + \gamma\omega_s - \omega^2} \quad (12)$$

where χ_{d0} and χ_{s0} are the static magnetic susceptibilities, ω_d and ω_s are the resonant frequencies of each magnetic contributions, α, β, γ are damping factors. To obtain a starting point for the model, the RM4A material was fitted using this model. The result is shown in Figure 15, with the reference data on black lines and the model on green lines.

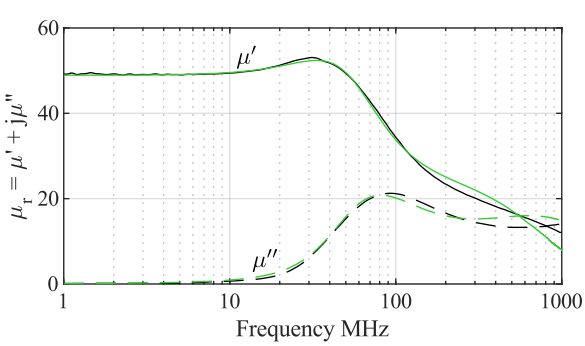

Figure 15: Material RM4A fitted with model of equation (12).

We observe that the model can predict with enough accuracy up to 300 MHz. Using this starting point, the required material (CA90U33LT) with permeability 90 and loss tangent 0.033 at 10MHz was modeled. These material properties are compared with the HPE1 and shown in Figure 16.

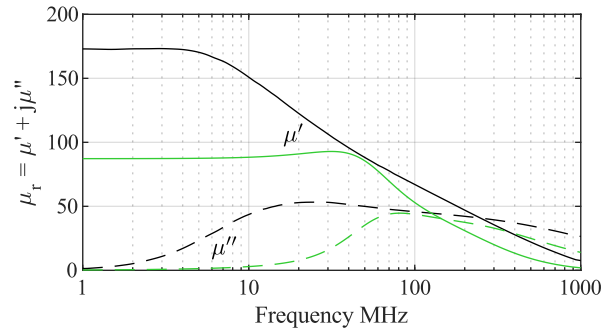

Figure 16: Required material CA90U33LT modeled with equation (12) in green, and measured permeability of HPE1 in black.

VIII. Required Inductor Performance

In order to obtain the expected inductance density of more than 90 nH/mm^3, the inductor structure was further extended as shown in Figure 17, with a tapped connection in the middle.

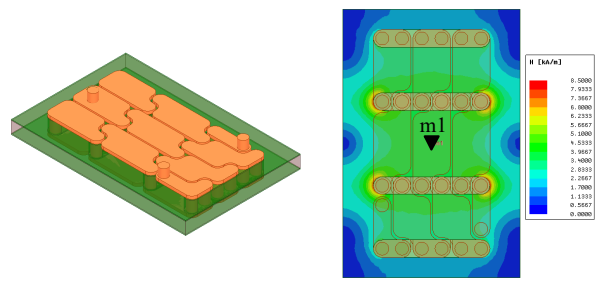

Figure 17: Extended inductor for 48V to 1V using hybrid series capacitor tapped inductor. Marker m1 = 3.9 kA/m.

This structure has a total DC resistance $R_{DC} = 24$ mΩ, total inductance $L = 374$ nH, saturation current $I_{sat} = 2.5$ A, and volume $V = 3.0 \times 2.0 \times 0.533$ mm^3 = 3.2 mm^3 giving an inductance density of 113 nH/mm^3.

As the inductor is switched between using the entire inductor during the energizing duty cycle and using only half of it during the rest of the switching period, the effective DC resistance is lower. If we denote I_{L1} and Δi_{L1} as the DC and current ripple during the energizing duty cycle, and I_{L2} and Δi_{L2} as the currents during the rest of the period, the next relations of energies must be satisfied,

$$2 \times (4L) I_{L1} \Delta i_{L1} = 2 \times (L) I_{L2} \Delta i_{L2} \quad (13)$$

$$0.5 \times (4L)(I_{L1} + \Delta i_{L1})^2 = 0.5 \times (L)(I_{L2} + \Delta i_{L2})^2 \quad (14)$$

where equation (13) means that the energy stored during the DT_s interval must be equal to the energy release during the rest of the period equal to $(1-D)T_s$. Equation (14) implies that, at the instants $D(T_s - \epsilon)$ and $D(T_s + \epsilon)$ with $\epsilon \to 0$, the total energy is conserved.

The current ripple Δi_{L2} is given by the magnetizing inductance of the secondary and the output voltage with $\Delta i_{L2} = 0.5 V_o (1-D) T_s / L$. The current I_{L2} is equal to the output current,

i.e. $I_{L2} = I_o$. We can solve for I_{L1} and Δi_{L1} to obtain,

$$I_{L1} = \frac{I_o}{2} \tag{15}$$

$$\Delta i_{L1} = \frac{\Delta i_L}{2} \tag{16}$$

If the output current is 2.5A and the current ripple is 0.5A, the inductor current during the energizing interval would be 1.25A with a current ripple of 0.25A. Therefore, the total inductance sees a maximum current of 1.5A and we can allow the saturation current to be 2A or greater.

The frequency response for this inductor configuration and material CA90U33LT is shown in Figure 18.

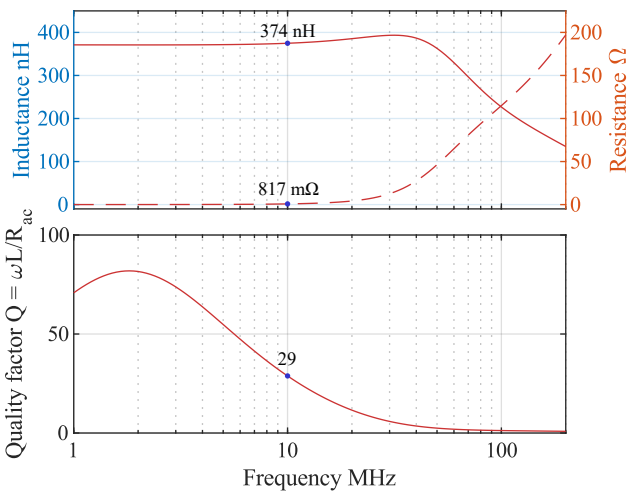

Figure 18: Required inductor frequency response.

Figure 19 shows the comparison of the proposed material properties against HPE1 and RM4A.

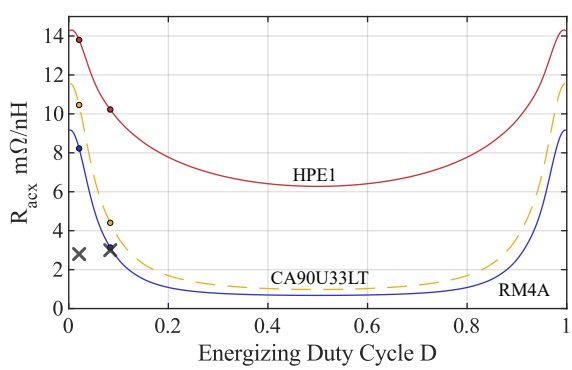

Figure 19: Inductor technology effective AC resistance density R_{acx}. Material CA90U33LT in yellow dashed line.

Still, we see that even a very low loss tangent of 0.033 is not enough to meet the target R_{acx}. This suggests an even more efficient material is needed or we need to further increase the inductance density and total inductance as per Figure 5.

IX. Fabrication Process

Inductors with a high inductance density but low DC resistance entails a trade-off between the thickness and number of copper windings. Inductors with high inductance density can be easily achieved with large number of windings. This inevitably leads to a large form factor and high DC resistance. A low resistance is imperative for power modules to reduce joule heating and stresses induced in the package due to thermal loading.

By incorporating advanced high-permeability magnetic composites as the core, the inductors can achieve high-inductance density without the need for large number of windings. Magnetic-core toroid inductors were designed for high conversion ratio converters and to ensure package embedding and thereby reduce interconnection lengths and associated parasitics.

The inductor design presented in this work [13] is to be fabricated using a magnetic sheet as substrate. In this, substrate slots are first drilled to make sure no magnetic material is between the vias and the coupling between them is maximized. This is important to achieve coupled inductors at this level of integration. The slots are then filled with dielectric and the vias are drilled in the slots to form the inductor. A process was developed to fabricate the designed inductors, as shown in Figure 20.

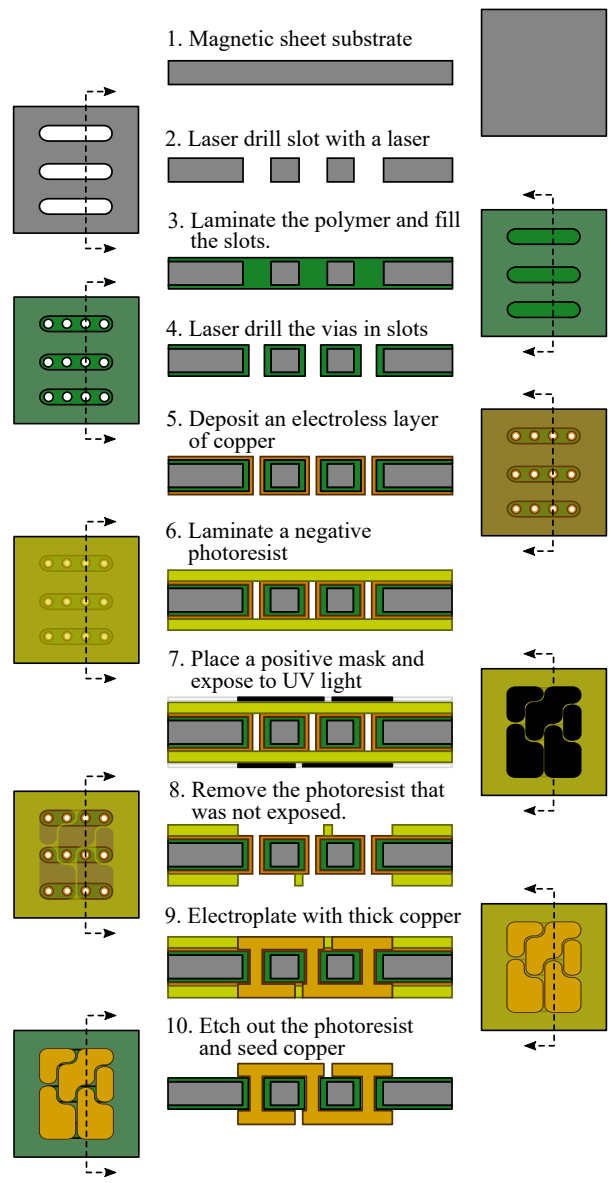

Figure 20: Fabrication process flow chart.

First a magnetic sheet is used as the substrate/core and ellipsoidal slots are drilled with a femto-second laser (steps 1 and 2). The femto-second laser thermally ablates the material

by impinging excited electrons on the core surface, that ionizes the material. The material evaporates in the form of plasma, creating the desired pattern. The size of the slots is controlled by optimizing the laser power, speed and drill repetitions.

Figure 21 (a) shows the initial attempts at drilling slots in the core, by only increasing the number of laser pulses. The process was optimized by pulsing laser at high speeds repeatedly in incremental steps, downward (z direction) through the core, keeping the laser power low. This prevents local heating of the material, which causes burning of the edges and flaking of magnetic particles in the core. The thickness of the core controls the accuracy and cleanliness of the slot. As expected, thicker cores need high power for the through slots, causing more error in the cuts. Figure 21 (b) shows the slots drilled using the optimized drilling process.

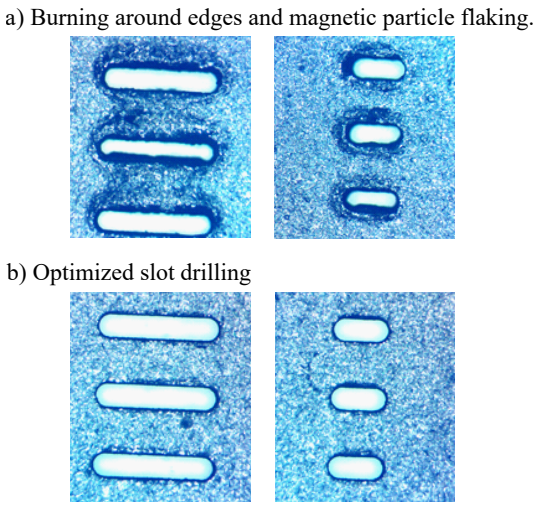

Figure 21: Top view of (a) initial slots in the core showing burnt edges and flaking of magnetic particles, due to thick core, high laser power and low laser speed (b) slots in the core using optimized laser drilling process.

In step 3, the slots are filled with a 15 μm ABF^{TM} film, by hot pressing under vacuum at the viscoelastic temperature of the dielectric, allowing it to flow into the slots. Thicker cores require thicker films to fill the slots completely in order to avoid voids and sagging of the dielectric within the slots. Next (step 4), the vias are laser drilled in the polymer-filled slots (via-in-via drilling). This allows the vias to be separated from each other by dielectric, leading to a toroidal structure around the top and bottom copper traces through the isolated vias. This process was optimized in a similar fashion as the slots. The top view of the vias drilled in the polymer-filled slots are shown in Figure 22.

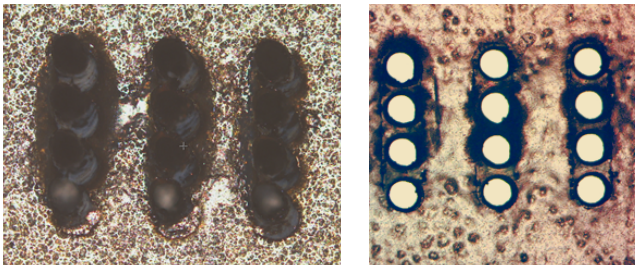

Figure 22: Top view of (a) initial vias in the polymer filled slots showing burnt edges and misalignment (b) vias in slots using optimized laser drilling process.

In step 5, a thin layer of electroless copper seed layer is deposited. This is followed by Ultraviolet lithography process, where a negative photoresist is laminated over the copper seed layer (step 6) and a positive mask is used to pattern the top and bottom layers (step 7). The photoresist that was not exposed is removed (step 8) and the inductor pattern become visible as shown in Figure 23.

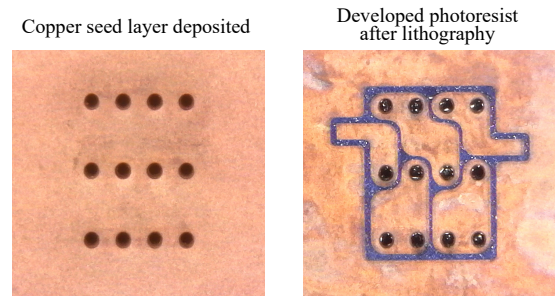

Figure 23: Top and bottom view after the photoresist development, exposing copper seed layer.

Then the copper top layer, bottom layer, and vias are electroplated (step 9). The remaining photoresist is stripped, the plated copper is annealed to remove residual copper stress, and finally the copper seed layer is etched using a differential etching process leaving behind the fabricated inductor (step 10). Figure 24 shows the inductor after the fabrication is completed.

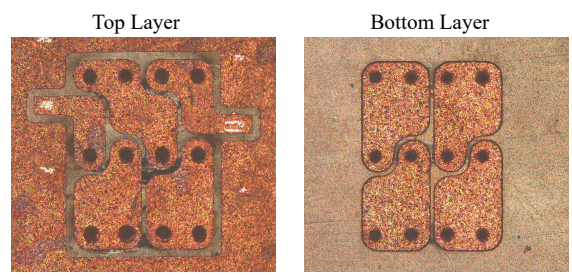

Figure 24: Fabricated toroid inductor after step 10.

X. Fabrication Results

To demonstrate the fabrication process, the inductor configuration (c) of Figure 11 was fabricated using the material HPE1 which has a thickness of 100 μm. Figure 25 shows two cross sectional views of the inductor and Figure 26 shows a close-up of the via structure.

The simulation model in ANSYS^{TM} HFSS was adjusted to match the fabricated results. The inductor layout and its dimensions are shown in Figure 27. The average copper thickness is 25 μm. The magnetic sheet size is set to be a square with width of 5mm. For simulation we use the measured material properties shown in Figure 6.

Figure 28 shows the fabricated inductor with structures for shunt measurements. For the inductance measurement, RF probes ACP40-GSG-500 from Cascade Microtech^{TM} were used. To measure in the range of 10 MHz and 500 MHz, a VNA from Agilent Technologies ^{TM} model E8363B was used, and in the range of 1 MHz to 50 MHz an open source low frequency VNA was used. To measure the DC resistance a 4-wire method with DC probes DCP-150K-50 and multimeter from Hewlett Packard model 34401A was used.

The measured DC resistance is $R_{DC,meas} = 16$ mΩ and the simulated value is $R_{DC,sym} = 13$ mΩ. The measured inductance

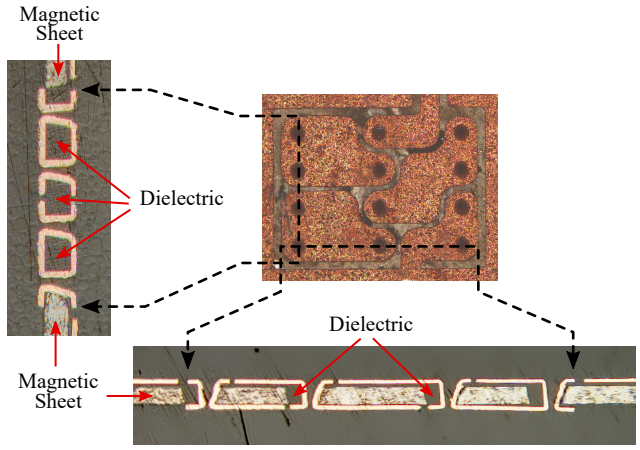

Figure 25: Cross section of fabricated inductor.

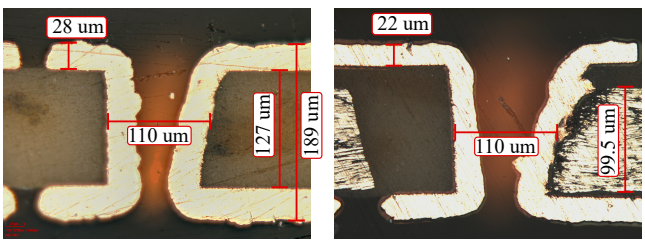

Figure 26: Fabricated inductor cross sections of vias with dimensions.

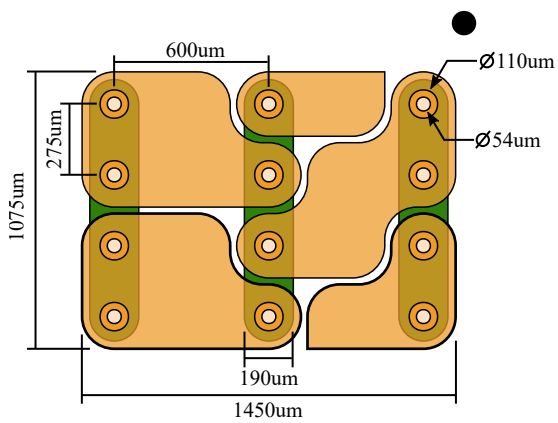

Figure 27: Simulated inductor dimensions.

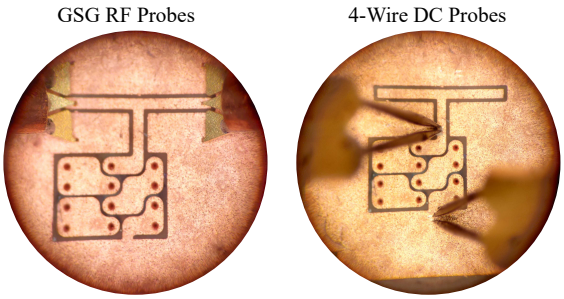

Figure 28: Probes setup for measurements of inductance, AC resistance, and DC resistance.

and AC resistance is shown in Figure 29. We observe that there is a good correlation between the simulation model and the measurements using the fabricated inductor.

Table I shows the comparison of values obtained by simulation and from measurements.

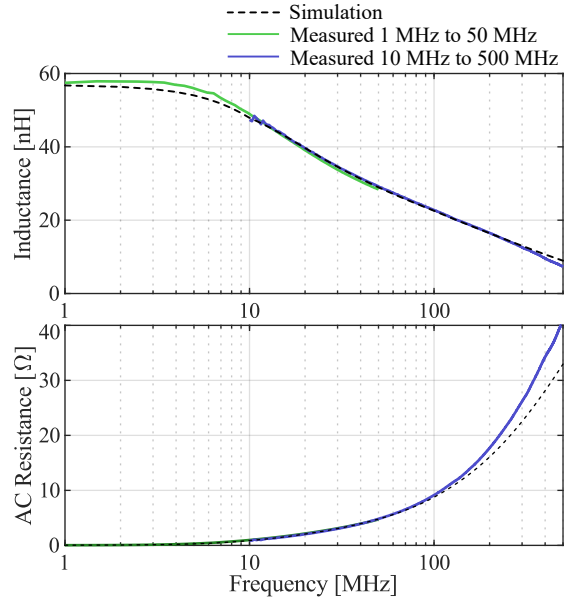

Figure 29: Comparison between simulated and measured inductance and resistance (measured between 1 MHz to 50 MHz in green, measured between 10 MHz to 500 MHz in blue, and simulated data in dash black line).

Freq. MHz	Simulated		Measured	
	L nH	R_{AC} Ω	L nH	R_{AC} Ω
1	56.8	0.036	57.5	0.031
5	54.0	0.277	55.9	0.321
10	47.9	0.882	48.9	0.977
50	29.0	4.790	29.2	4.841
100	22.6	8.760	22.8	9.139
500	8.9	32.968	7.4	40.822

Table I: Measured and simulated values for inductance and AC resistance.

When we simulate the inductor using a magnetic sheet with width = 1.8 mm and length = 1.7 mm, the inductance at 10MHz, reduces from 47.9 nH to 44.95 nH. This is only a reduction of 6% from an inductor in a magnetic sheet with infinite width and length dimensions. The resulting volumetric inductance density at 10 MHz is $44.95/(1.8\times1.7\times0.189) = 77.7$ nH mm^{-3}, and the surface inductance density at the same frequency is $44.95/(1.8\times1.7) = 14.7$ nH mm^{-2}

If the inductor presented in Section VIII is fabricated with this process and using the material CA90U33LT shown in Figure 16, the inductance density would be 113 nH mm^{-3}.

XI. Conclusions

High voltage and high conversion 48V to 1V integrated voltage regulators are limited in frequency of operation by the power stage due to the switching losses and by the magnetic material due to its frequency range of operation and high losses at high frequencies. The higher difficulty of this task is better shown by using the parameter called effective AC resistance or R_{acx}. A low voltage 1.7V to 1V IVR running at 50 MHz only requires 8 nH and R_{acx} = 32.6 mΩ/nH allowing the use of air core inductors or very lossy magnetic materials. In contrast, for 48V to 1V IVR running at 10 MHz (which is already challenging for the power stage) an inductance of 364 nH, R_{acx} = 3 mΩ/nH, and $R_{DC} =$ 18 mΩ is required, which needs the use of high permeability ultra-high efficiency magnetic sheets.

In order to satisfy the inductor requirements, a material was modeled with permeability 90 and loss tangent factor of 0.033 at

10 MHz stable up to 50 MHz. This material along with the novel inductor proposed in this work can deliver an inductance density of 113 nH/mm^3 and effective AC resistance $R_{acx} = 4.2$ mΩ/nH. For 48V to 1V the required R_{acx} is 3 mΩ/nH, which means that more advances in magnetic material are required to create ultra efficient magnetic sheet along with a further increase in the total inductance. The proposed inductor can achieve 374 nH in an area of 6 mm^2 and volume of 3.2 mm^3, DC resistance of 24 mΩ, effective AC resistance R_{acx} of 4.2 mΩ/nH, and saturation current of 2.5A.

The measurements of the fabricated inductor correlates very well with the simulation model. This allows to predict with good accuracy other inductors derived from the novel basic toroidal inductor cell [13] presented in Figure 10.

Both, the novel inductor design [13] and the proposed magnetic sheet material can allow the next generation data centers to incorporate single stage 48V to 1V integrated voltage regulators. The fabrication process shown in this work, along with the enclosed magnetic field property of the inductor, enables to build many inductors as required by all the down conversion phases in order to deliver hundreds of amperes of current demanded by today processors.

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