Greetings from
Georgia Tech
Interconnect and Packaging Center (IPC)
Madhavan Swaminathan, Director
Muhannad Bakir, Associate Director
School of Electrical and Computer Engineering
SRC
GRC
Georgia Tech
Institute for Electronics and Nanotechnology
INTERCONNECT and PACKAGING CENTER

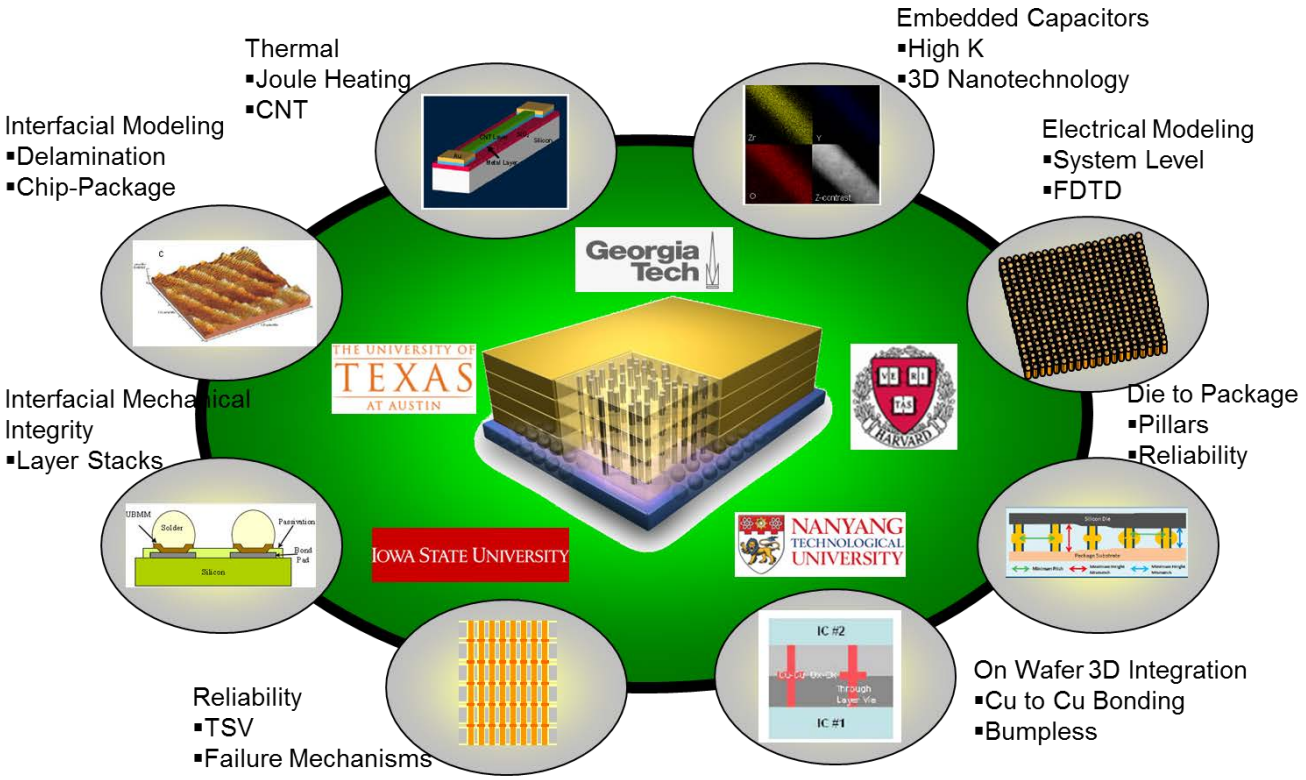
Outline

- A brief introduction of IPC

- Research Presentations – A Snap Shot
  - Packaging – Madhavan Swaminathan
  - CAD, Circuits, Architecture – Sungkyu Lim
  - Devices, Circuits, Interconnects – Muhannad Bakir

Interconnect and Packaging Center (cont.)

- Established in 2009 as an SRC Center of Excellence
- Multi-university center with research focus on 3D Technologies, leading to 3D IC technology innovation, exploration, and discoveries
- Started with Nine faculty and several graduate students
- Paul Kohl (GT), Scott List (SRC) – Started the program
- Jon Candelaria (SRC) – Served as program director

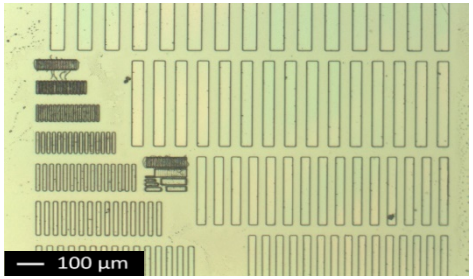


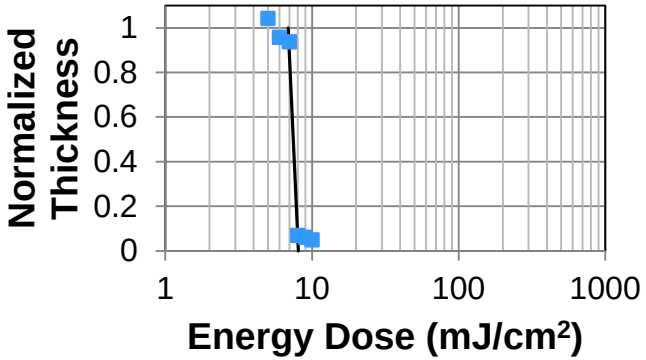
Research Presentations
Packaging

- Paul Kohl, ChBE
- Suresh Sitaraman, ME
- Rao Tummala, ECE/MSE
- Madhavan Swaminathan, ECE

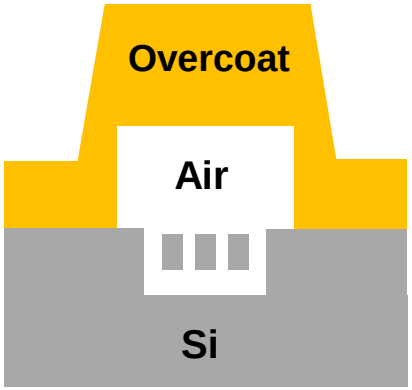
New Polymeric Materials for Interconnect and Packaging

Paul A. Kohl, ChBE

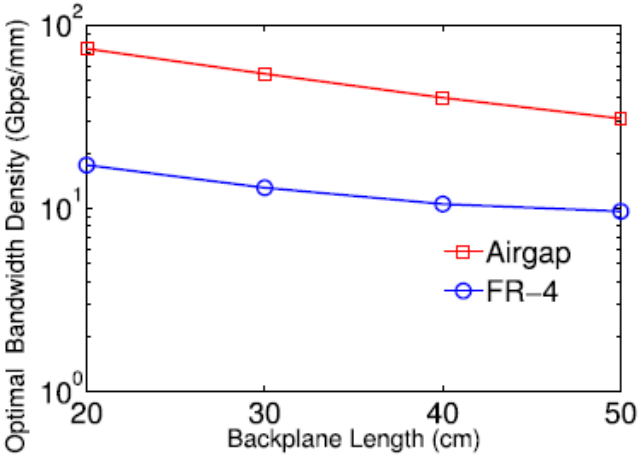




First chemically amplified, positive tone, aqueous developed permanent dielectric for electronic packages. Sensitive is 10-20x higher than non-chemically amplified



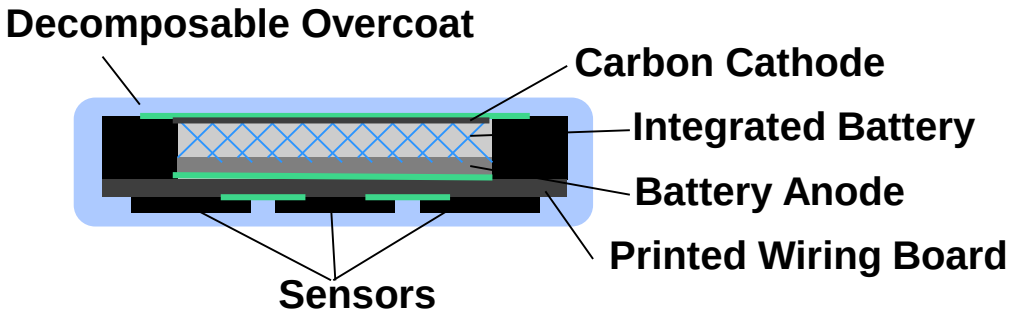
Family of sacrificial polymers for (i) ultra low-k insulation on PWB and (ii) low-cost MEMS packaging using lead-frame and epoxy overmolded packages



Demonstrated that air-isolated interconnect on PWB has 4x higher bandwidth density at optimum energy/bit

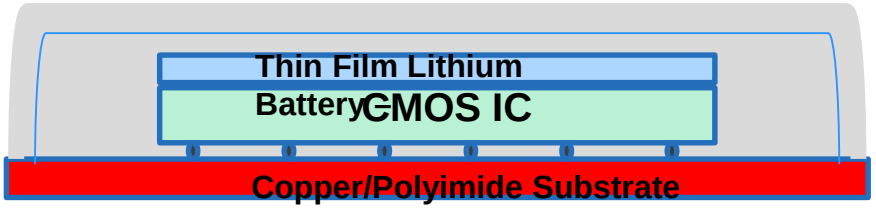
Battery Integration into ICs and Packages

Paul A. Kohl, ChBE



Self powered sensors- vanish on command (DARPA)- decomposable PWB, case and battery

Integrated, thin-film battery-including new designs for low-voltage, high energy density future wireless devices

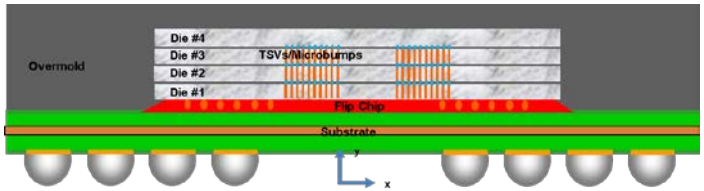


Previous SRC Projects Include:

- IFC (Focus Center): (i) Ultra-low dielectric constant materials for packages, (ii) integrated power sources in ICs and Packages, (iii) waste heat recovery and reuse via new absorption cycle refrigeration
- All copper chip-to-substrate attachment replacing solder attachment
- Improvements in polyimide adhesion and surface roughness for interconnect

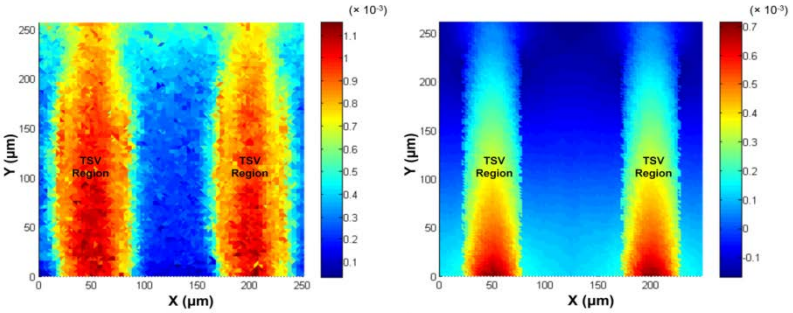
3D Microsystems and Through-Silicon Vias

Suresh K. Sitaraman, ME



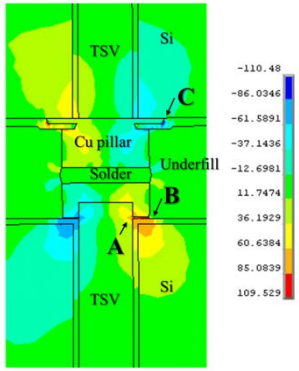
Stacked die with TSV modeling

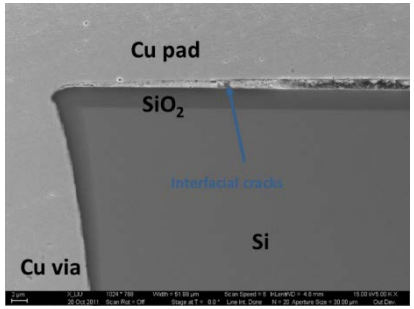
- Developed validated models to predict failures in TSVs
- Developed design guidelines for next-generation TSVs
- Sensors to measure strains near TSVs

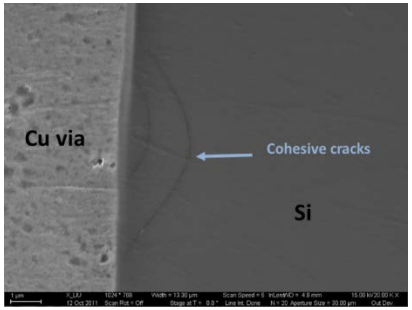


$(a)\ \varepsilon'_{xx}$

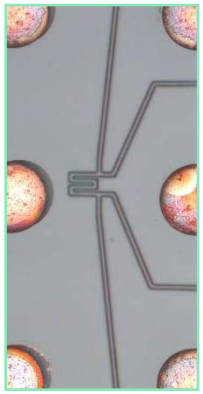
Synchrotron XRD measurements and model predictions

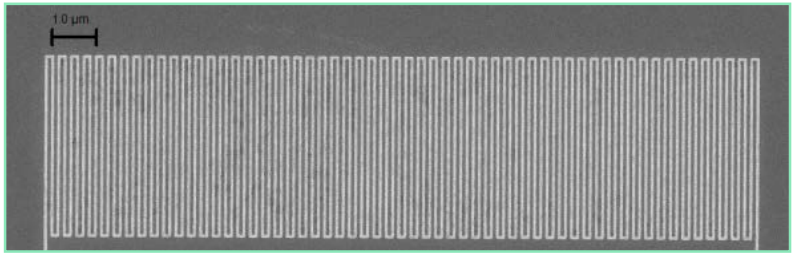


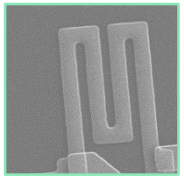




Cu/SiO2 Interfacial Cracking and SiO2 Cracking



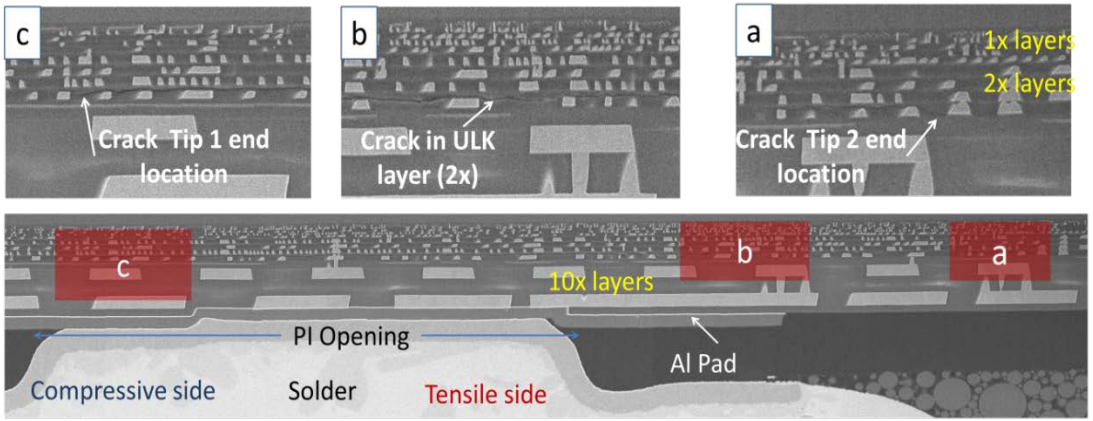




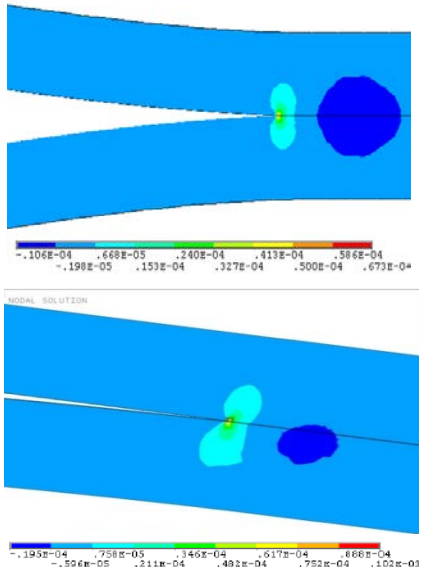
Nano- and Micro-Scale Strain Sensors

On-Chip Interfacial Delamination

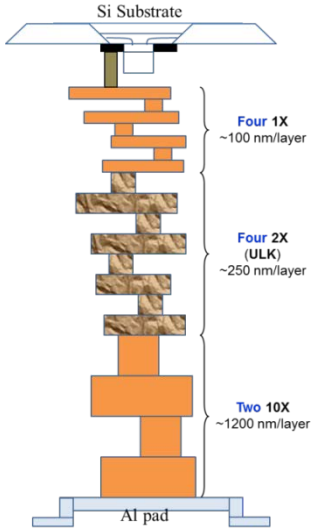
Suresh K. Sitaraman
ME



BEOL Cracking

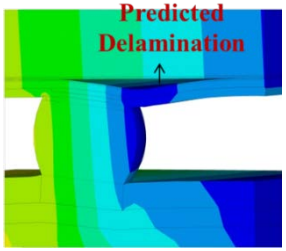


Interfacial Delamination Models



Example BEOL Stack

Interfacial Delamination Tests



BEOL Cracking Predictions

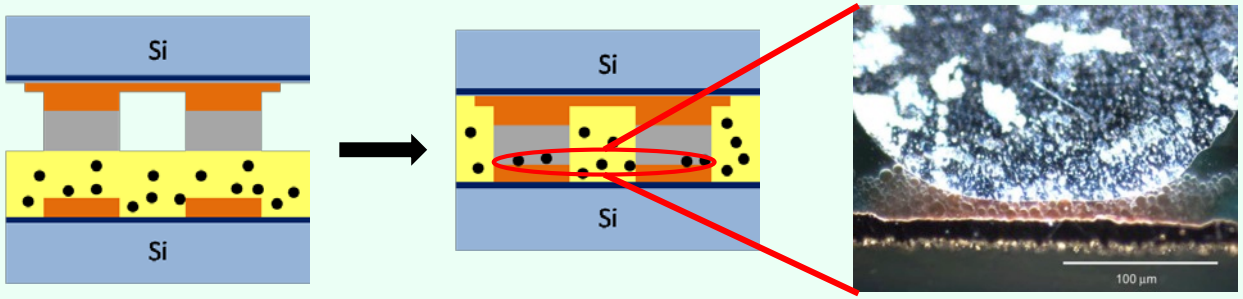
- Developed cohesive zone models (CZM) to predict the onset and propagation of delamination
- Developed innovative approach to extract CZM parameters from experimental tests
- Demonstrated application to on-chip and off-chip interfacial delamination
- Developed pathways to mitigate interfacial failures

Simultaneous Stack-Bonding and Underfill Encapsulation by Self Patterning

Objective:
High-reliability and high-throughput assembly processes for 3D IC stacks with ultra-thin interconnections, using simultaneous assembly and underfilling by self-patterning

Rao Tummala, ECE/MSE

Current process:
Simultaneous assembly and underfilling



Fillers trapped !!

SRC project focus:
Simultaneous assembly and underfilling with self-patterning

No filler entrapment with self-patterning

Task 1: Create superhydrophobic surface for underfill self-patterning

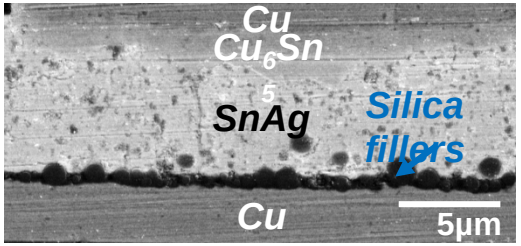
Task 2: UF formulation for thermocompression bonding (TCB)

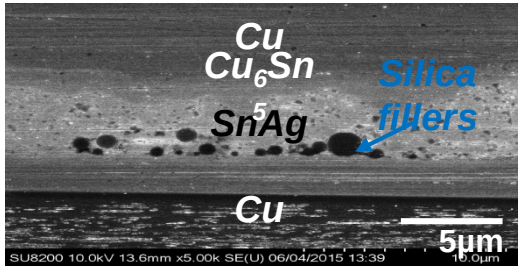
Task 3: TCB process and reliability characterization

Key Accomplishments

Rao Tummala
ECE/MSE

Task 1: Demonstrated superhydrophobic surface for underfill self-patterning

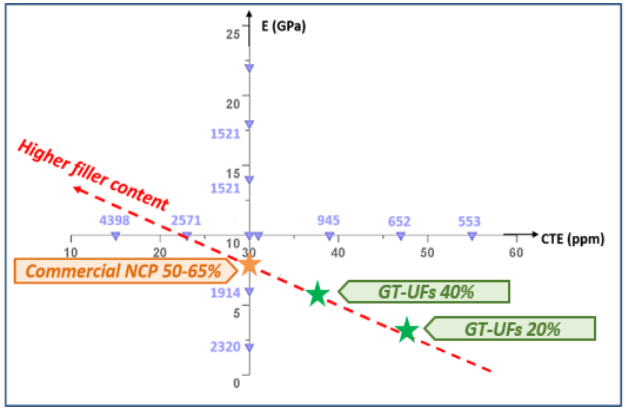




- Self-patterning of silica-filled underfill on copper pads by superhydrophobic treatment
- SEM cross-sections illustrate lower filler entrapment for improved reliability;

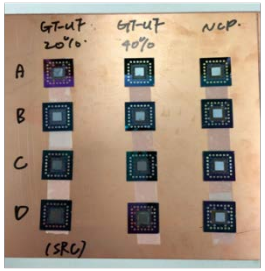
Task 2: UF formulation for TCB:

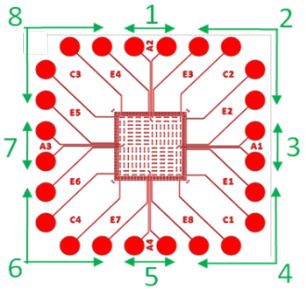
- FEM modeling for optimal underfill properties
- Developed self-fluxed underfill with various filler contents



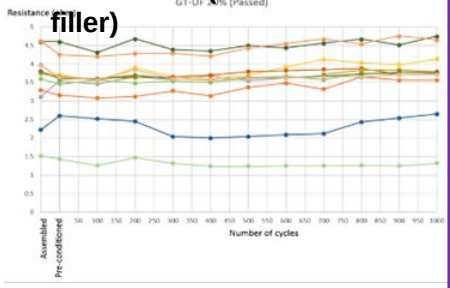
TCT prediction for various combinations of UF CTE and modulus

Task 3: TCB process and reliability characterization





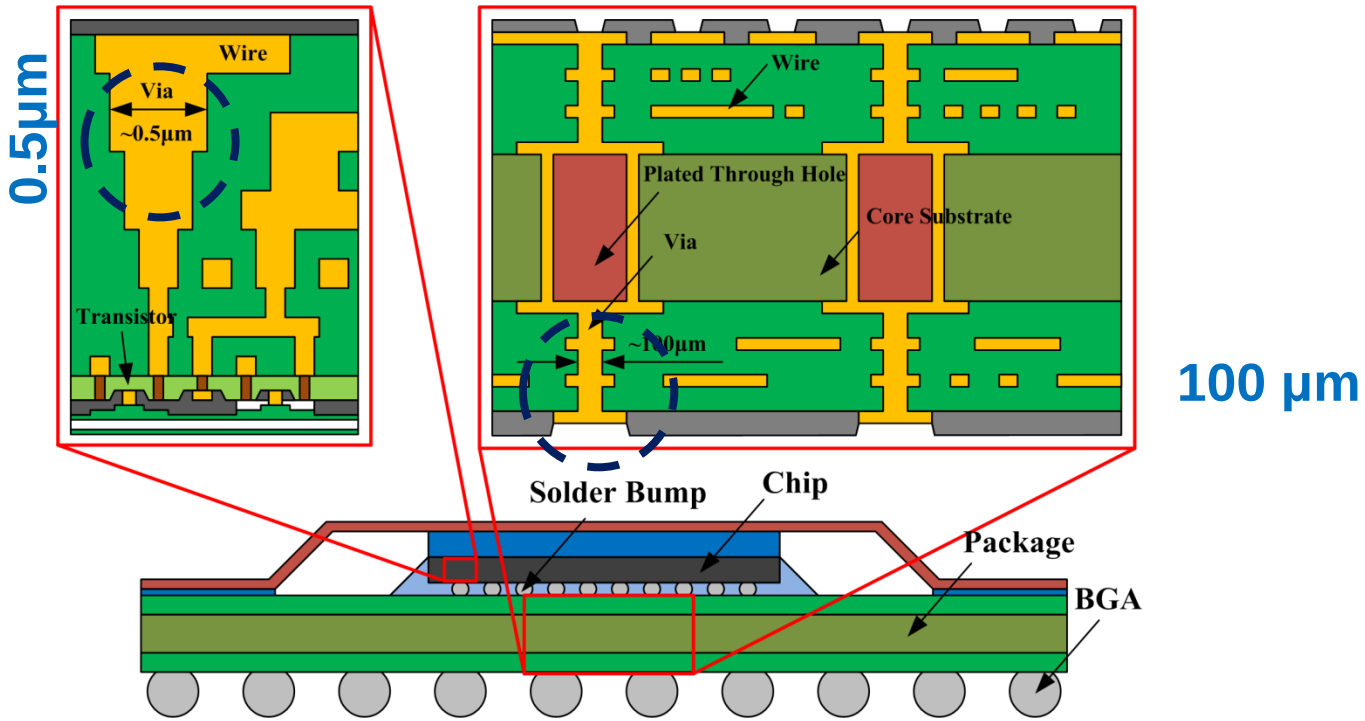
1000-cycle reliability with GT-UF (20 vol. % filler)

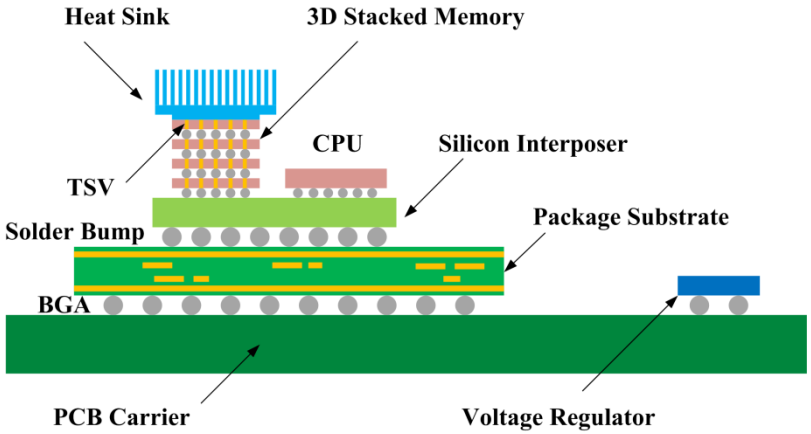


Performed assembly, reliability characterization and failure analysis correlating failures to filler entrapment;

Multiscale Modeling and Simulation

Madhavan Swaminathan
ECE

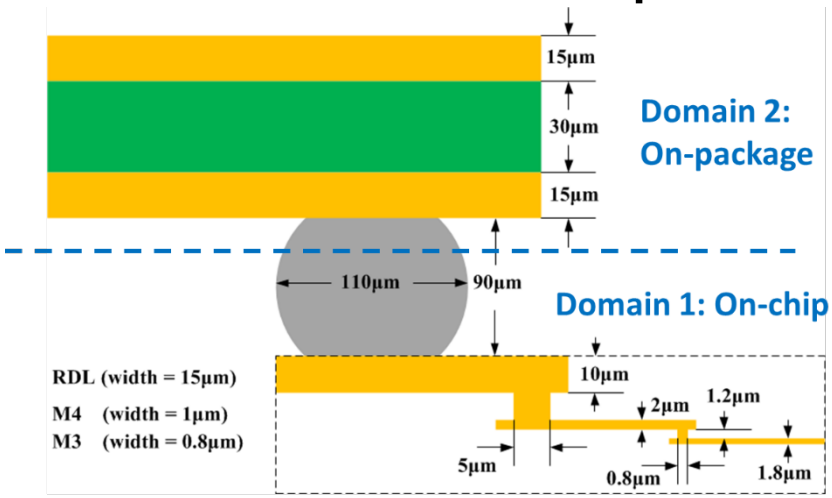




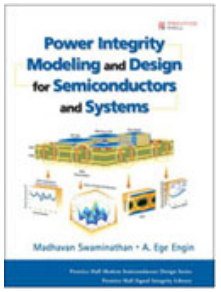
- Electromagnetic modeling of chip and package with multiple length scales
- Focus on Frequency and Time Domain Methods
- New techniques for modeling TSV in silicon interposers
- Domain decomposition based fine difference methods
- Method of moments with specialized basis functions
- Extension to include surface roughness for advanced interconnects such as SIW (w/ Intel)
- Extension to include multiphysics

Recent Accomplishments

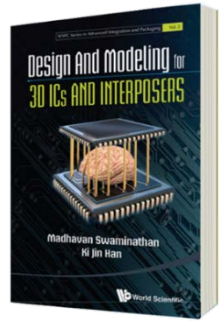
Madhavan Swaminathan
ECE



Multiscale interconnects in chip-package structure

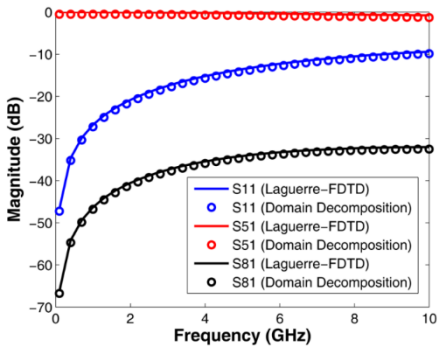


2007

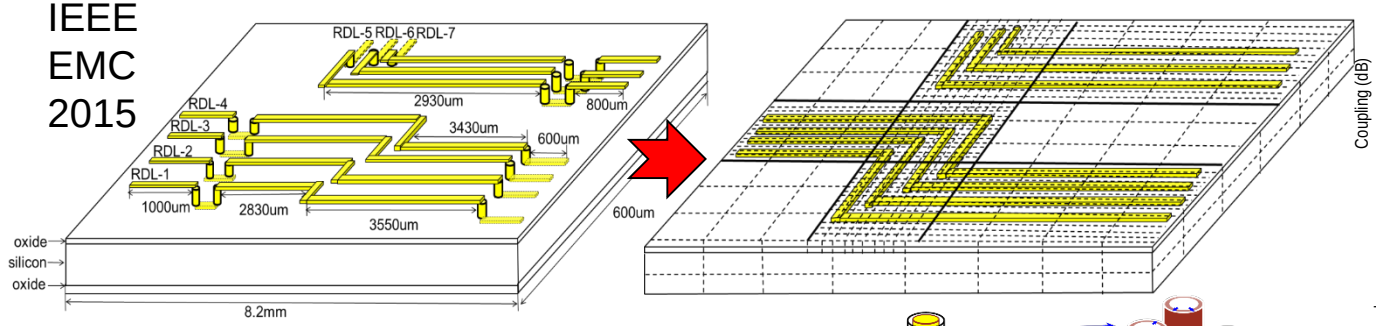


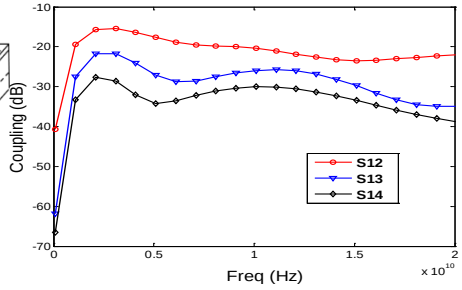
2013

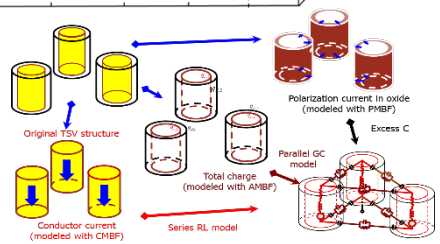
First demonstration of Laguerre-FDTD with Domain Decomposition (IEEE CPMT 2015)

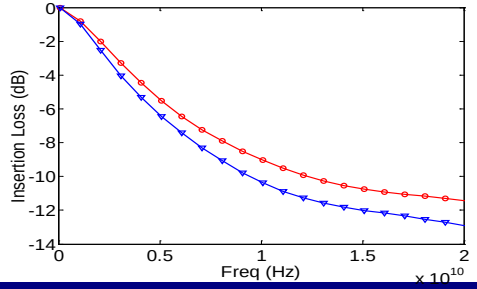


IEEE EMC 2015



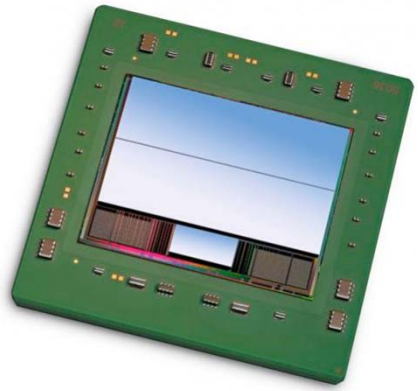


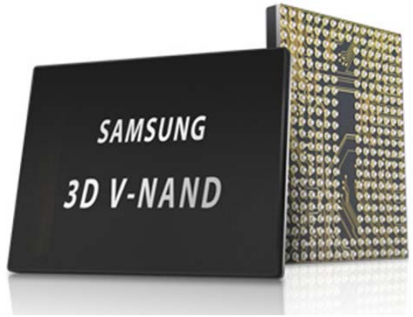




- Modeling of Silicon Interposer
- Specialized basis functions for TSVs
- Domain decomposition
- Finite Difference Frequency Domain

3D IC: Where Are We?





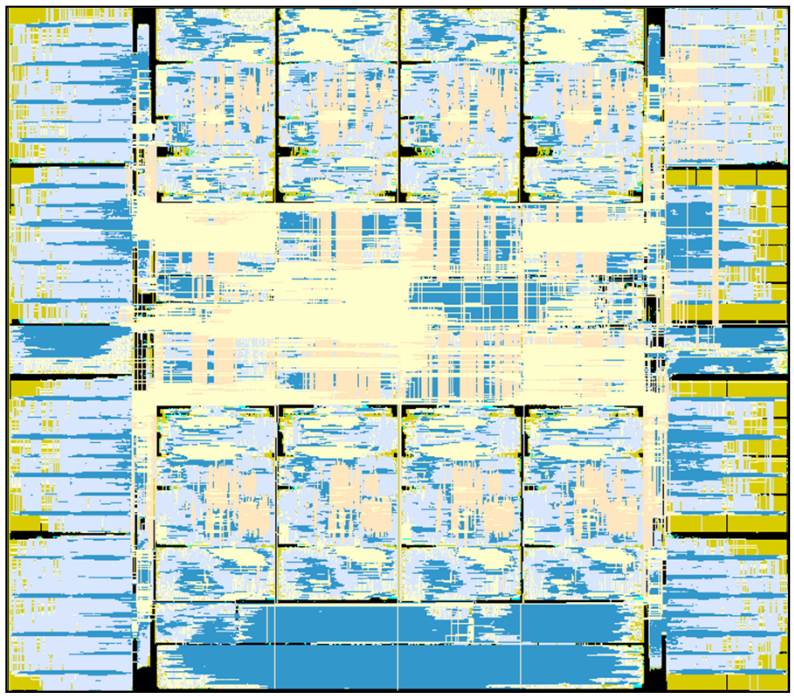
Gen 1	Gen 2	Gen 3	Gen 4
package-on-package	interposer	on-chip TSV	monolithic 3D
Package-oriented (OSAT)		Chip-oriented (foundries)	
Mobile commercialized	FPGA, GPU commercialized	HMC & HBM commercialized	V-NAND commercialized
		logic+logic next	logic+memory logic+logic next

Power Saving with 3D ICs

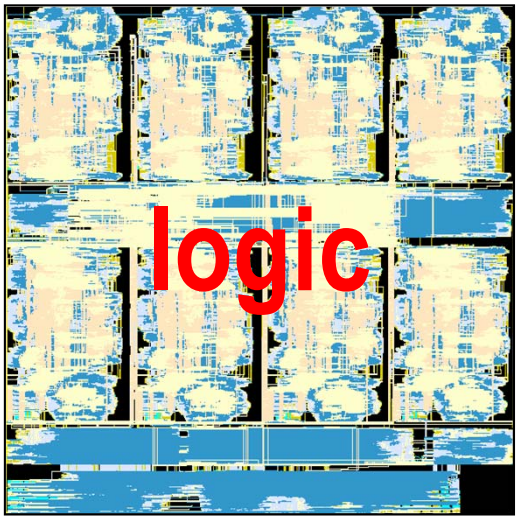
(PI: Sung Kyu Lim, GRC-SLD 2293)

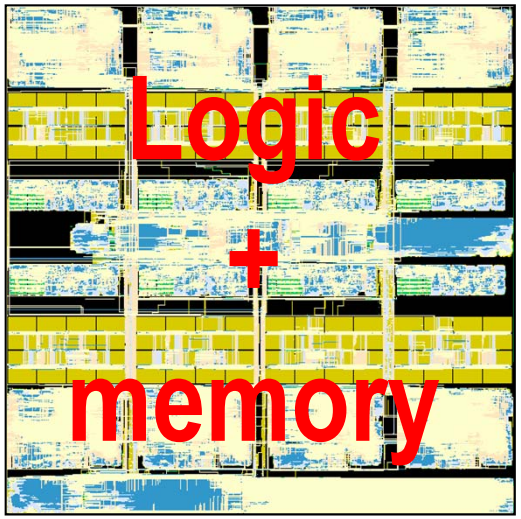
670MHz

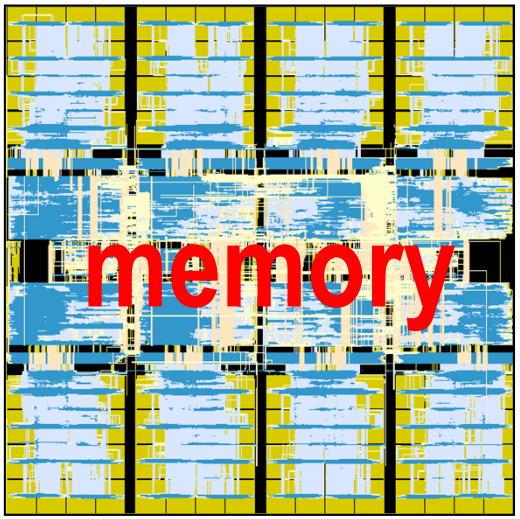
SYN 28nm (bulk)



2D (8x9mm, 8.24W)

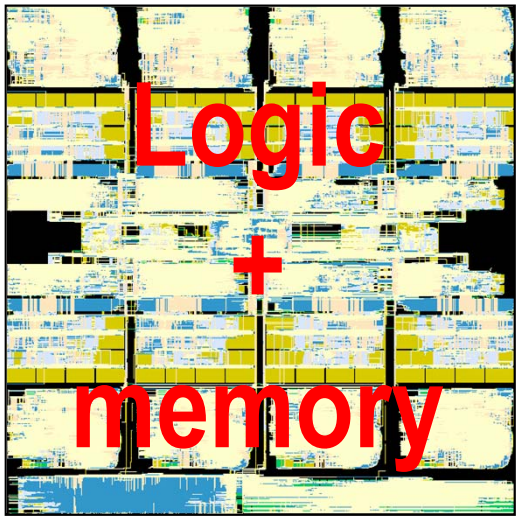






3D (6x6.4mm, 7.19W)

Δ12.7%, TSV=3,263



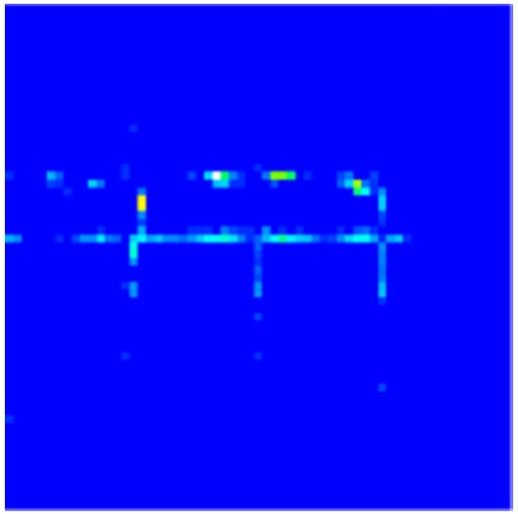
3D (6x6.4mm, 6.81W)

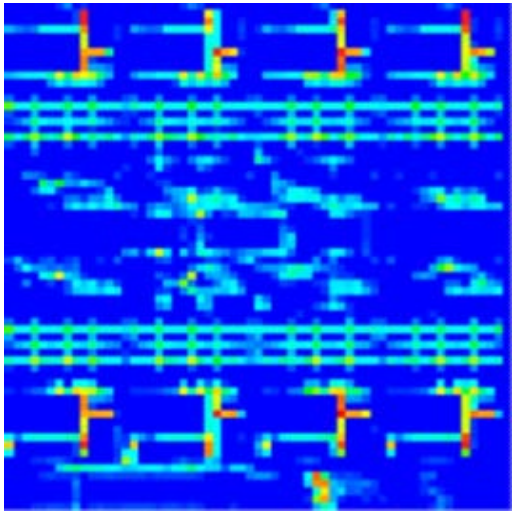
Δ17.3%, TSV=69,091

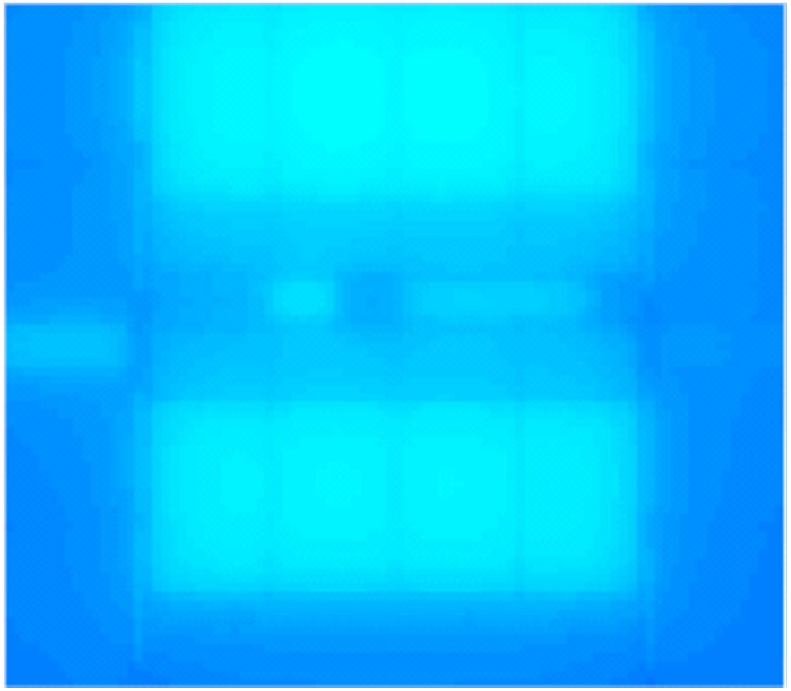
Thermal Analysis

(PI: Sung Kyu Lim, GRC-SLD 2293)

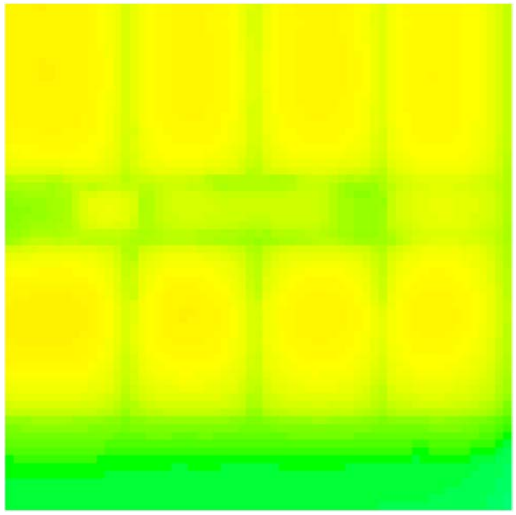
Thermal conductivity map
= where TSVs are



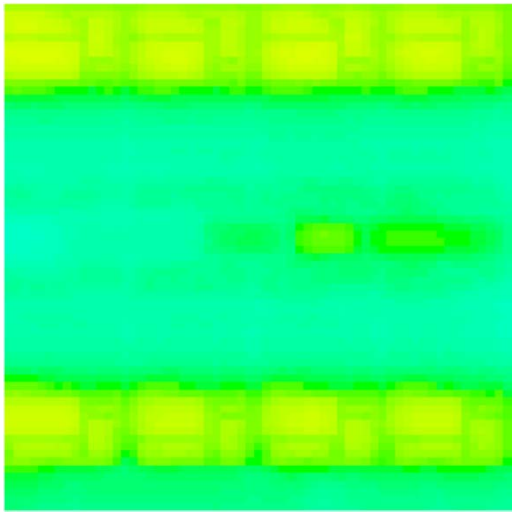




2D (Tmax = 45.4^{O}C)



3D (Tmax = 61.7^{O}C)

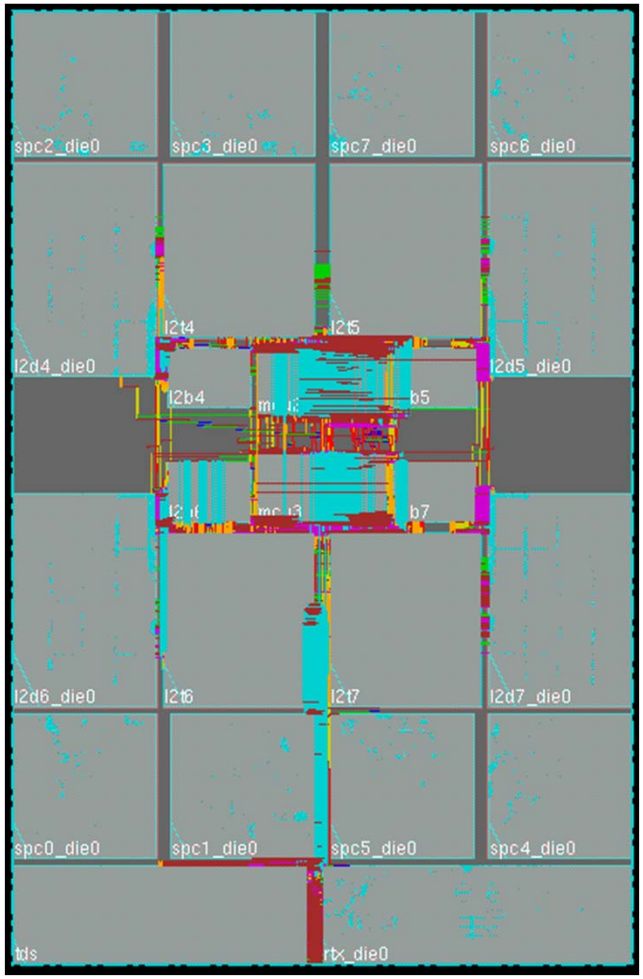


3D (Tmax = 59.2^{O}C)

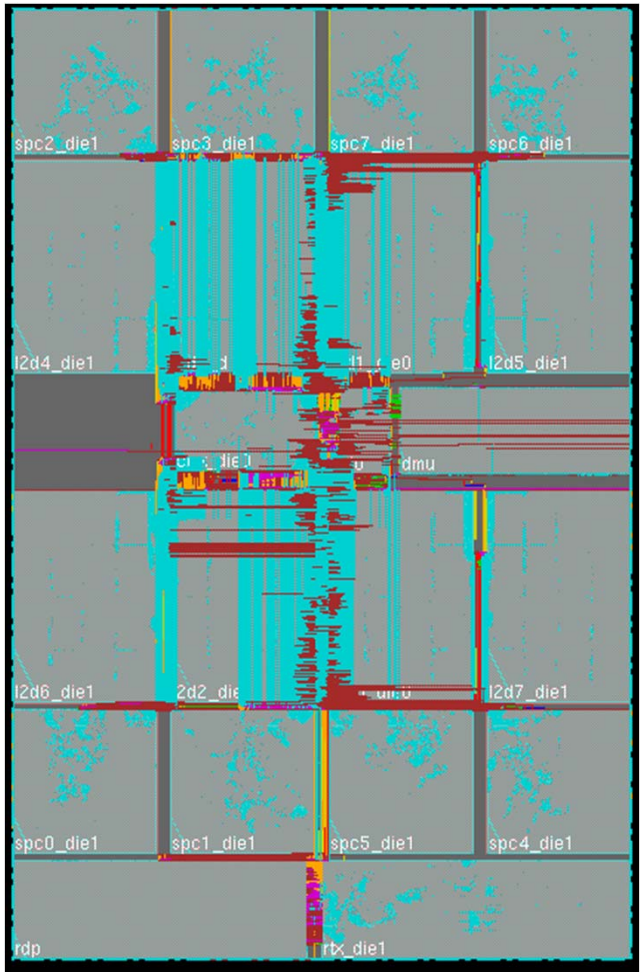
Want More Saving? Add One More Tier

(PI: Sung Kyu Lim, GRC-SLD 2293)

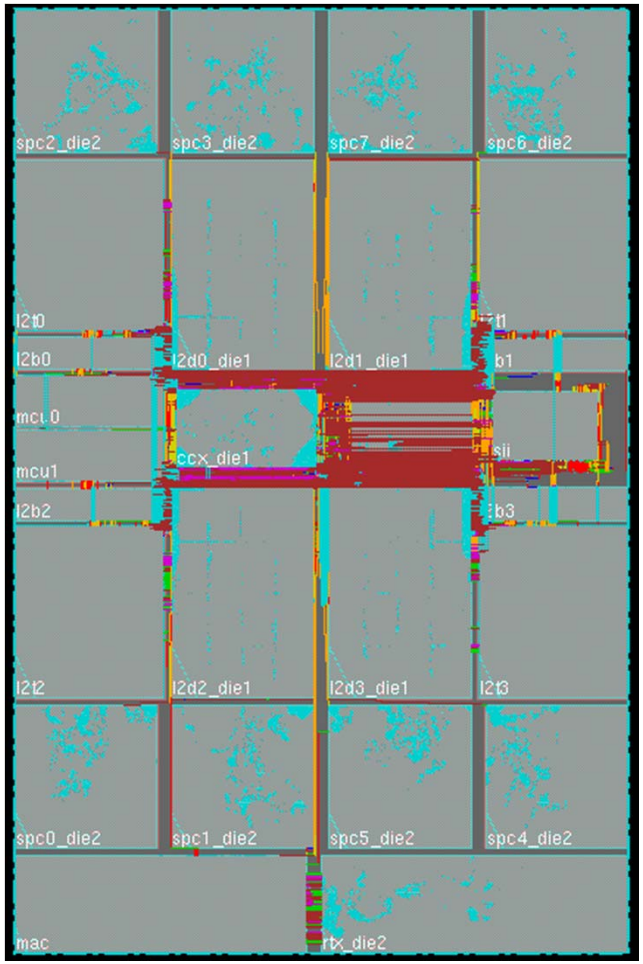
- **Power saving is now 25.6%! = one node advantage**



Tier 1



Tier 2

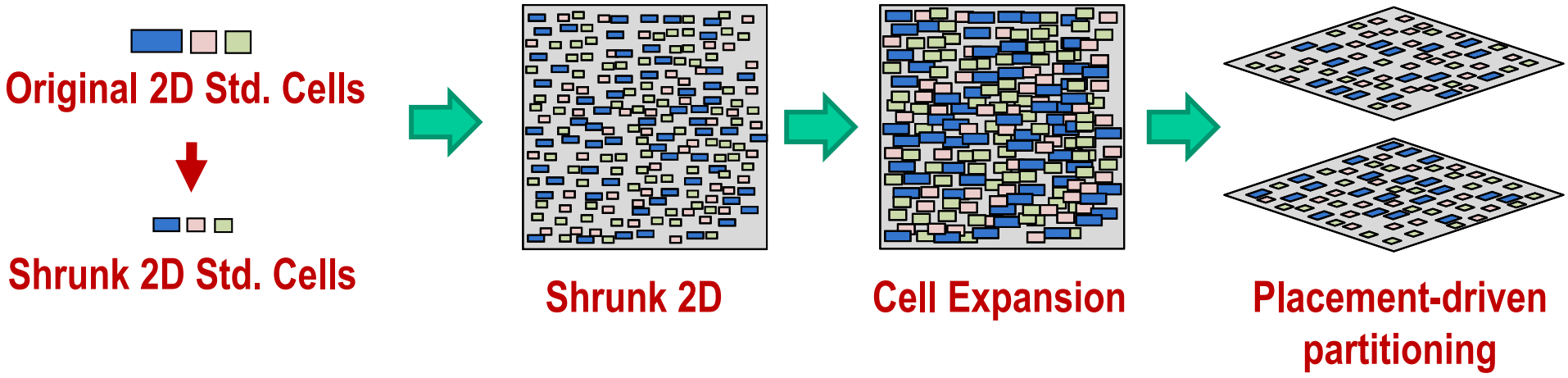


Tier 3

Beating Commercial 2D First Time Ever

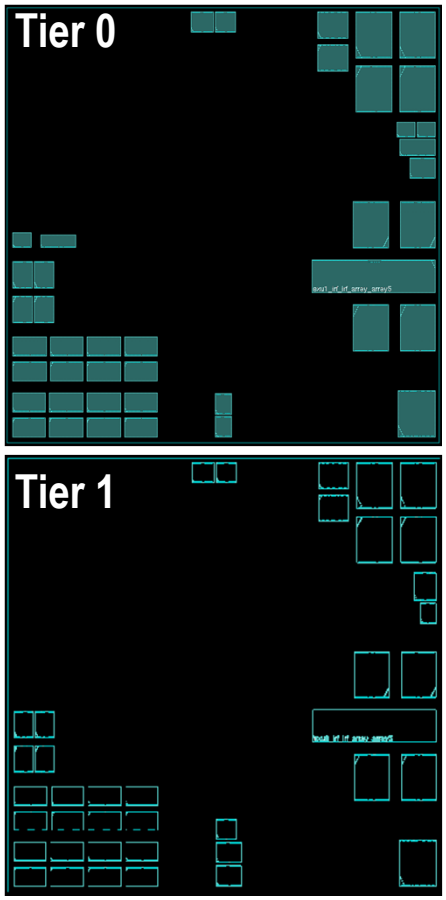
(PI: Sung Kyu Lim, GRC-CADT 2239)

- "Shrunk 2D" flow [ISLPED'14]
  - Reduce footprint, cell, and interconnect by 50%
  - Perform 2D place/route using a commercial tool
  - Repopulate, partition, placement repair, and detail route
- Transferred to
  - Qualcomm (2012), UC San Diego (2014), ARM (2015), IMEC (2015), GlobalFoundries (2015)

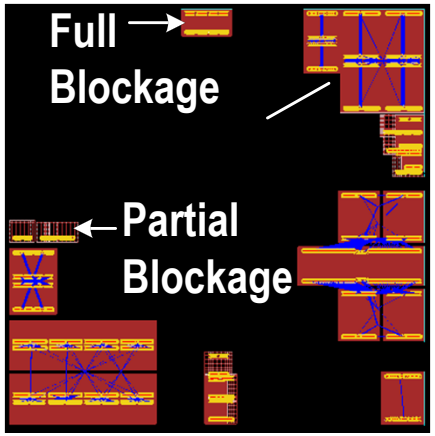


Handling Macros

(PI: Sung Kyu Lim, GRC-CADT 2239)

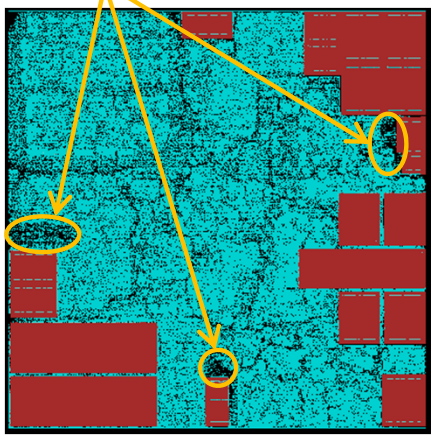


1. Pre-Placed Memory

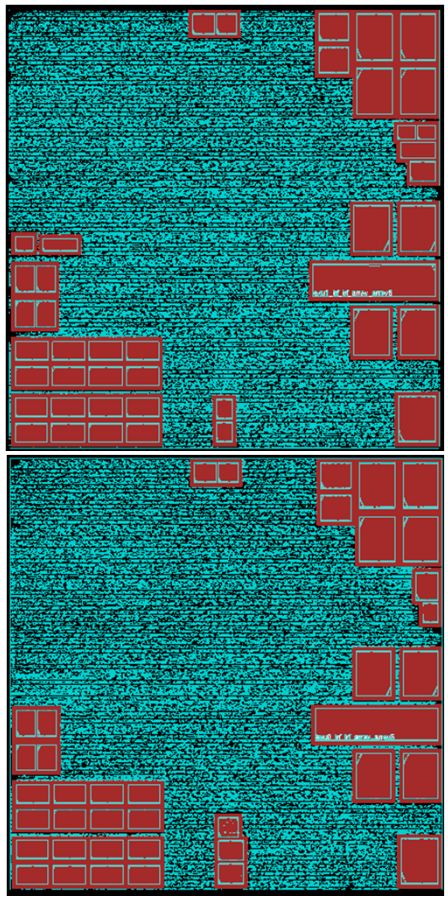


2. Memory Projection

reduced placement density over partial blockages



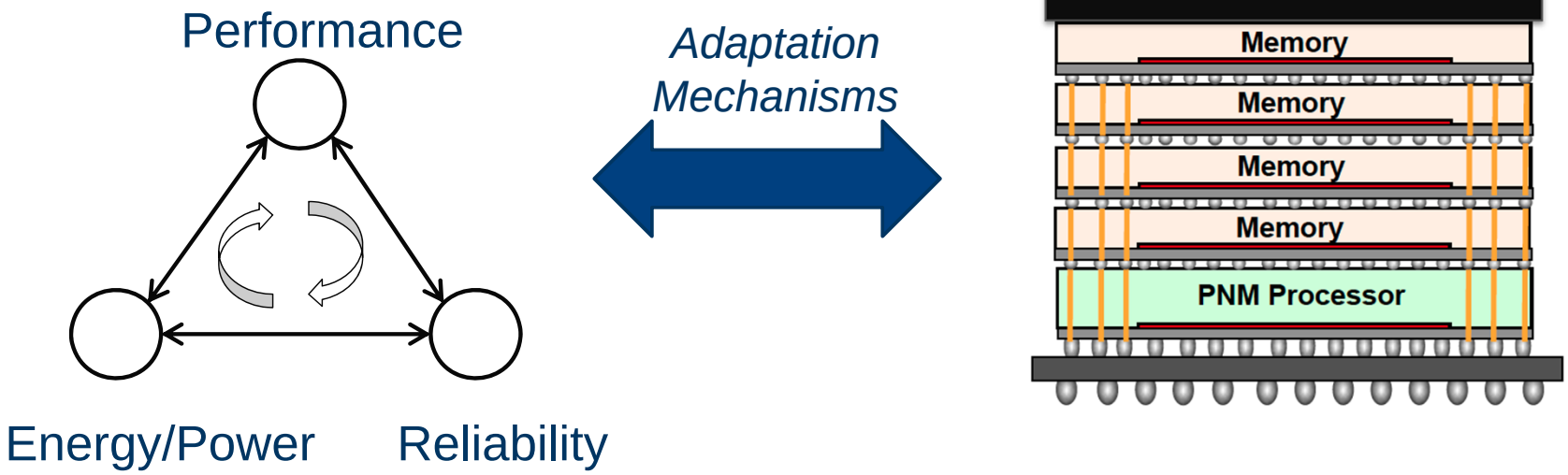
3. Shrunk 2D P&R



4. Tier Partitioning

Exploration of Adaptive 3D Many Core Architectures

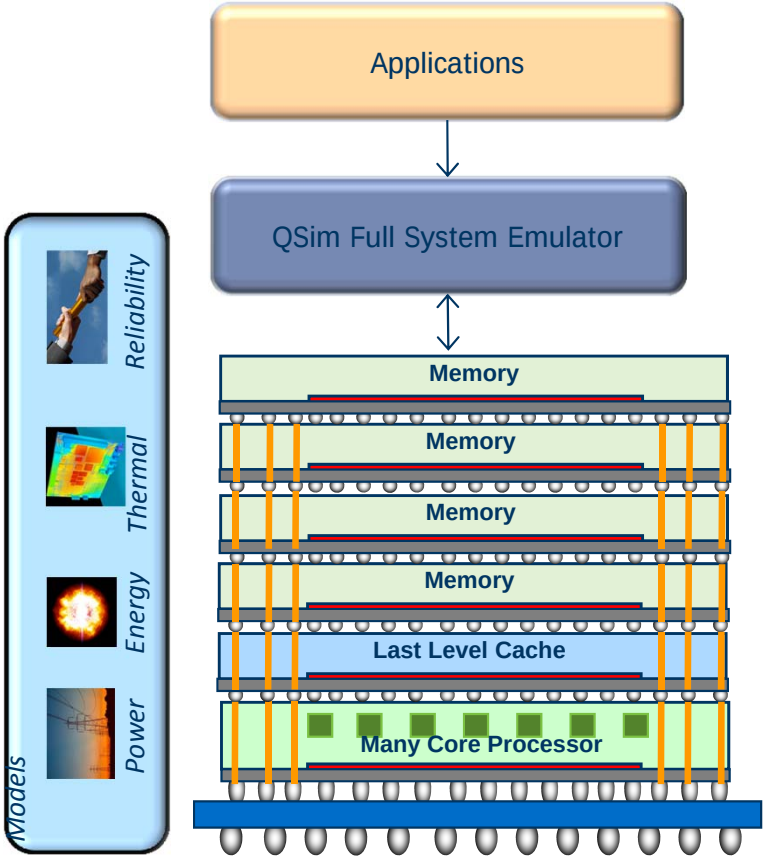
Goal: Sustaining Performance Implications of Moore's Law
Challenge: Impact of physical phenomena on system performance
Solution: Adaption mechanisms to extend voltage-frequency operating range of 3D many core processors



PIs: Sudhakar Yalamanchili and Saibal Mukhopadhyay
Students: William Song (SRC Fellow), He Xiao, Wen Yueh
Internships: IBM (2014), Intel (2014)
Liaisons: V. De (Intel), R. Rao (IBM)

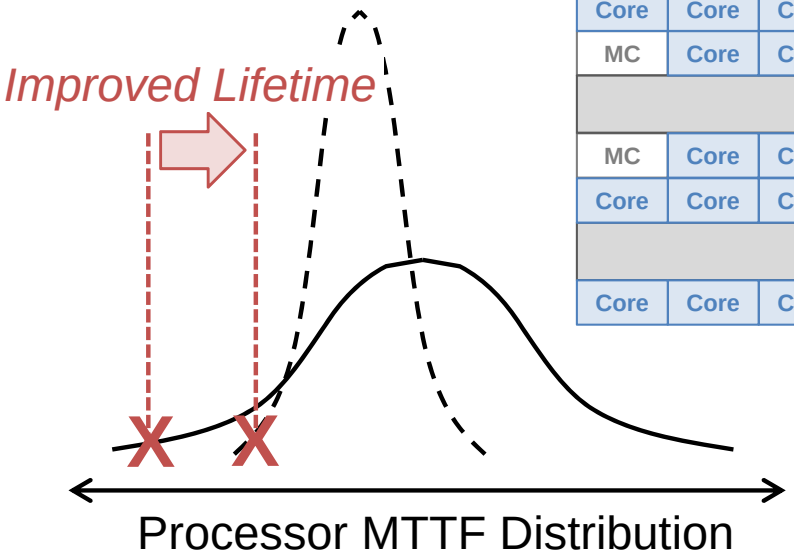
Full System Architecture-Application-Physics Co-Simulation

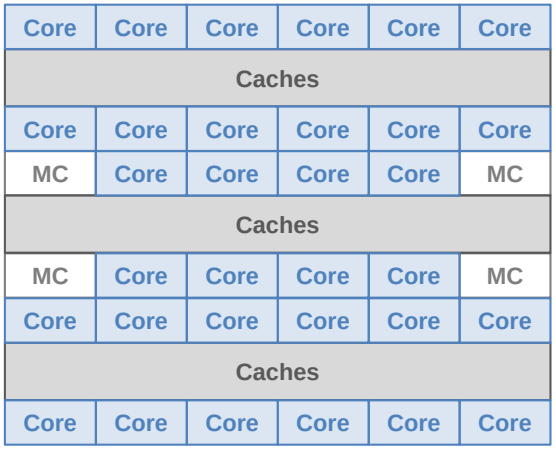
- Completion of a full system open source modeling environment for 3D architectures
  - + Power delivery network (PDN) models
  - + New thermal field models
  - + Integrated 3D models including cooling
  - + 3D system architecture models
  - + Improved temperature-delay model for SRAM (+) and eDRAM (+)
    - FinFET and Planar device models (+)
  - + Proposed SRAM adaptation mechanisms
  - + Improved 3D system architecture model
  - + Short Stack 3D architecture concept
  - + System Level Impact of IVR
  - + Multicore Lifetime Reliability Management



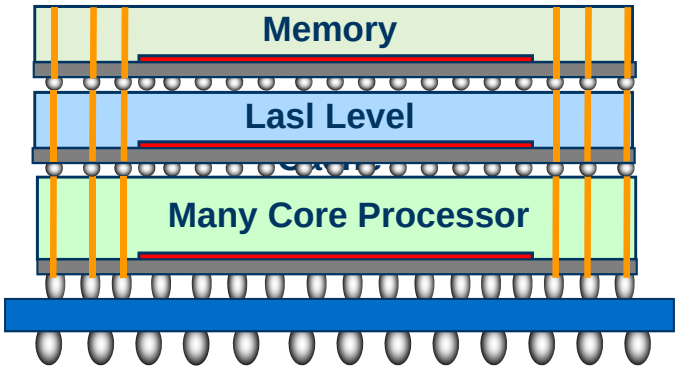
Major Program Results

1. Lifetime Reliability Management

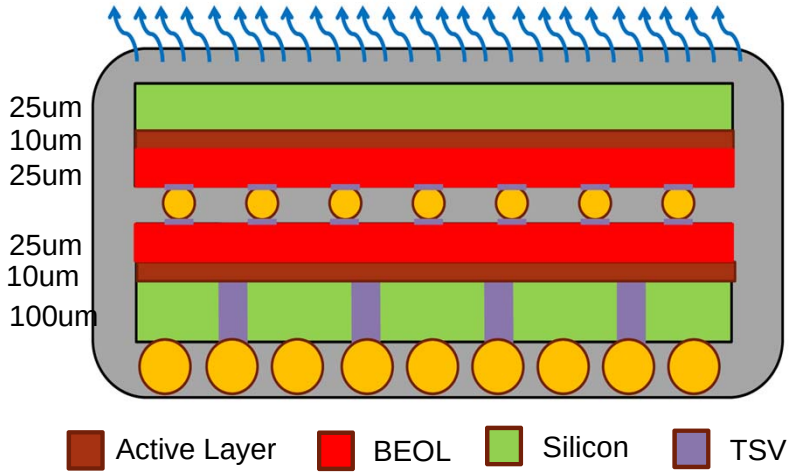




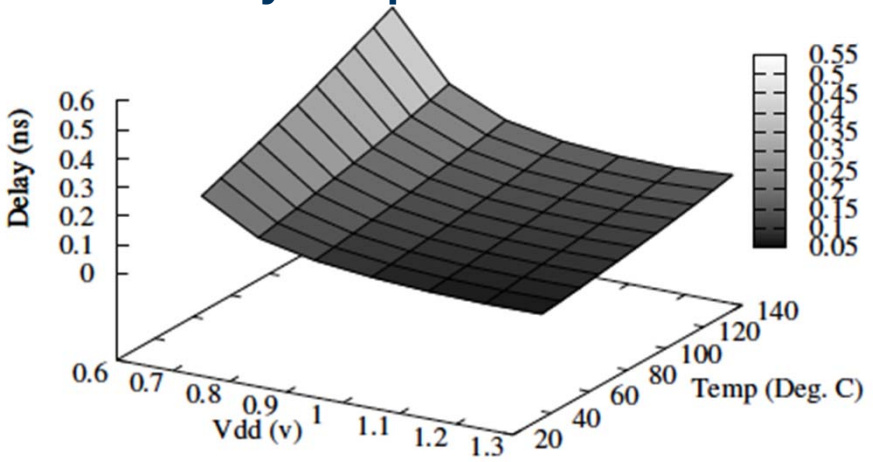
2. Adaptive Core-Cache Power Management



3. Short Stack: Multicore +Last Level Cache

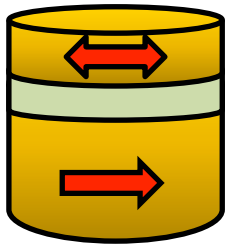


4. Thermally Adaptive Last Level Cache

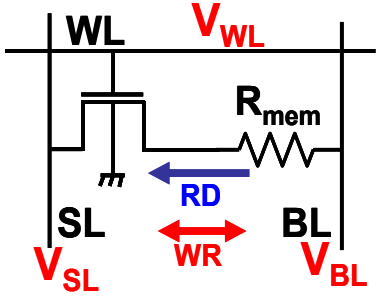


Task ID: 2493.001 **Task Period:** Nov 2013- Oct2016

Task Title: Models, Algorithms and BIST Hardware Development for Manufacturing & Characterization Tests of Spin-Transfer-Torque MRAM Arrays



Storage Element



Bitcell

Array Level

- Variations and Defects
- Fault Models
- BIST and test coverage

Task Leader: Arijit Raychowdhury

Custom Funding: Intel

Industry Liaisons: Helia Naeimi, Suriyaprakash Natarajan (Intel)

Science Area: Computer Aided Design & Test Sciences

Students: Abhinav Parihar, Ashwin Chintaluri

Internships: Intel (2014)

Deliverables and Status

Key Deliverables and Status

Year 1:

- ✓ Build atomistic models for spin dynamics with current injection and extract model parameters for circuit level evaluation.
- ✓ Deduce fault models (RD/WR/RET) for both variation and defects

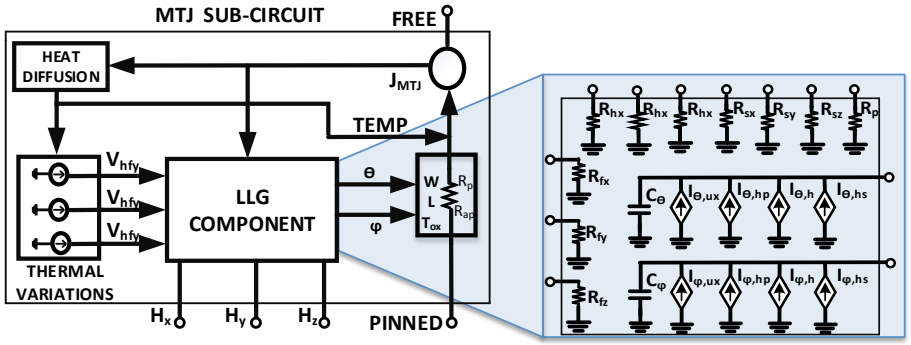
Year 2:

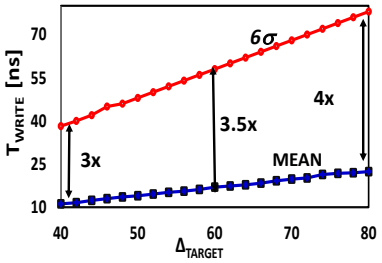
- ✓ Develop design of BIST and DfT circuits to allow statistical data collection.
- Initial exploration of regression models for fast and efficient testing of retention time using short-pulse measurements.

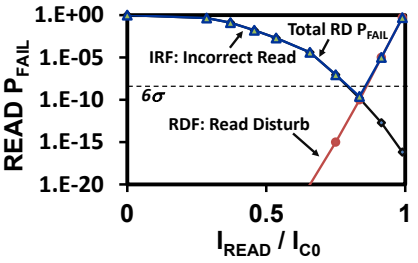
Year 3:

- Investigate regression models along with extreme-value statistical models to allow P_{FAIL} data collection at short pulses and correctly extrapolating them to longer pulse widths for correct determination of Δ. Calibration of proposed model with measurements (joint work with Intel).
- Exploration of novel STTRAM architecture for yield, and resiliency through on-line tests and adaptation schemes.

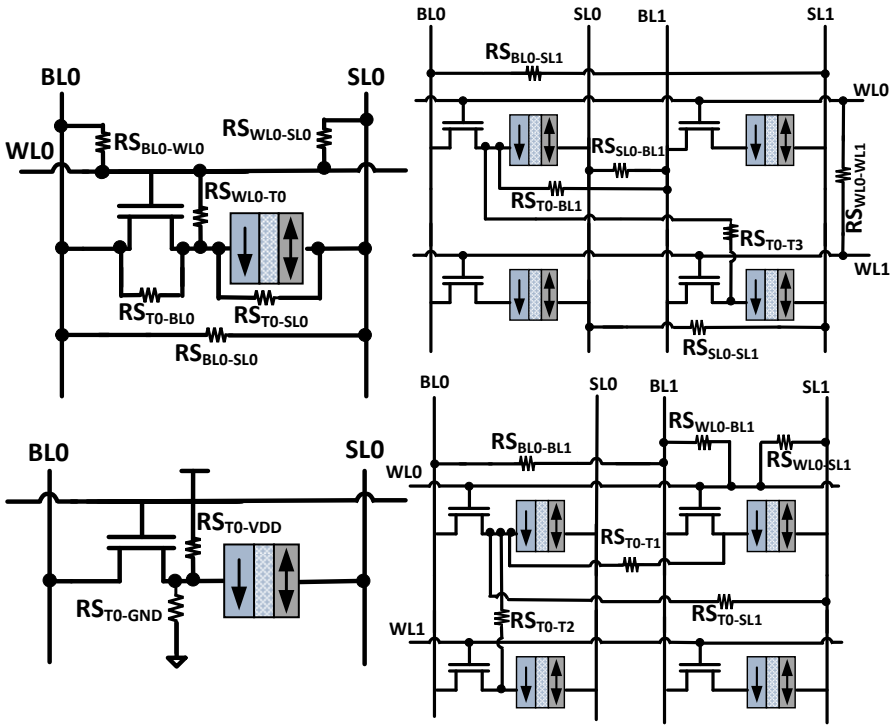
Key Results





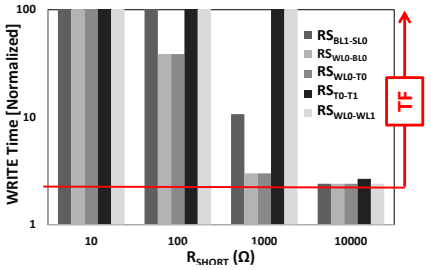


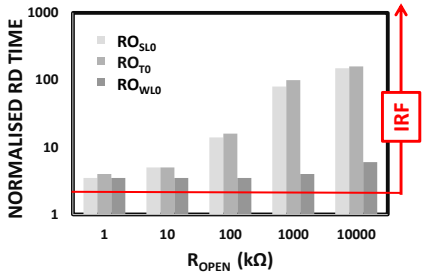
STTRAM Model from devices to arrays



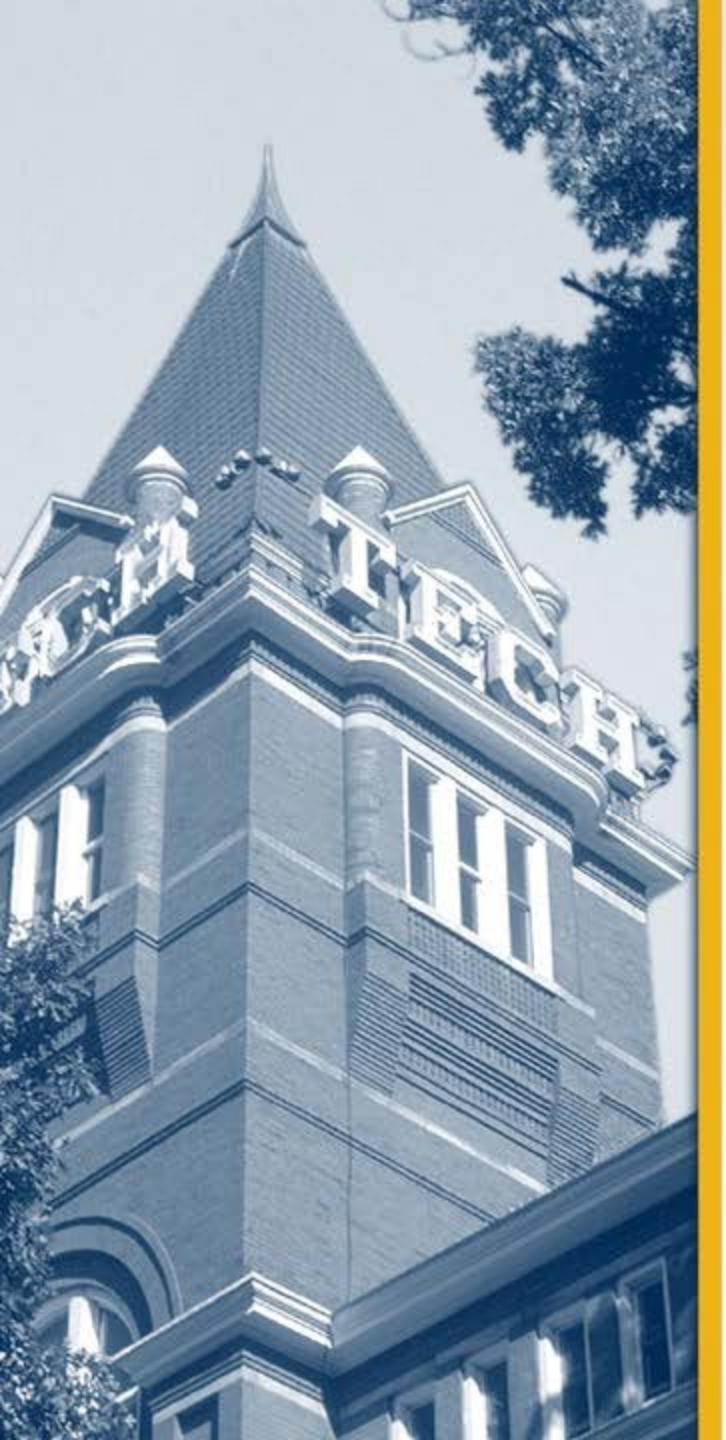
Inter and intra-cell Defect Models

Analysis of variations in RD, WR and Retention





1. Effect of defects on RD, WR in arrays
2. Sensitivity Analysis of defects
3. Data pattern dependence and test patterns necessary to activate defects.



SRC Research Overview: Devices, Circuits, Interconnects

Muhannad Bakir
Hua Wang
Azad Naeemi
John Cressler

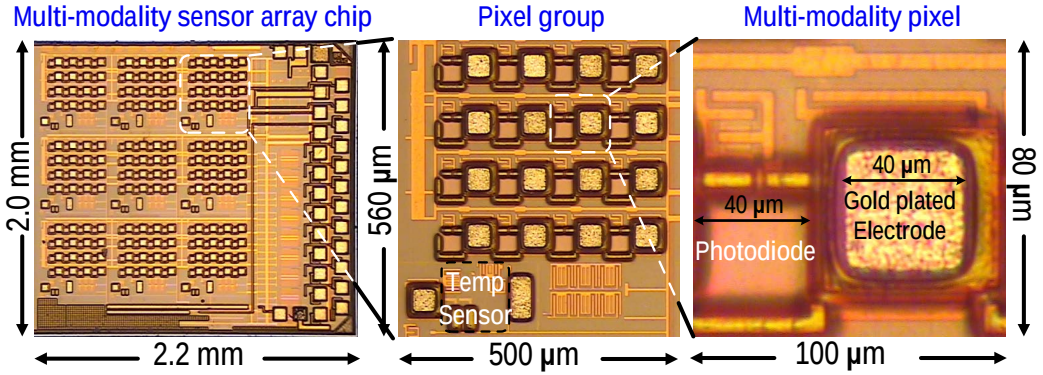
Georgia Institute of Technology

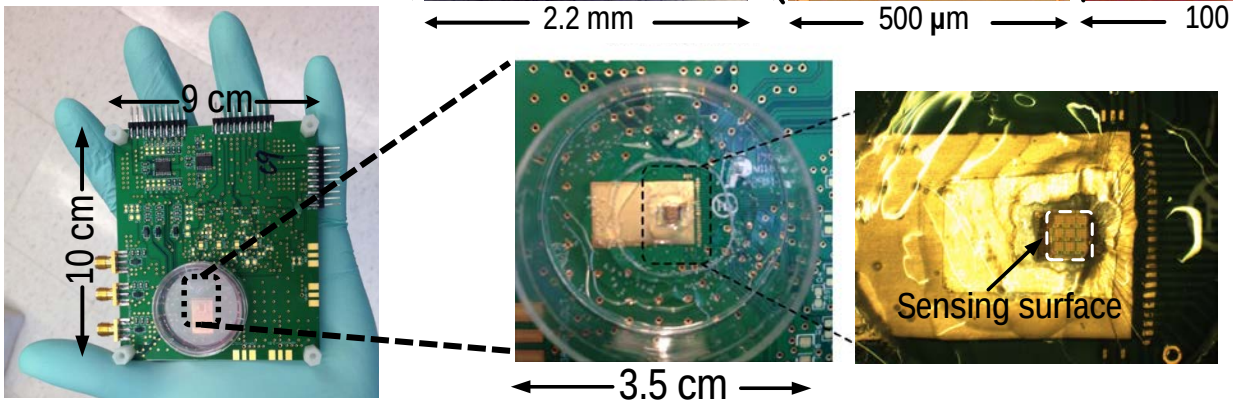
SRC

SRC Semiconductor Synthetic Biology

Hua Wang, ECE

- SRC GRC Semiconductor Synthetic Biology (SemiSynBio) Program (Task ID: 2484.001).
- GT PI: Hua Wang (ECE) and Co-PI: Mark Styczynski (ChBE)
- Motivation: Existing solid-state biosensors are mostly of single-modality and cannot capture the complex and multi-physical cell responses. This substantially limits the capability of cell-based arrays.
- Achievements: World-first multi-modality cellular sensor array in standard CMOS for chemical screening and drug development application (*J. Park, et al., IEEE ISSCC 2015*).



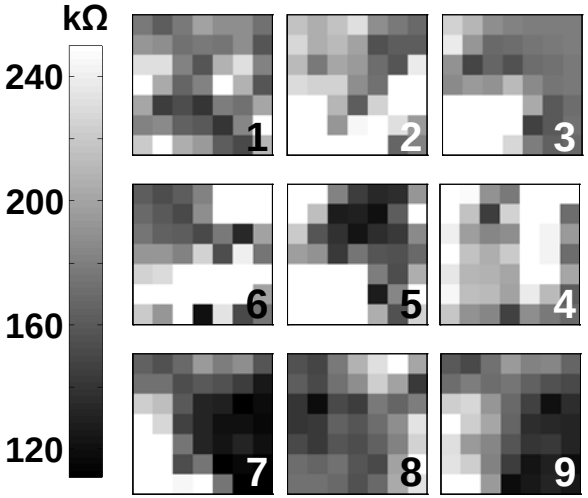


- CMOS sensor chip in a standard cell culture plate
- I/O pads and wire-bonds are sealed by PDMS packaging.

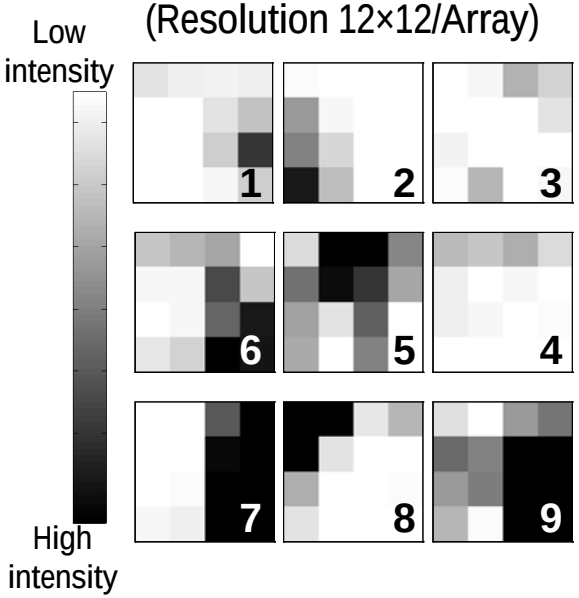
SRC Semiconductor Synthetic Biology

- Biological multi-modality measurement: Impedance + optical shadow imaging

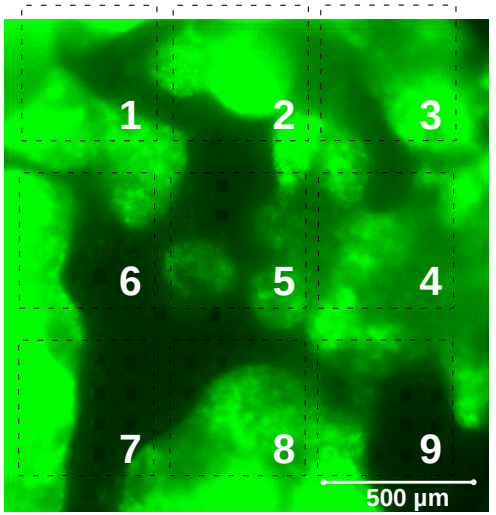
Electrical Impedance Mapping (Resolution 21×21/Array)



Optical Shadow Image (Resolution 12×12/Array)



Fluorescent Image of the Entire Multi-Modality Sensor Array



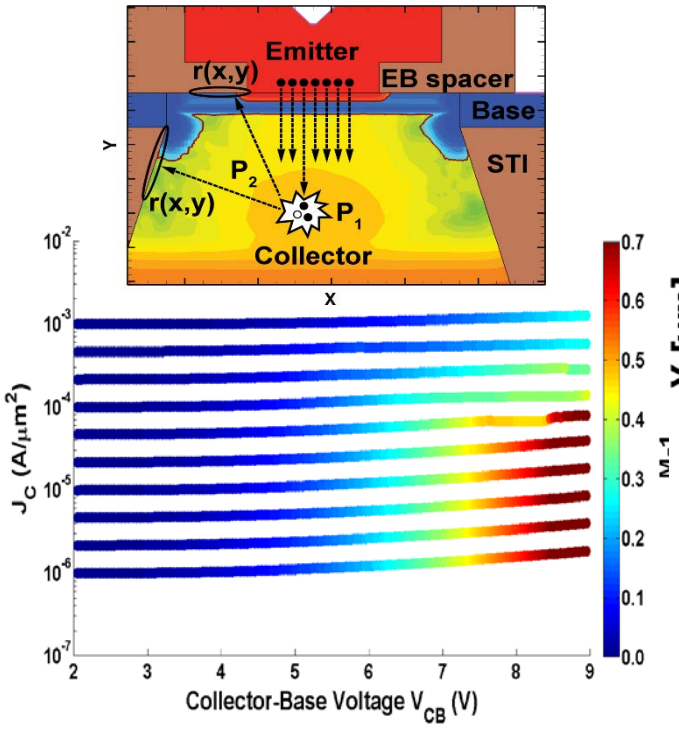
- Mouse Neurons labeled with green fluorescent protein are used as the sensing cells
- The optical shadow image (middle) closely matches the fluorescence image (right)→ Showing the correct 2D distribution of the cells.
- Electrical impedance imaging measures the cell attachment, which cannot be captured by the optical image → Providing orthogonal cellular information.

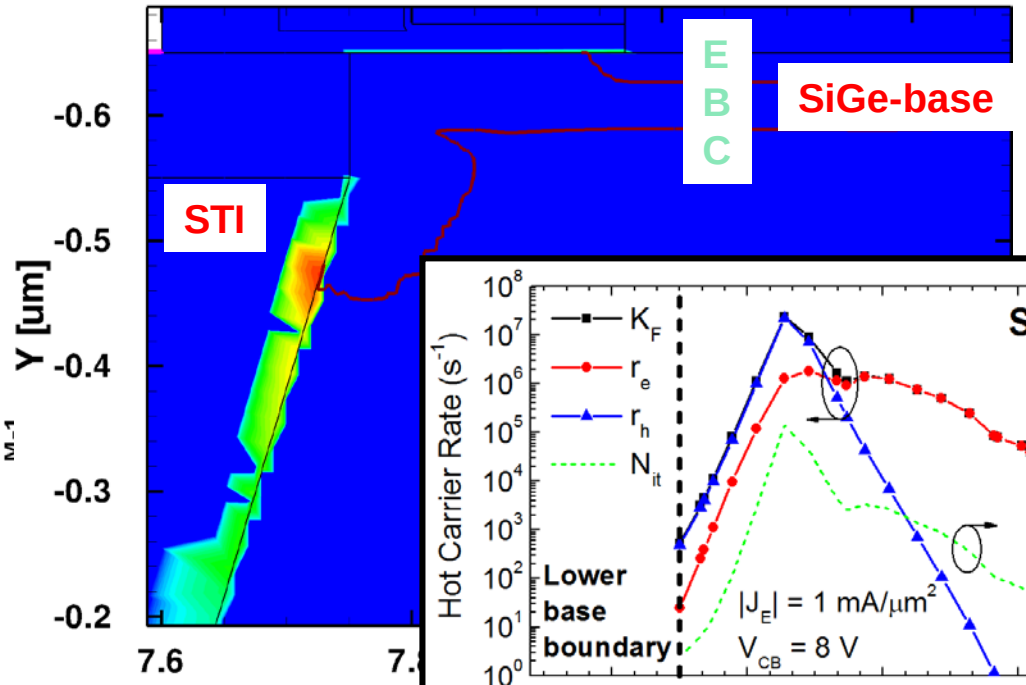
J. Park, T. Chi, J. Butts, T. Hookway, T. C. McDevitt, and H. Wang, "A Multi-Modality CMOS Sensor Array for Cell-Based Assay and Drug Screening," *IEEE ISSCC*, Feb. 2015.

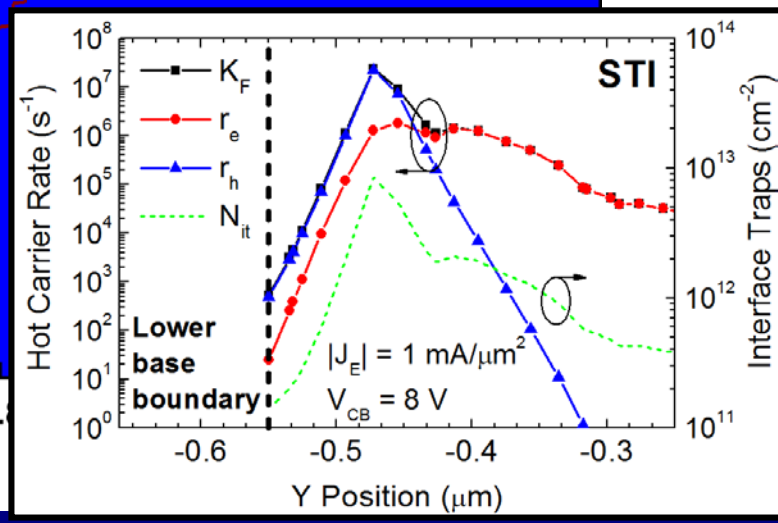
John D. Cressler

- **Physics and Modeling of SiGe HBT Reliability**
  - **Analog and Mixed-Signal Thrust: GRC Task 2160 (TI mentored)**
- **Aging-Enabled Compact Models for SiGe Circuits**
  - **Analog and Mixed-Signal Thrust: GRC Task 2388 (TI mentored)**

Goal: Empower Circuit Designers By Developing Tools to Quantitatively Predict End-of-Life Performance of Mixed-Signal SiGe HBT Circuits





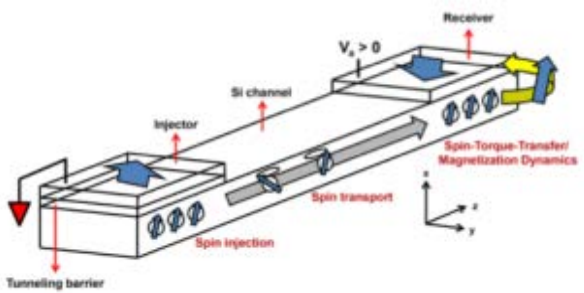


Beyond CMOS Material, Device, and Circuit Research SRC-MSR (Intel) and SRC-NRI (INDEX)

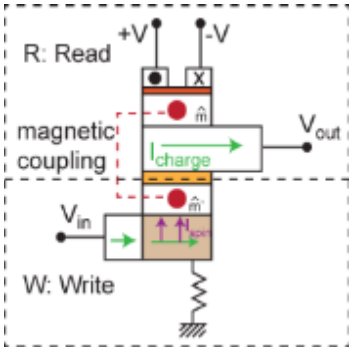
Azad Naeemi, ECE

- Compact physical models are being developed and used to optimize/benchmark emerging devices, to guide technology development, and to formulate novel circuit concepts.

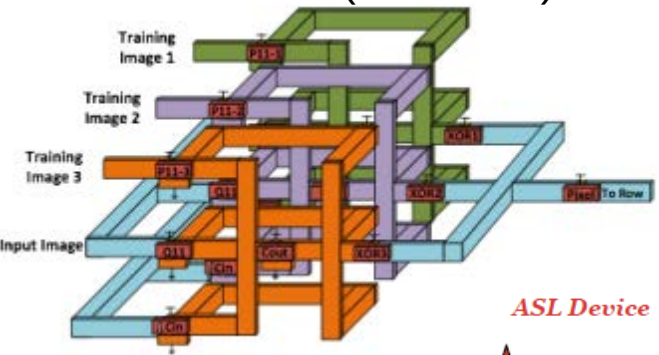
Si Interconnect for All-Spin Logic (*IEEE T-MAG 2014*)



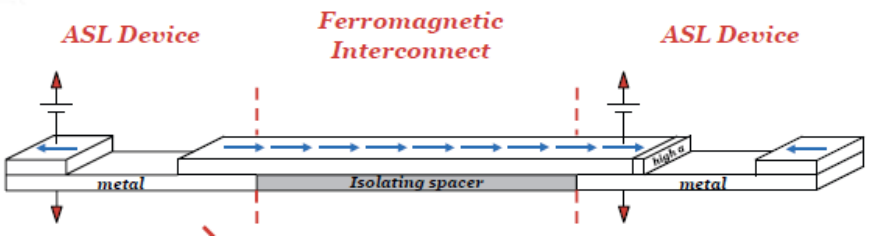
Giant Spin Hall Current Controlled Logic (NRI-INDEX)



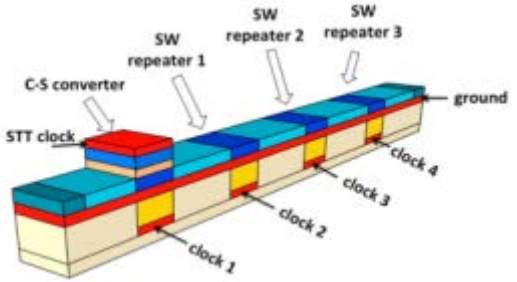
Novel Circuit Concept for Pattern Recognition Using spintronic Devices (submitted)



Domain Wall Automotion Interconnect (*IEEE JxCDC*)

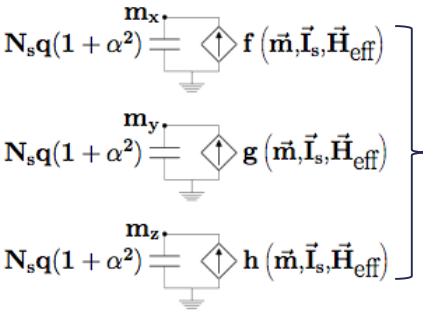


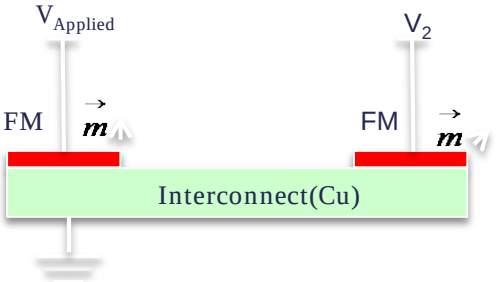
Novel Spin Wave Circuit Concept (*Nature Scientific Report*)

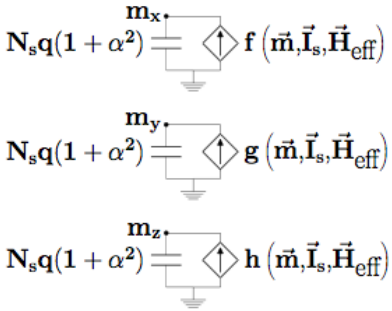


Example: Complete SPICE Model for Spintronic Devices/Circuits

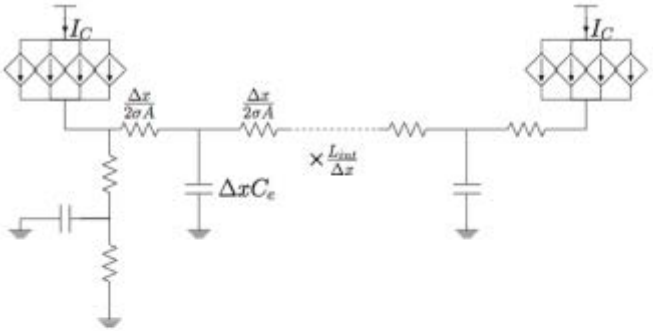
Stochastic LLG for nanomagnet dynamic

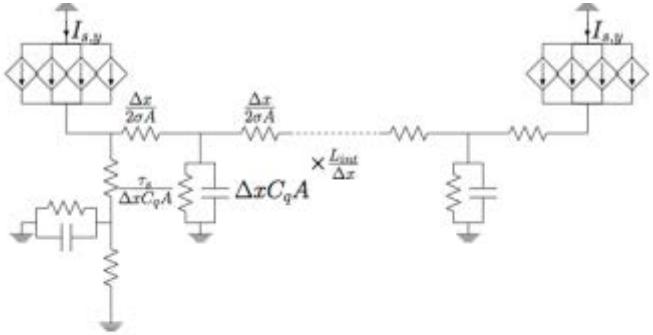






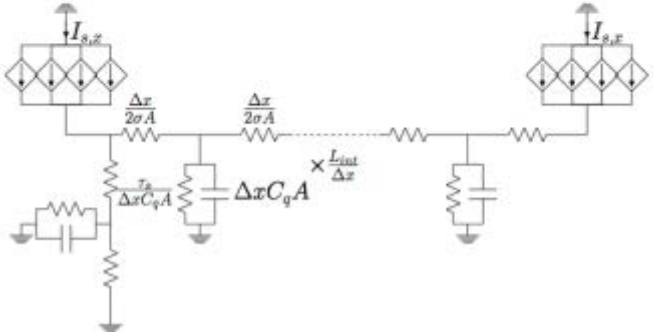
Describes the electric voltage and current

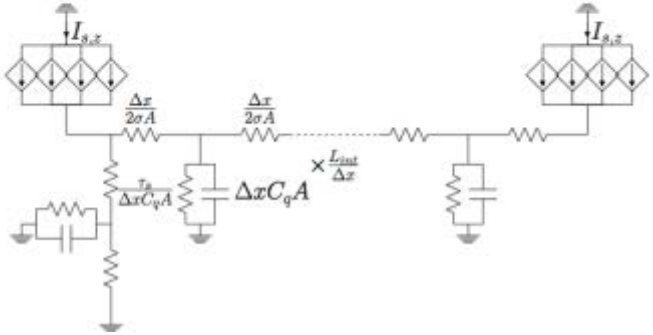




Describes the the x component of the spin current

Describes the the y component of the spin current





Describes the the z component of the spin current

IEEE Trans. Electron Devices, May 2014.

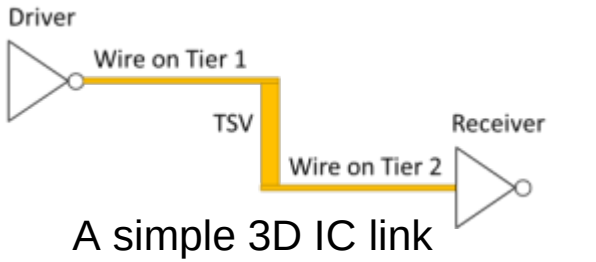
Impact of TSVs and Wires on 3D IC Interconnect Links

Muhannad S. Bakir, ECE

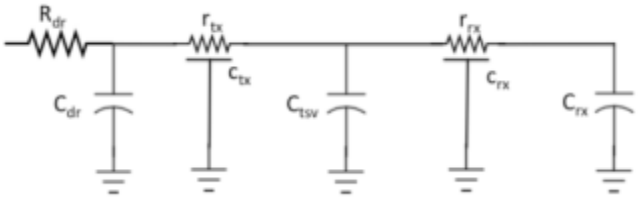
Research motivation and goal:

- ❑ Understand how TSVs and wires impact 3D IC link performance.
- ❑ Analyze the key bottle necks limiting 3D IC link performance with modeling and experiments.

Modeling



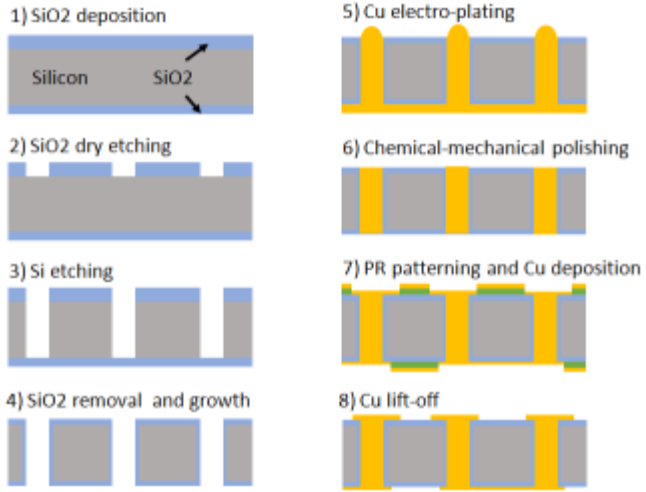
A simple 3D IC link



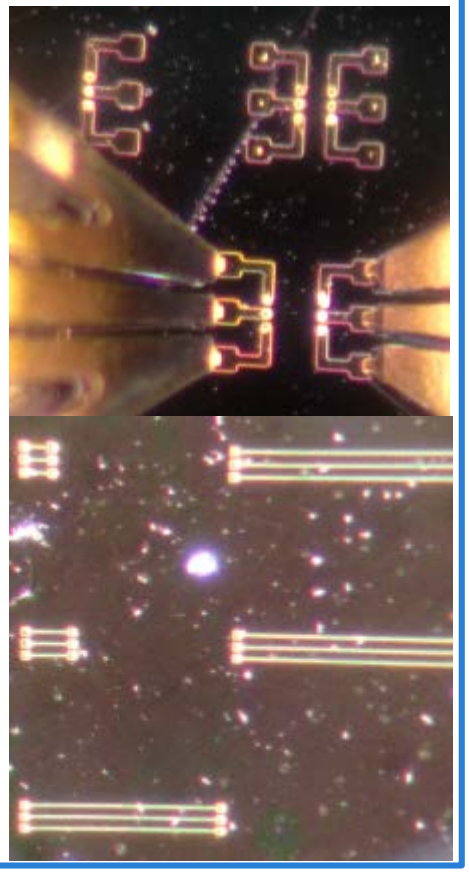
Circuit Model for the 3D IC link

Experiment

Fabricated structure



Fabrication process

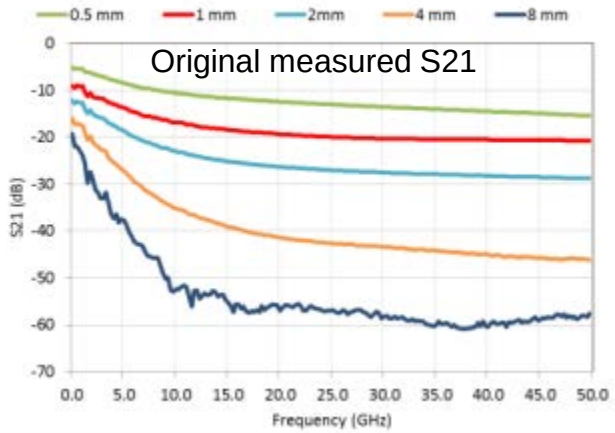


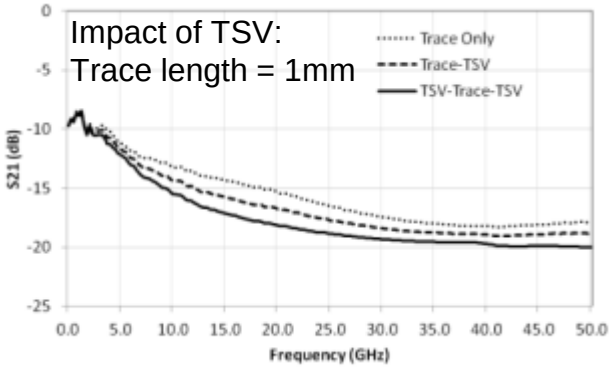
Impact of TSVs and Wires on 3D IC Interconnect Links

Conclusion:

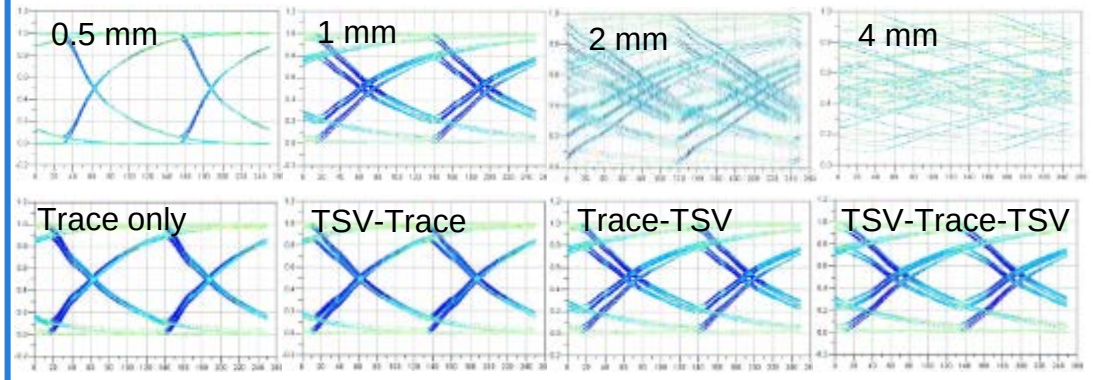
- ❑ Impact of TSV is less significant when it is placed close to the driver
- ❑ Driver side resistance and TSV capacitance dominates 3D IC link delay

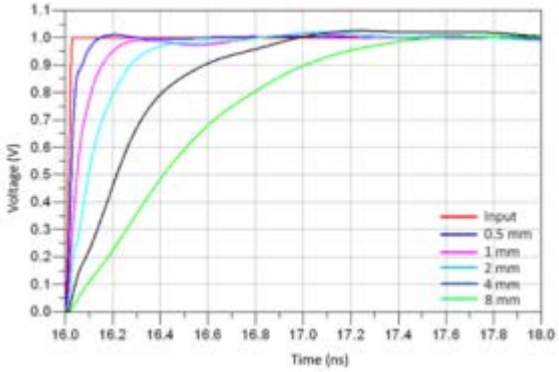
Frequency Domain

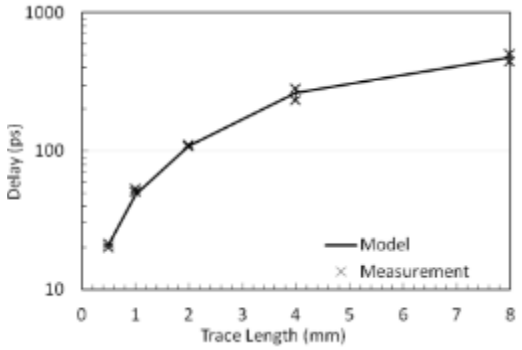




Time Domain*

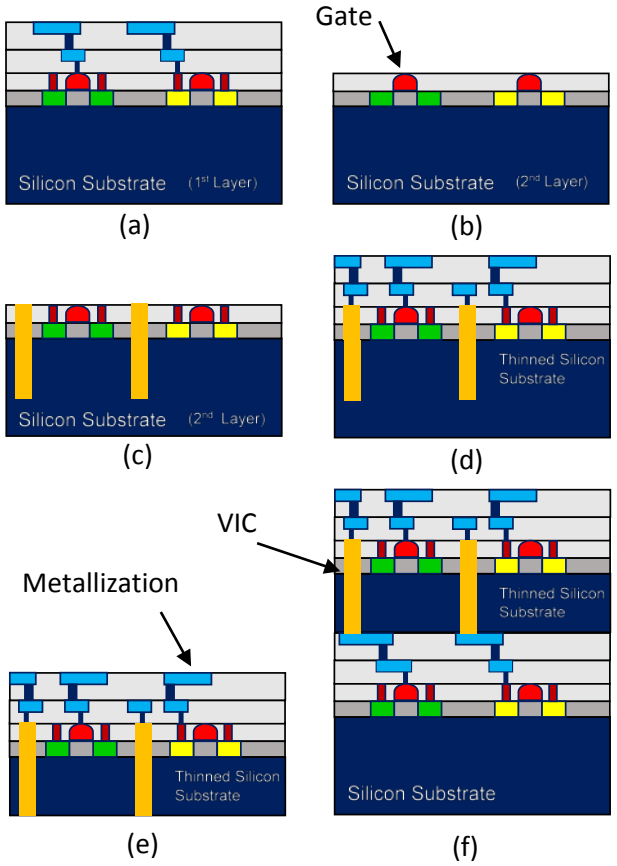




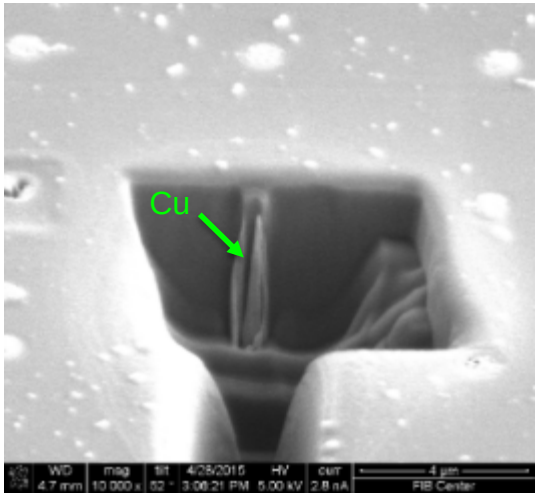


*data rate at 8 Gbps. Trace length = 1 mm for eye diagrams at second row

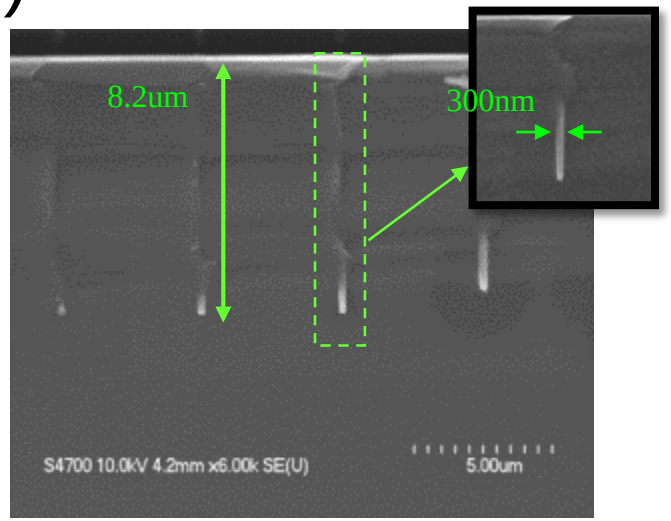
High Aspect Ration Nano-scale Vertical Inter-tier Connection (VICs)



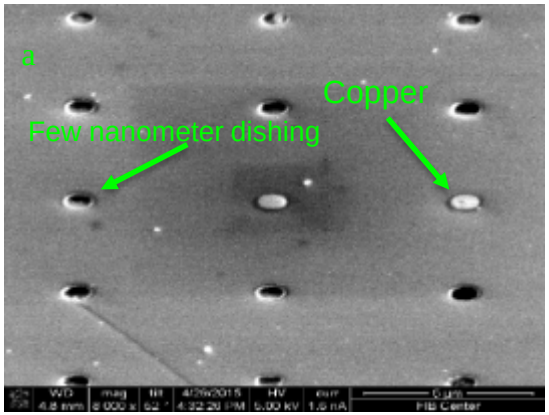
The schematic of our sequential 3D integration technology. a) Fabrication of 1st layer (the most bottom layer), using conventional CMOS process. b) Fabrication of the second layer using conventional CMOS process. c) Integration of the VICs. d) Continuing metallization process for the 2nd layer. e) Thinning down the 2nd silicon substrate. f) Stacking up the 2nd layer.

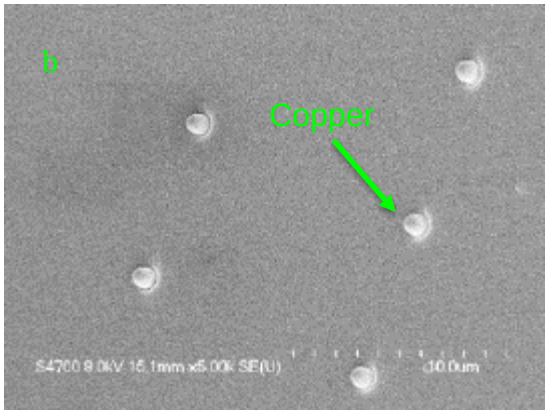


FIB cross-sectional view of void-free Cu filled 700nm diameter VIC.



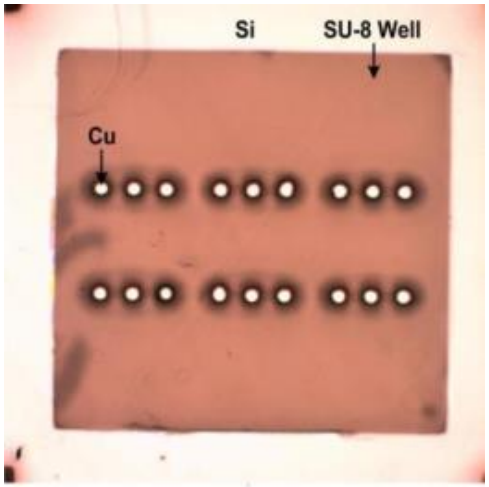
Cross-sectional view of a cleaved sample, shows void-free copper filled 300nm diameter VICs with 27:1 aspect ratio.

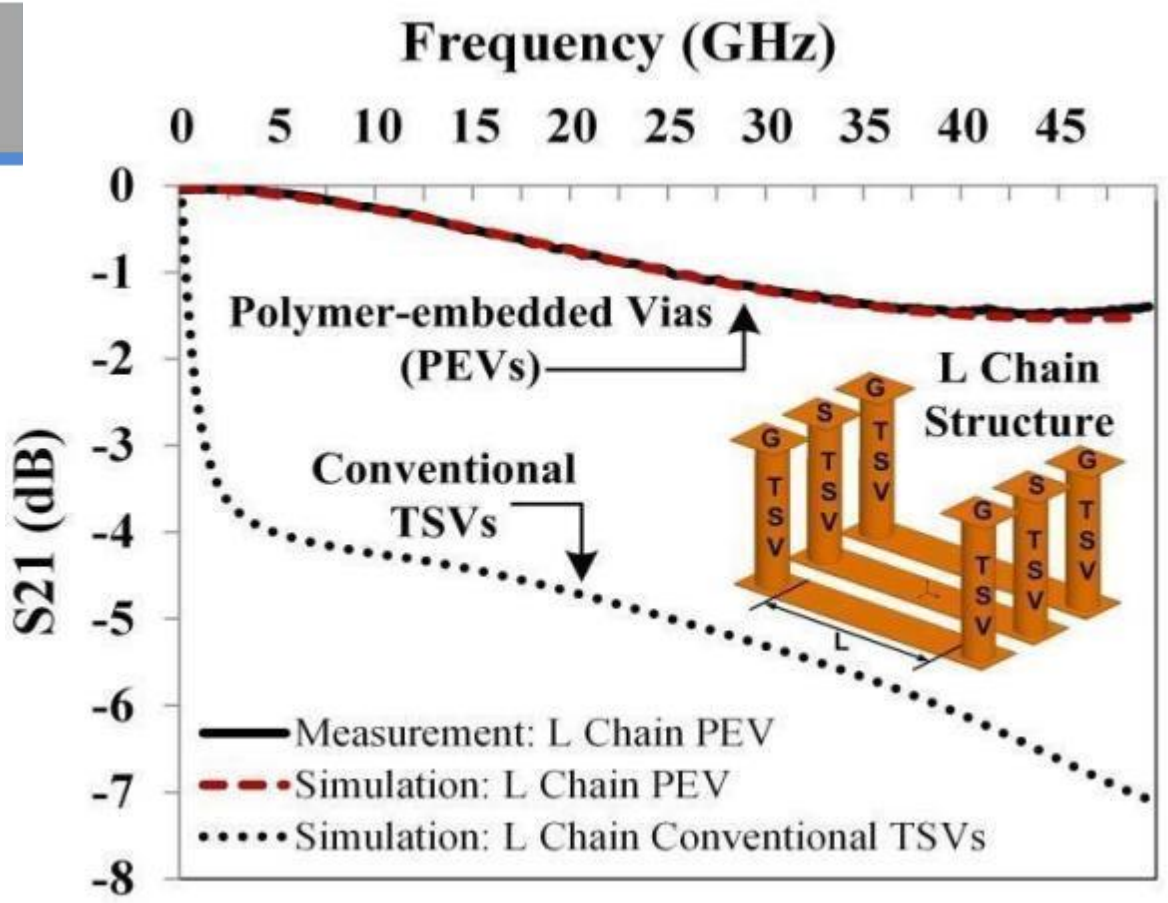




a) Top-view SEM image of VICs. The excessive electroplated copper layer is polished off using CMP process and the copper filling is visible. b) The substrate is back etched, accessing the bottom of VICs for electrical characterizations and the SEM images shows the copper filling is void free at the bottom.

Polymer-embedded Vias for Superior Electrical Performance



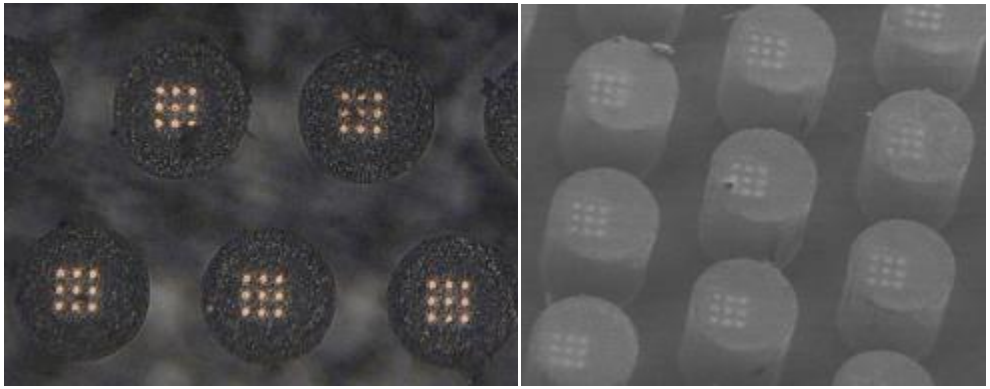


TSV de-embedding required to understand losses and extract parasitics of a polymer-embedded via.

Integration of Microfluidic Cooling With 3D ICs

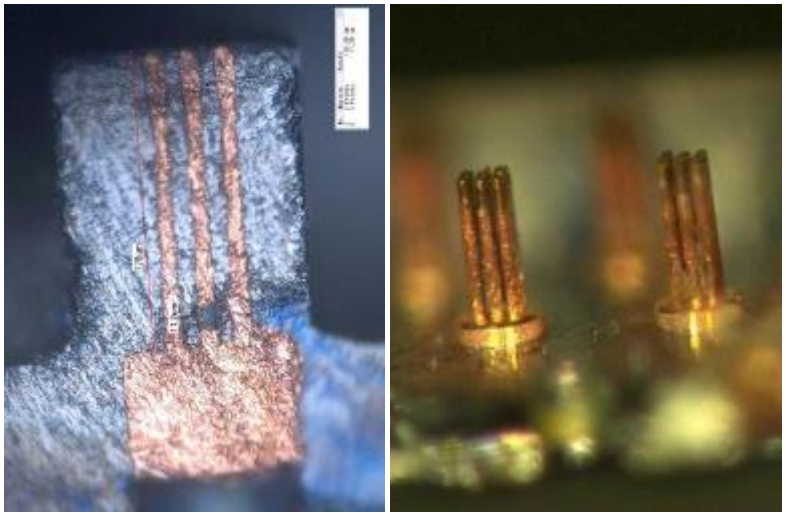
- Silicon micropin-fins with embedded TSVs

Top and angled view

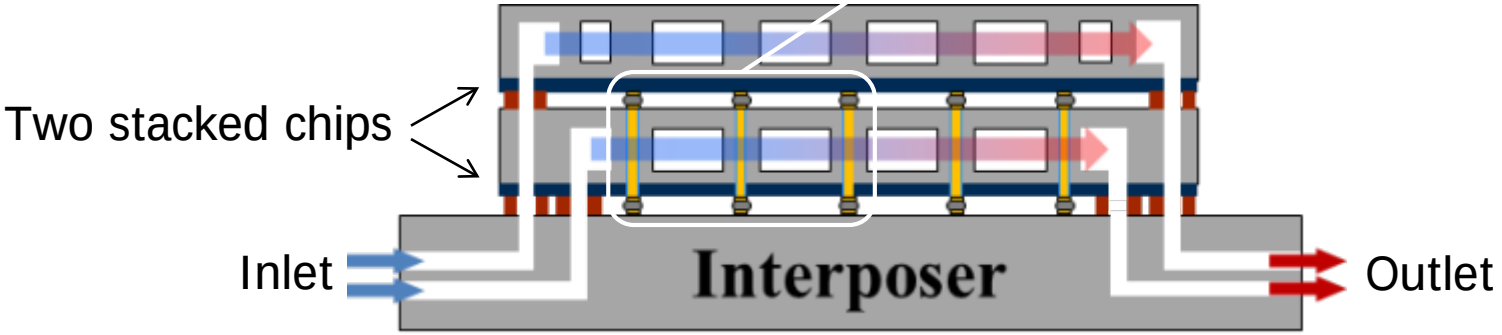


Circular micropin-fin heat sink embedding 9 TSVs

Cross-sectional and side view



Bottom-up electroplated TSVs (18:1 AR)



"Interlayer Microfluidic IC Cooling Integration with Through Silicon Vias", Ashish Dembla, Yue Zhang and Muhannad S. Bakir, IITC 2012

30 Years of Collaboration with SRC

- Two Centers: IFC (10 Univs) and IPC (5 Univs)
- $103M in grants, contracts and fellowships to GT
- 44 patents
- 95 Graduate and 12 post docs supported
- Extensive research program for UG students through ORS
- Several major SRC and national/international awards to GT faculty

Thank you!

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