Poster Introductions

Session I: Convolutional Networks for Co-Optimization of IVR and Embedded Inductor for 2.5D Packaging

Student(s): Hakki M. Torun, Huan Yu **Faculty:** Madhavan Swaminathan

❑ Objective:

- Develop an efficient & accurate co-optimization framework for IVR & embedded inductors
- Quantify the advantage of co-optimization over two-step optimization

❑ Technical Approach:

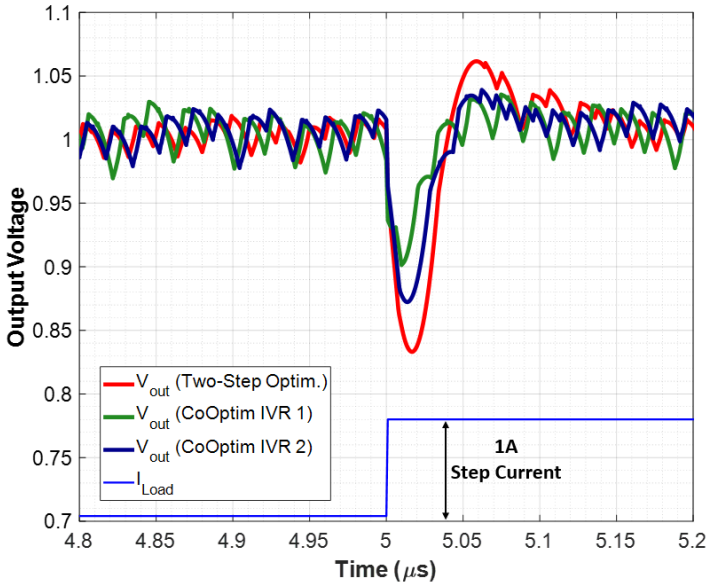
- We propose a new convolutional network-based model to learn inductor frequency response using limited number of data.
- Derived model is then used to generate 5-dimensional Pareto front of the IVR.

❑ Latest Results:

Achieved up to

- **51.5% reduced inductor area**,
- **40.9% reduced voltage droop**
- **26.1% reduced settling time**

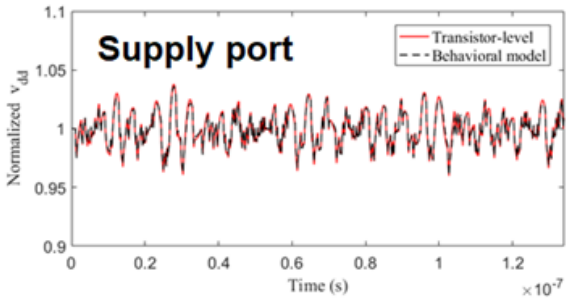
compared to two-step optimization.

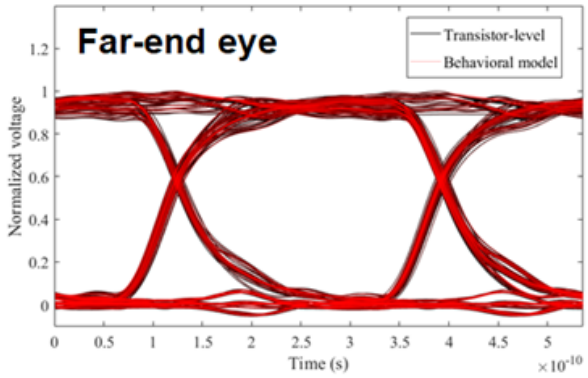


Behavioral Modeling of I/O Drivers Using Neural Networks

Students: Huan Yu, Mourad Larbi (postdoc)
Faculty: Prof. Madhavan Swaminathan

- Objective:
  - Develop behavioral model (BM) for complex I/O driver circuit that
    - Protects IP and is superfast.
    - Is significantly more accurate than IBIS.
    - Is parameterized and compatible with existing tools.
- Technical Approach:
  - The nonlinear dynamic behavior of I/O drivers is captured with sub-models and weighting functions using machine learning techniques.
- Latest Results:
  - Multi-port BM for SI&PI simulation with ~300X speed-up.



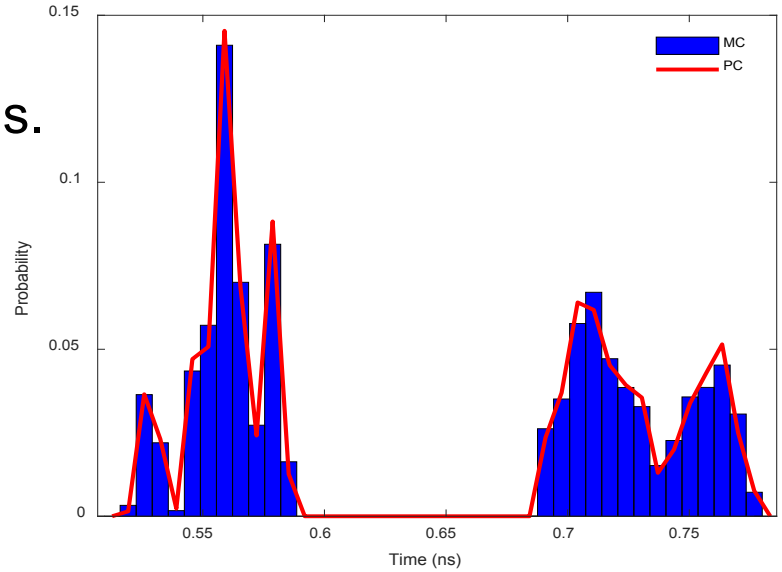


This work was funded by the National Science Foundation under Grant No. CNS 16-24731 and the industry members of the CAEML IUCRC.

Session I: Jitter and Eye Estimation in High-Speed Channels

Student(s): Majid Ahadi, Faculty: Madhavan Swaminathan

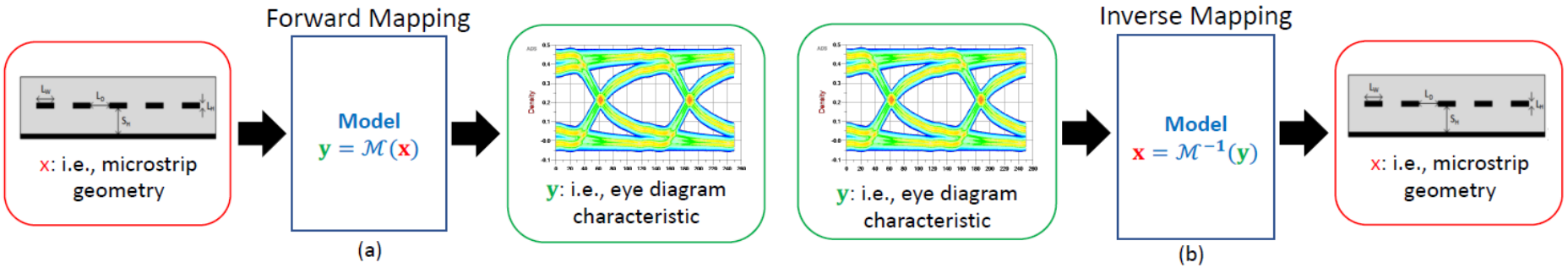
- Objective:
  - Accurate eye analysis for non-LTI high-speed channel using surrogate models.
  - Saving computation costs in eye analysis with BER < 10^{-12}
- Technical Approach:
  - Surrogate models based on modified Polynomial Chaos theory.
  - Applied to receiver voltage and directly to jitter.
- Latest Results:
  - High accuracy in jitter and eye analysis.
  - ~16X speedup.



Session I: Inverse Design of High-speed Links with Machine Learning

Student(s): Majid Ahadi, Postdoc: Kallol Roy,
Faculty: Madhavan Swaminathan

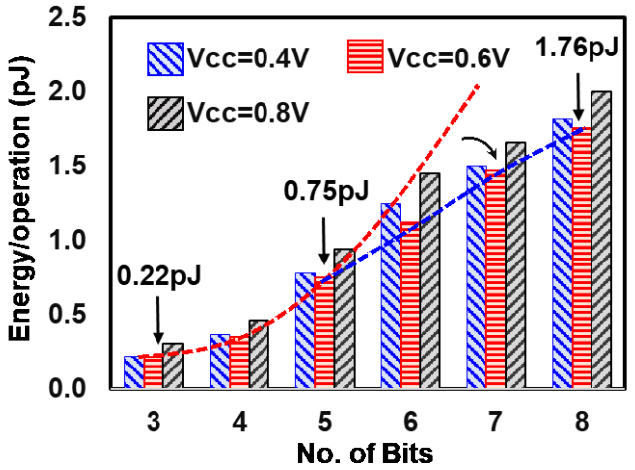
- Objective:
  - Finding suitable design parameters from the desired characteristics.
  - Saving time and costs in the design process.
- Technical Approach:
  - Least square support vector machine (LS-SVM)
  - A tradeoff between accuracy and overfitting.
- Latest Results:
  - Preliminary results for the design of a five channel bus.
  - Dimensions of microstrip lines are extracted from eye characteristics.



A Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Swarm Robotics

Students: Ningyuan Cao, Muya Chang Faculty: Arijit Raychowdhury

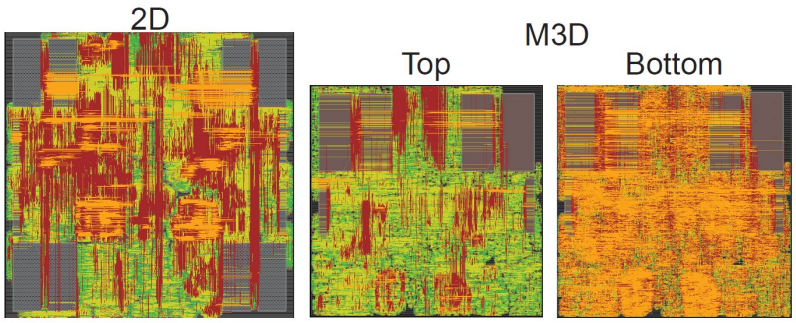
- Objective:
  - Proposed platform features accelerator supporting model-based and model-free swarm robotic applications
  - Computation is bit-precision scalable to account for varying swarm sizes
- Technical Approach:
  - Dedicated nonlinear function evaluator and linear processing unit
  - Time-domain mixed-signal 3-8b multiplication kernel
- Latest Results:
  - Supports applications such as path planning, cooperative RL and etc.
  - Achieved 8-3b 1.1-9.1 TOPS/W arithmetic energy efficiency



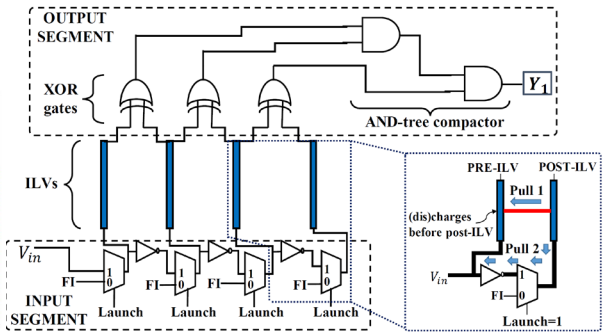
Session I: RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs

Student: Heechun Park Faculty: Sung Kyu Lim

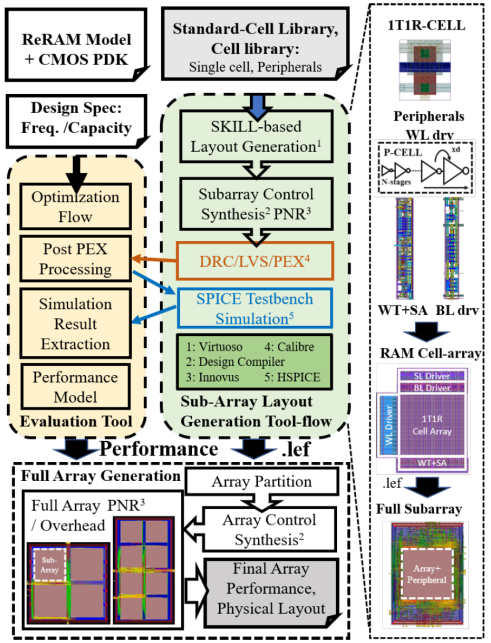
- Objective: RTL-to-GDS design flow for Monolithic 3D (M3D) IC
  - BIST for Inter-layer via (ILV)
  - ReRAM module generator
- Technical Approach
  - Shrunk-2D based M3D design + ILV-BIST insertion
  - CAD-tool-based ReRAM compiler EDA
- Latest Results
  - Better PPA with M3D + minimal BIST cost
  - EDA methodology & DSE for ReRAM array



Layouts



ILV BIST architecture

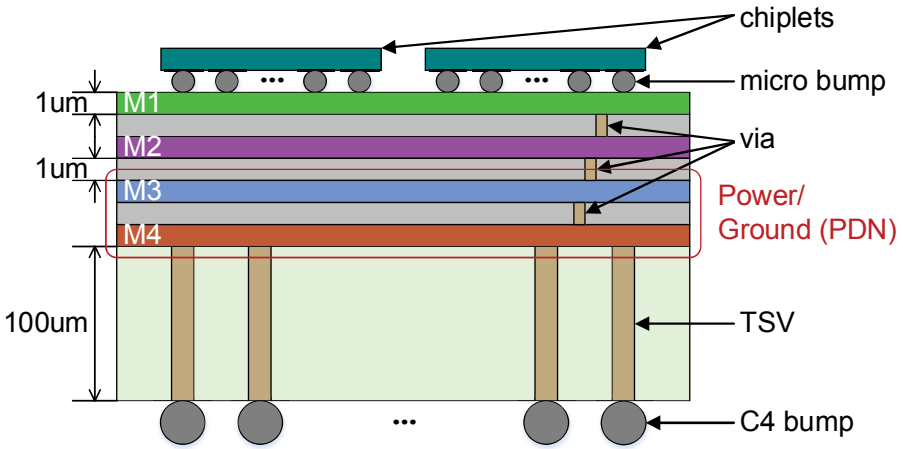


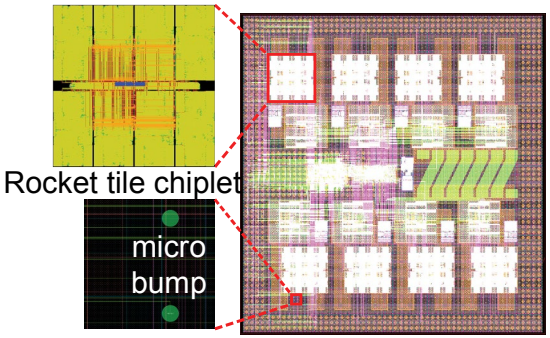
ReRAM generator

Session I: Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse

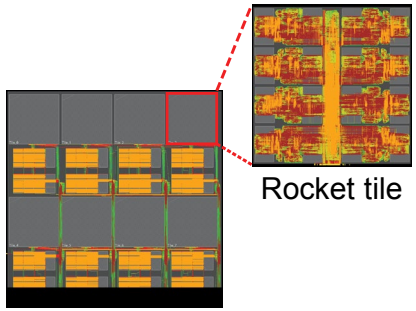
Student: Jinwoo Kim Faculty: Sung Kyu Lim

- Objective:
  - Analyze the power-performance-area overhead of 2.5D IC design
- Technical Approach:
  - A vertically-integrated EDA flow for 2.5D IC design
  - Hybrid-Link: A new protocol for 2.5D chiplet communication
  - ROCKET-64: RISC-V based 64-core architecture
- Latest Results:
  - 2.5D IC overhead
    - 2.5x area / 1.008x power / 17.0x avg. wire length increment





(a) Interposer-based 2.5D design



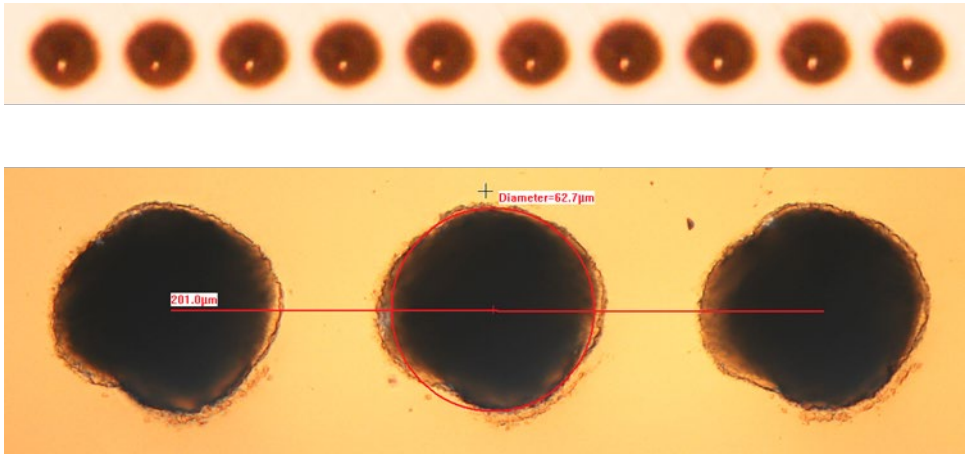
(b) Monolithic 2D design

This research is funded by the DARPA CHIPS project under Award N00014-17-1-2950.

Session I: High Aspect Ratio TGVs

Student: Rui Zhang Faculty: Prof. Swaminathan, Prof.Tummala

- Objective:
  - Investigate and develop high aspect ratio and small opening Through Glass Vias with low surface roughness for high density interconnects for 2.5D and RF applications
- Technical Approach:
  - Femtosecond NIR laser ablation
- Latest Results:
  - 80 µm TGVs in 300 µm glass using front side drilling
  - 60 µm TGVs in 300 µm using double side drilling
  - Process development for back side drilling



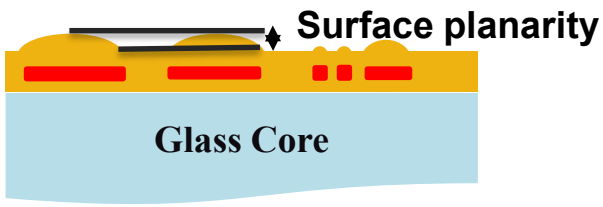
Session I: Ultra Low-K Ultra-thin Dielectrics for Panel RDL

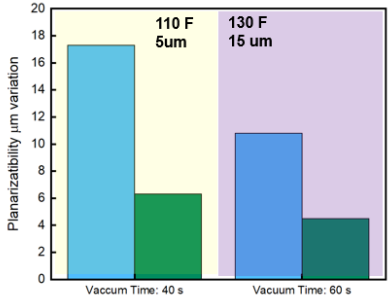
Student: Shreya Dwarakanath Faculty: Prof. Tummala, Prof. Swaminathan, Prof. Losego

- **Objective**: Develop RDL dielectric materials and processes to meet next generation interconnect needs for ultra-high bandwidth

- **Technical Approach**:
  - Ultra-low Dk (< 3.0) polymer materials selection and characterization
  - Develop RDL patterning and metallization processes for 1-2 µm line/space and 1-5 µm via with < 5% TTV of 1-5 µm dielectric height
  - Investigate chemical adhesion, residual stress and electrical reliability of material candidates with fine-pitch RDL

- **Latest Results:**
  - Evaluated surface planarity for dry-film dielectrics – thickness, process parameters, feature size (line/space, copper height)

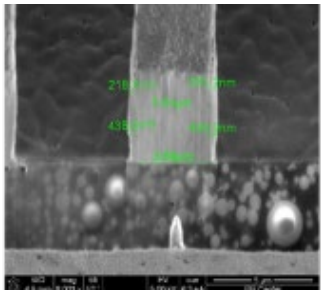


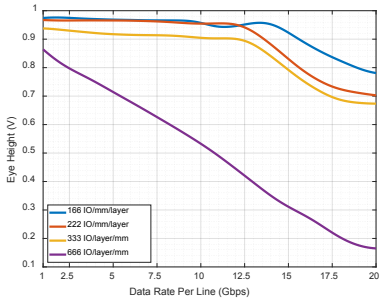


Session I: Modeling, Design, and Demonstration of 1 μm Low Resistance RDL for High Performance Computing

Student: Bartlet DeProspo
Faculty: Prof. Tummala and Prof. Swaminathan

- Objective: Development of required materials, tools and processes to develop 1 micron panel scale RDL
- Technical Approach: Fundamental analysis on technical limitations of SAP process
  - Figure out the material, tool and process limitations on SAP scaling
- Latest Results:
  - Established a roadmap for high performance RDL design
  - Studied substrate impacts on photoresist performance



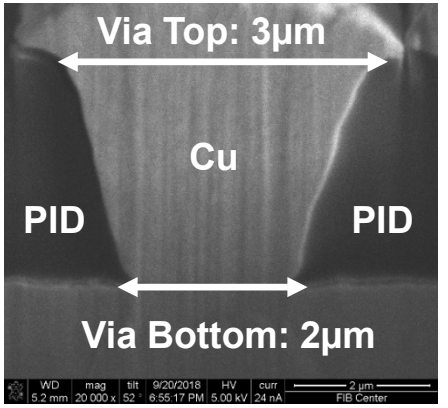


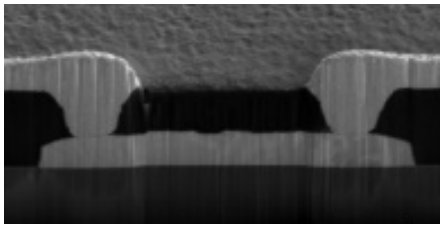
Metal Layer	370 nm	385 nm	405 nm
Aluminum	99.34%	97.41%	90.97%
Chromium	33.92%	23.22%	25.77%
Ti/Cu	47.17%	44.91%	46.49%

High Reliability Demonstration of 3 µm Photo-Vias in PID material for 2.5D Glass Interposer Applications

Takenori Kakutani, Visiting Engineer (Taiyo Ink Mfg. Co., Ltd.)

- Objective:
  - Challenge for high-density packaging is to maintain high reliability. To improve the package reliability, the high resolution dielectric material should have low CTE and strong adhesion.
- Technical Approach:
  - By minimizing the size of inorganic fillers, PID material with high resolution, low CTE, and good adhesion to substrate are produced.
- Latest Results:
  - 3 µm photo-microvias, with excellent adhesion were demonstrated in a PID material.
  - Very stable daisy chain containing 400 microvias with 3 µm diameter passed 2,000 cycles of TCT reliability test.





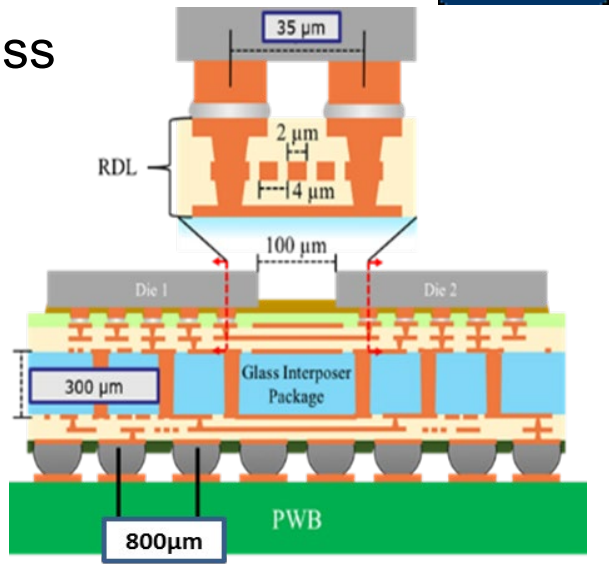
Session I: Design and Demonstration of 2.5D Glass Interposer

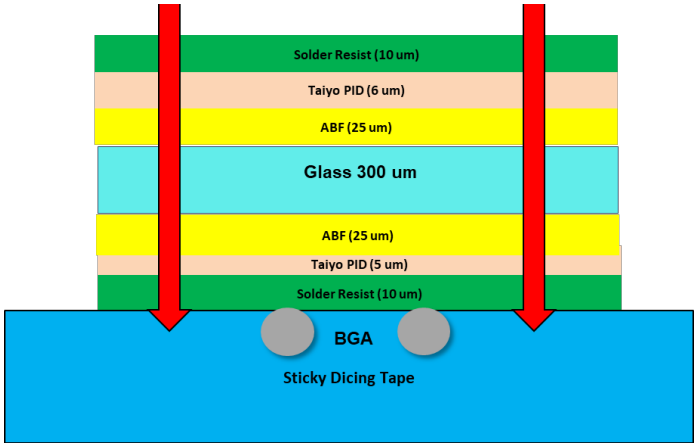
Students: Pratik Nimbalkar Faculty: Prof. Swaminathan, Prof. Tummala

- Objective: Design and Demonstration of 2.5D Glass Interposer BGA package with 2 µm ML RDL

- Technical Approach:
  - Glass interposer with tunable glass CTE for high thermo-mechanical reliability as next generation to Silicon interposers

- Latest Results:
  - Optimized sputtering conditions for improved adhesion and reliability of RDL
  - Residual stress analysis for ML RDL
  - Dicing test vehicle fabrication has been completed using three (3.4, 7.8 and 9 ppm/^{0}K) CTE glass substrates
  - Mechanical test vehicle fabrication is ongoing





Session I: 2.5D and 3D Glass Panel Embedding for High Performance Computing

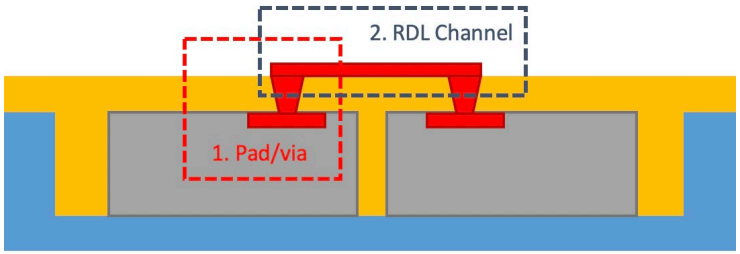
Student: Siddharth Ravichandran Faculty: Prof. Tummala, Prof. Swaminathan

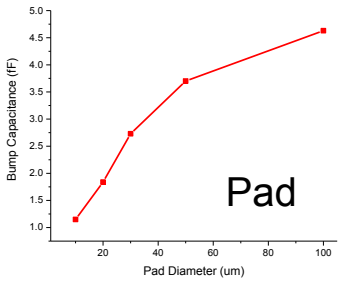
- Objective:

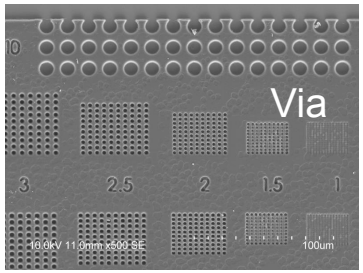
  Design and Demonstrate next-generation 2.5D & 3D architecture for 1 TB/S bandwidth at 1 pJ/bit power efficiency with:
  - < 20 μm I/O pitch
  - Smaller Form Factor
  - No TSV in Logic IC
  - Integrated Thermal Management
  - Lower Cost
  - Large-body direct board attach

- Technical Approach:
  - Fine-pitch 2.5D embedding in Glass panels with < 2 μm die-shift and integration with low-loss high-density polymer RDL
  - Fine-pitch (35 μm) TCB on GPE for < 50 μm 3D interconnect length

- Latest Results: Modeling and TV Fabrication for parasitic extraction





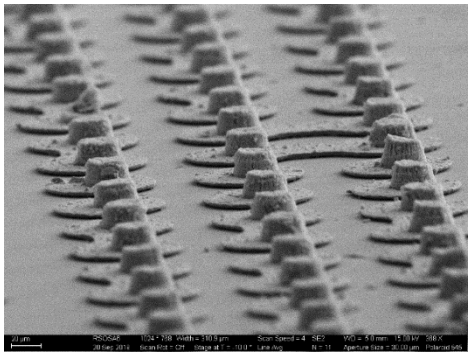


Session I-Direct Cu-Cu bonding in C2S applications using Cu-pillar with nanoporous-Cu caps

Student(s): Ramón A. Sosa
Kashyap Mohan

Faculty: Dr. V. Smet,
Dr. A. Antoniou

- Objective:
  - Enable fine pitch C2S all-Cu interconnections with high tolerance to non-coplanarities in assembly, and without a viscous phase to ensure scalability to fine pitch
- Technical Approach:
  - PRC is developing the Cu-pillar with nanoporous-Cu (np-Cu) cap technology, an all-Cu alternative to traditional solder
  - Nanoporous-Cu is a low modulus, solid-state, and highly reactive system that can be scaled to fine pitch, and bond at modest temperatures and pressures, sintering to an all-Cu joint
- Latest Results:
  - Studies to determine how different parameters affect dealloying and resulting np-Cu
  - Preliminary assembly demonstration

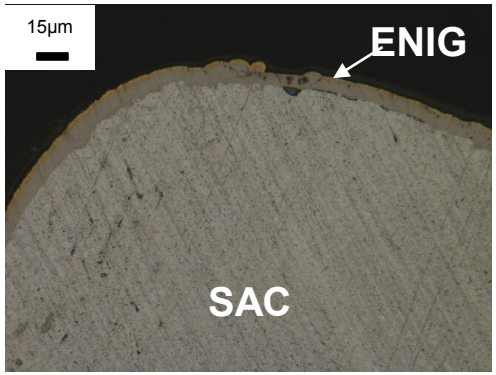


Session 1: Fabrication, attachment and characterization of solder spheres with multi-layered thin-film coatings for socketing and surface mount applications

Student: Omkar Gupte Faculty: Dr. Vanessa Smet, Prof. Rao Tummala

- **Objective:**
  - Design and demonstrate a single board-level interconnection system that can be used in socketing and surface mount applications
- **Technical Approach:**
  - Fabricate solder spheres with multi-layered diffusion barrier – noble metal coatings to satisfy contradicting requirements
- **Latest Results:**
  - Characterized package for socketing by thermal aging

ENIG coated solder sphere



Coated solder sphere attached with controlled solder paste wicking