Session II

Poster Title: **Analysis of Maximum Voltage Droops In Power Delivery Network**

Student(s): Seunghyup Han Faculty: Prof. Madhavan Swaminathan

❑ Objective:

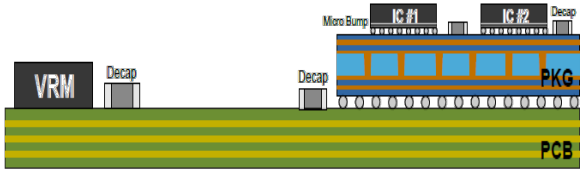
- Effectively estimate voltage droops and clarify the causes
- Estimate voltage droops from arbitrary currents

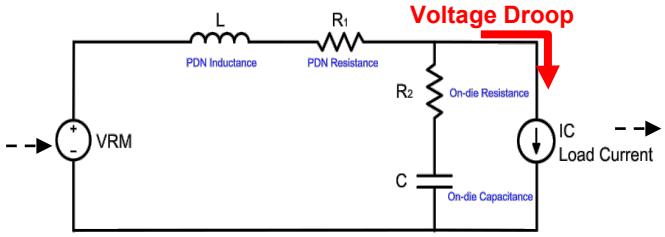
❑ Technical Approach:

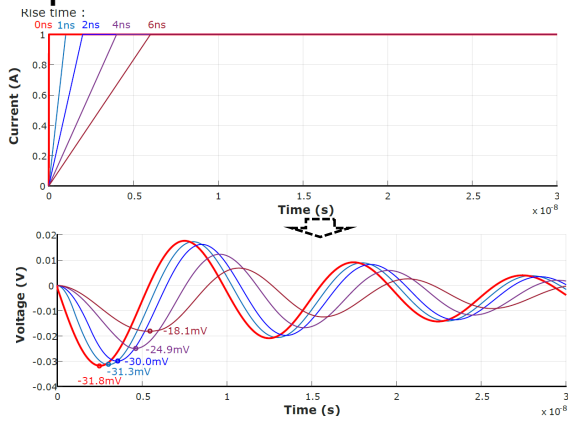
- Use the simplified equation and full equation derived in previous work
- Apply the decreased envelop term caused by current rise time

❑ Latest Results:

- Estimation of voltage droops from a step current considering its rise time
- Estimation voltage droops when multiple impedance peaks existed



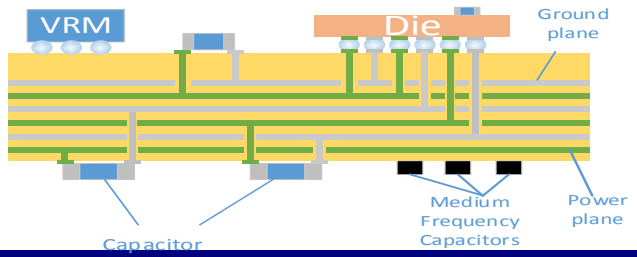


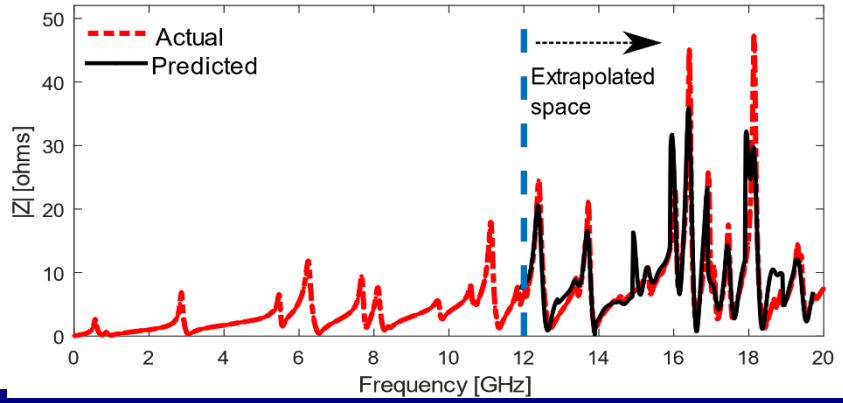


Session II: Impedance Response Extrapolation of PDNs using Recurrent Neural Networks

Student: Osama Waqar Bhatti Faculty: Madhavan Swaminathan

- Objective:
  - Design Machine Learning architectures that aid in design of power delivery networks reducing design time and computational complexity
- Technical Approach:
  - Deep neural networks provide ways to generate responses directly from physical structure of the circuit
  - Correlation in frequency space enables us to form connections to build impedance response
- Latest Results:
  - PDN impedance response can be extrapolated
  - 66% bandwidth extension achieved with 0.004 MSE ohm squared
  - Computation time

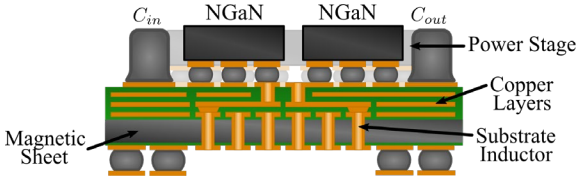




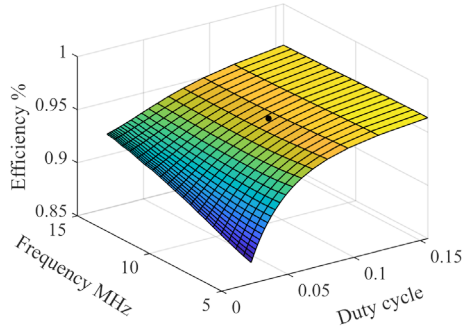
Session II - **Embedded inductors and Power Stage Co-Design for 48V to 1V Integrated Voltage Regulators**

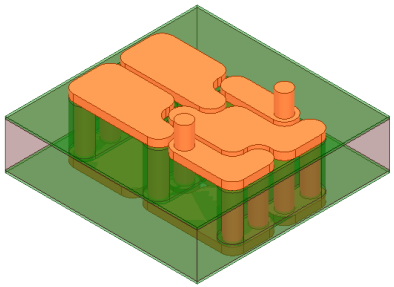
Student(s): Claudio Alvarez, Srinidhi Suresh, Venkatesh Avula
Faculty: Dr. Himani Sharma, Dr. Raj Pulugurtha,
Prof. Madhavan Swaminathan , Prof. Rao Tummala

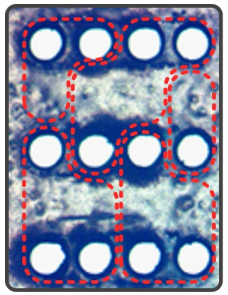
- **Objective:**
  - Design and demonstrate a 48V to 1V IVR with embedded inductors
  - IVR Efficiency 90% (Power Stage 95%, Inductor 95%)
- **Technical Approach:**
  - Power stage and inductor co-design
  - Frequency and duty cycle dependency on inductor efficiency
- **Latest Results:**
  - Determination of the minimum inductor requirements for 95% efficiency
  - Design of a high performance toroidal structure on magnetic sheets
  - Development of the fabrication process



Inductor Efficiency with L = 100nH





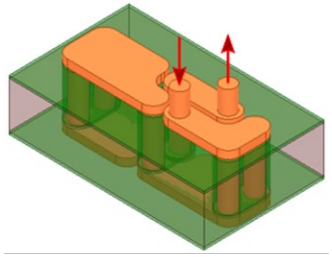


This work was supported in part by the Georgia Tech PRC industry consortium members.
This work was supported in part by the Semiconductor Research Corporation (SRC) and DARPA.

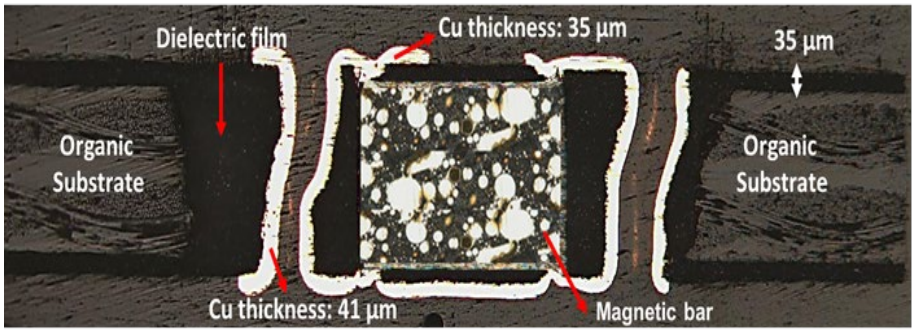
Session 2 **Poster Title:** Ultra-High Efficiency Substrate-Embedded Inductors for IVRs

Student: Srinidhi Suresh **Faculty:** Dr. Himani Sharma, Prof. R. Tummala, Prof. M. Swaminathan

- **Objective:**
  - Miniaturized high-density, ultra-low DC resistance embedded inductors for low (1 – 10 MHz) and high frequency (100 -140 MHz) IVRs.
- **Technical Approach:**
  - Spiral (2D), solenoid and toroid (3D) inductor topologies are modeled and fabricated to realize substrate-embedded inductors.
  - Advanced metal-polymer composites are used as the substrate core material.
- **Latest Results:**
  - Optimized 2D inductors fabricated using low and high frequency composite materials.
  - Fabricated solenoid inductors using low and high frequency composite materials (to be measured).
  - Modeled novel toroid inductors with an efficiency ~96% and established process flow (being optimized).



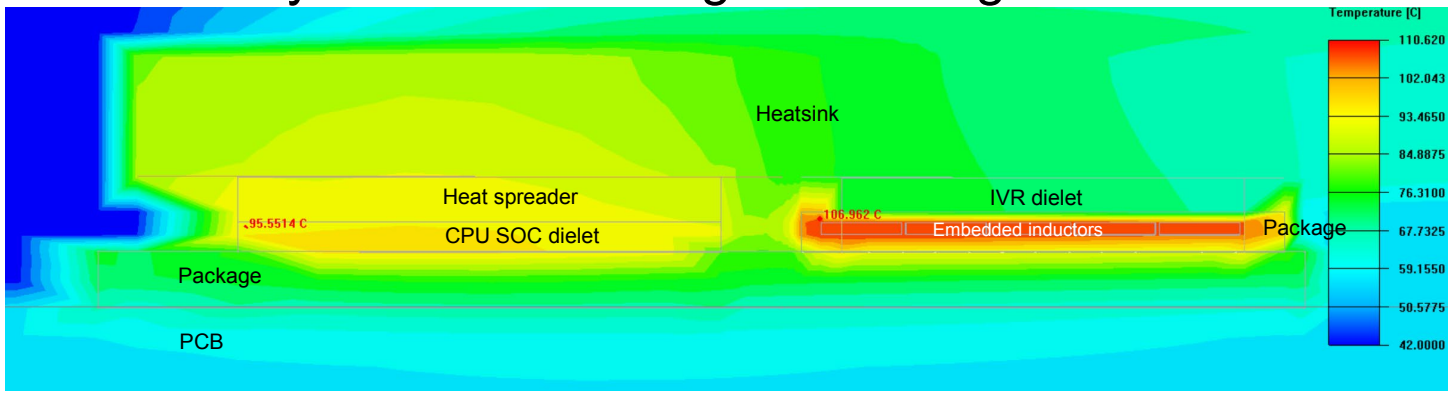
Novel Toroid Inductors



Session II: **Thermal Analysis of Integrated Voltage Regulators**

Students: Venkatesh Avula, Lydia Mele and Claudio Alvarez
Faculties: Dr. Vanessa Smet, Prof. Madhavan Swaminathan and Prof. Yogendra Joshi

- Objective:
  - Model, design and demonstrate substrate-integrated cooling solutions for 48V-1V IVR modules with embedded inductors.
- Technical Approach:
  - Board- or package-integrated vapor chamber as a thermal solution for the IVR, in combination with forced air cooling.
- Latest Results:
  - System-level thermal impact of integrated voltage regulators.
  - Thermal analysis of two heterogenous integration architectures of IVR.



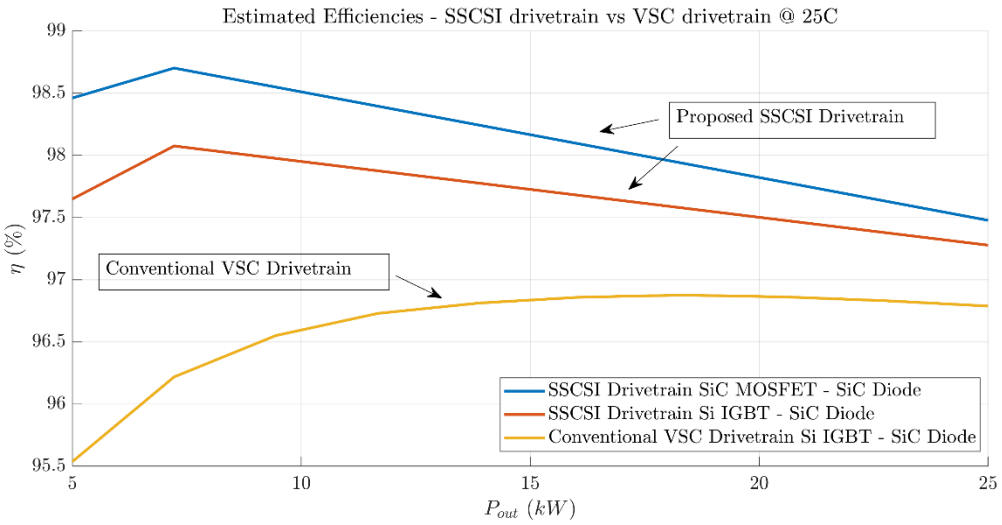
Temperature profile of a package-on-package IVR configuration

*** This work was supported in part by ASCENT, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.**

Session II: Soft-Switching Current Source Inverter for next-generation Electric Vehicle Drivetrains

Mickael Mauger, Prasad Kandula and Deepak Divan

- Objective:
  - Develop new power electronics for high power density, high efficiency and high reliability electric vehicle drivetrains
- Technical Approach:
  - Use novel soft-switching current source topology integrating all required functionalities into a single conversion stage
  - Leverage latest SiC devices advancements with controlled dv/dt
- Latest Results:
  - Unprecedented efficiency profile well-suited for electric vehicle applications



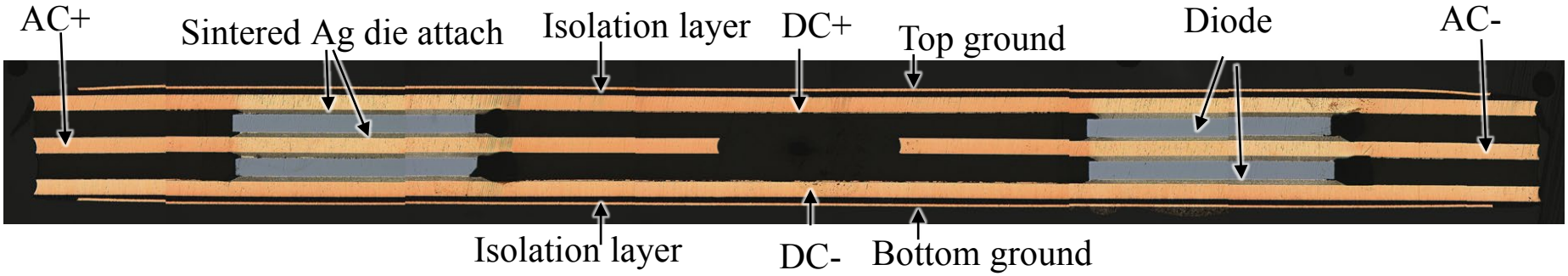
Session 2 – Design & Demonstration of3D Stacked Rectifier Module

Student: Haksun Lee Faculties: Dr. Vanessa Smet, Prof. Rao Tummala

- Objective: Design, demonstrate and characterize a new class of ultra-low parasitics, 3D SiC power modules with high efficiency, high dv/dt capability, and enhanced thermal Management and thermomechanical reliability

- Technical Approach:
  - Minimized parasitics L&C through 3D stacking suitable for high speed switching
  - Thick metal structures for high thermal capacitance, double-sided large area interconnect
  - Highly modular (ease of scalability to higher power)
  - Compatible with current and future manufacturing processes

- Latest Results:
  - Design and demonstration of 200V/15A 3D full-bridge rectifier module
  - Electrical and thermal characterization of the module

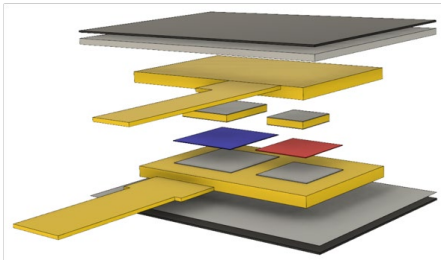


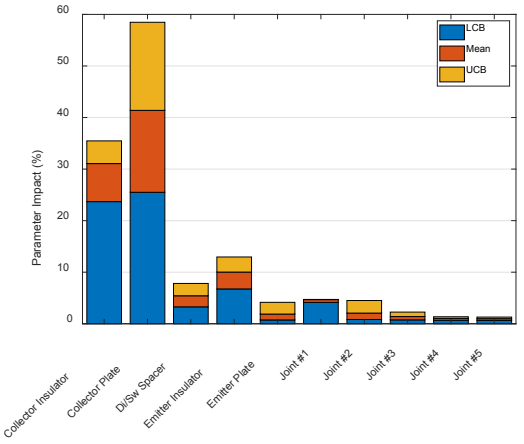
Session II - Bayesian Learning for Optimization and Analysis of SiC-based Inverter Package

Student(s): Hakki M. Torun, Ryan Wong

Faculty: Dr. Vanessa Smet, Prof. Madhavan Swaminathan

- Objective:
  - Determine optimal geometry of power card to maximize thermal performance, focusing on degrees of freedom in Z-direction as a first step.
  - Quantify which parameters affect the package temperature the most.
- Technical Approach:
  - Bayesian Active Learning to ensure convergence to global optima while minimizing CPU time & establish confidence bounds on the predictions.
- Latest Results:
  - Critical parameters are identified.
  - Improved thermal performance (~2°C)



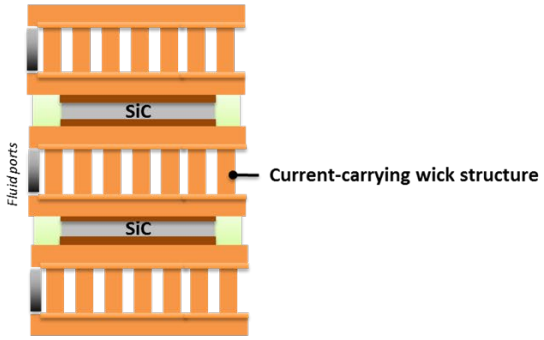


Session 2 | **Multiphysics Modeling of SiC-Based Power Inverters in (H)EVS: Integrated Cooling**

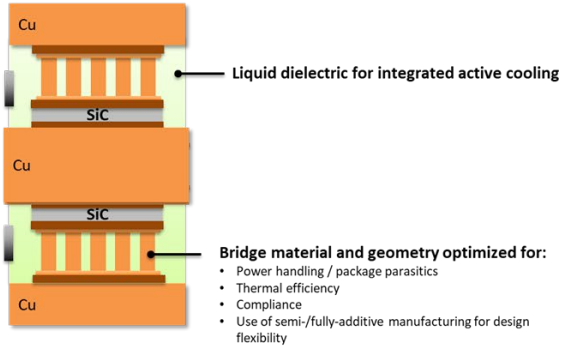
Students: *Ryan Wong, Lydia Mele, Hakki Torun*
Faculties: *Dr. Vanessa Smet, Prof. Antonia Antoniou, Prof. Yogendra Joshi, Prof. Madhavan Swaminathan*

- **Objective:**
  - Model, design, and demonstrate integrated single-phase cooling solutions for SiC 3D lead frame-based power cards.
- **Technical Approach:**
  - Use of machine learning algorithms to optimize wick structures in the auto-generation and combination of different layout, geometries, and materials.
- **Latest Results:**
  - Established framework for multiphysics environment and machine learning, with material development underway.

Advanced Cold Plates as Current Terminals



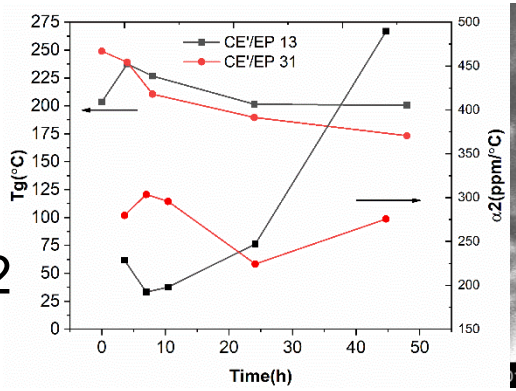
Direct Chip Cooling with Liquid Dielectric

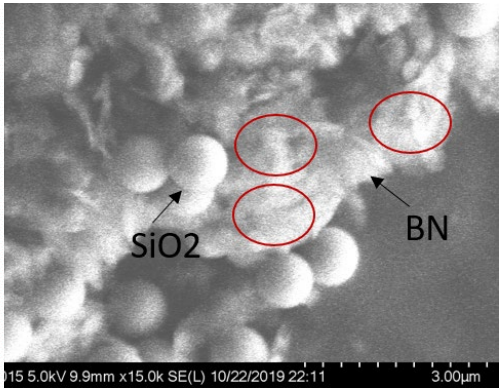


Session II – High Temperature, High Voltage and High Thermal Epoxy Molding Compound

Student(s): Jiaxiong Li Faculty: Prof. CP Wong

- Objective:
  - Demonstrate novel EMC with high temperature and high voltage reliability
  - Design filler technology to enable high thermal conductivity
- Technical Approach:
  - Incorporation of high temperature resin (cyanate ester) in epoxy
  - Design high thermal filler (BN) stacking structure and surface chemistry
  - Synthesis of high purity low moisture absorption resin and utilize additives (ion and electron trap) to improve BDV
- Latest Results:
  - Analysis of high temperature aging on Tg and chemical structure of CE/EP
  - Synthesis of BN coated SiO2 from self-assembly





Session # 2, Sintered Nanoporous Copper Die-Attach Interconnections for High-Power, High-Temperature Applications

Students: *Kashyap Mohan, Ramon Sosa* ***Faculty:*** *Prof. Antonia Antoniou, Dr. Vanessa Smet, Prof. Rao Tummala*

- *Objective:*

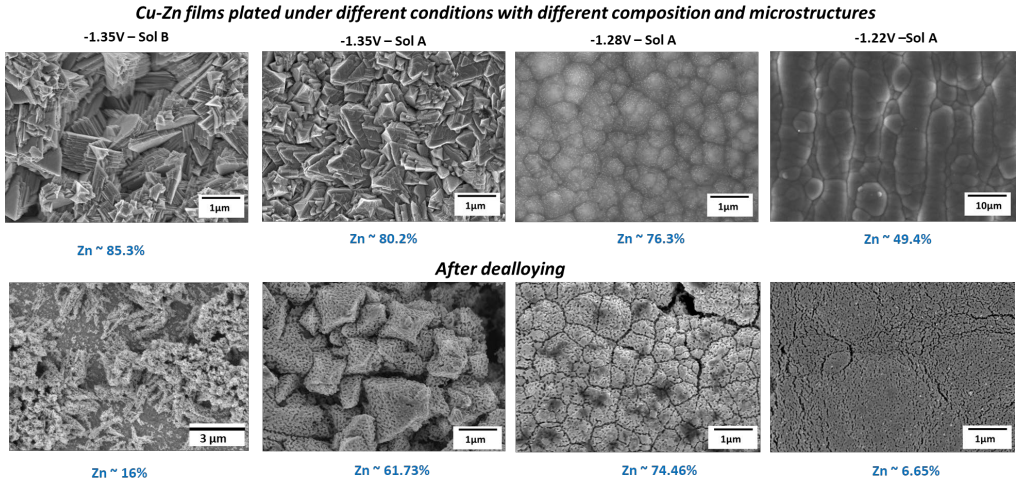
  Design and demonstrate low-cost, all-Cu die-attach interconnections with enhanced processability, by low-temperature (<250°C), low-pressure (<5MPa) sintering, for superior electrical, thermal and reliability performances under high operating temperatures (>250°C) and power densities.

- *Technical Approach:*

  - PRC is developing all-copper die-attach technology based on low-temperature film sintering of nanoporous copper (np-Cu), as an alternative to solders and Ag sintering.
  - Sintering of np-Cu offers several over sintered Ag pastes –
    - No residual organics after sintering.
    - Low shrinkage during assembly.
    - Low-modulus of np-Cu helps in accommodating surface roughness during assembly.
    - High densification giving bulk-Cu like joint properties.
    - Industry standard SAP processing for fabrication.
    - Versatility in implementation- can be used as an insert or fabricated directly on substrates/wafers.

- *Latest Results:*

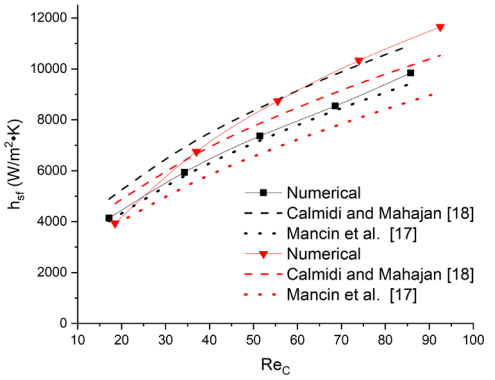
  - Fabrication of np-Cu films complete.
  - Work on sintering and assembly using np-Cu ongoing.

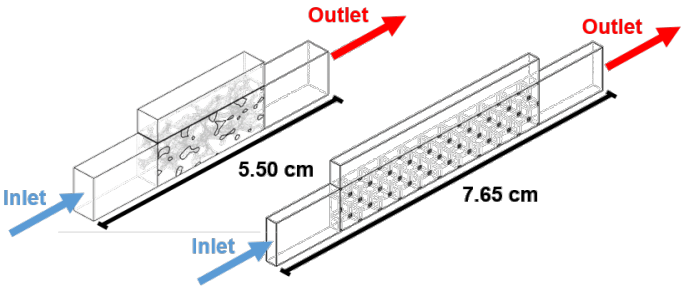


Session 2 – Poster Title: Additive Manufactured Foams for Power Electronics Thermal Management

Student: Justin Broughton **Faculty:** Prof. Yogendra Joshi

- Objective:
  - Demonstrate AM foam structures for power electronics cooling
  - Compare performance with commercial structures
- Technical Approach:
  - Numerical (CFD-HT) simulations with experimental validation
  - Pore-scale level models
- Latest Results:
  - Tortuosity was numerically compared for AM and traditional structures
  - Impact of attachment layer thermal conductivity investigated
  - Interfacial heat transfer coefficients compared to correlations





Session II Poster Title: Feasibility of integrated single-stage 48V to 1V conversion using GaN power devices

Student: Minxiang Gong
Faculty: Arijit Raychowdhury

- Objective:
  - Integrated single-stage 48V to 1V voltage regulator for point-of-load
  - High efficiency, high output current
- Technical Approach:
  - Optimal dead time control to improve efficiency
- Latest Results:
  - Feasibility study of single-stage high voltage conversion