Greetings from

Georgia Tech

Welcome & PRC Overview
Fall 2019 IAB Meeting

Madhavan Swaminathan
John Pippin Chair in Microsystems Packaging & Electromagnetics
School of Electrical & Computer Engg.
School of Materials Science & Engg.
Director, 3D Systems Packaging Research Center (PRC)

Georgia Tech | Institute for Electronics and Nanotechnology

Welcome

Industry

Students

Staff

Faculty

Key
1. Industry Members - 51
2. Students and PRC staff - 54
3. Faculty and research staff - 17
4. Non Members - 18

Total: 140 Attendees

Outline

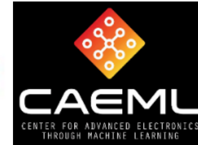
- PRC Overview
  - Organization
  - Membership & Benefits
- System Scaling enabled by Heterogeneous Integration
- Research Areas
- IAB Meeting Format

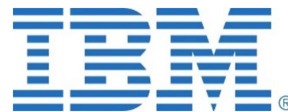
PRC Team

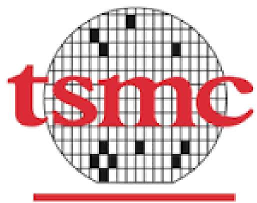
- 29 Faculty
- 8 Research Staff
- 3 Admin Staff
- 50+ G & UG Students
- 35 Industry Collaborators
- 4 Visiting Engineers on Campus
- Four Schools: ECE, MSE, ChE, ME (Multi-disciplinary)
- Diverse Research Focus
- Several Federally Funded Research Programs
- Mega-center on packaging & system scaling with expertise in Chip – Package – System
- Positioning: #1 Academic Center on Packaging around the Globe

PRC Students

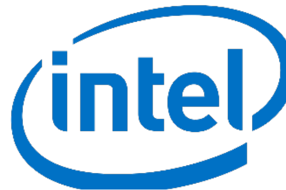
Collaborators







Designed for Brilliance. Engineered for Production.



TOKYO OHKA KOGYO CO., LTD.

Shared User PRC Facilities

- ❑ Comprehensive global Industry Consortium in System Scaling to enable supply-chain manufacturing to end-user needs
- ❑ Industry culture and R&D infrastructure (300mm clean room facility)

Plating Facility

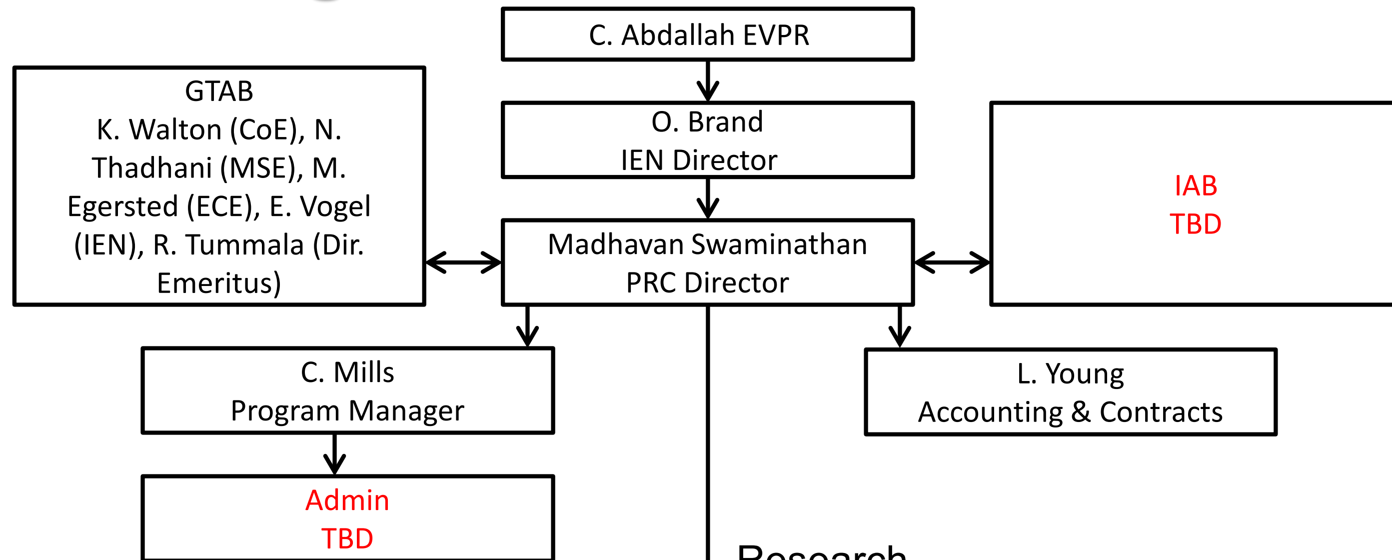
Substrate Cleanroom

Assembly Facility

Environmental Testing

Shared User Labs

Organizational Structure



Research

M. Kathaperumal
AI & HPC

Faculty

- Y. Joshi
- A, Antoniou
- A. Raychowdhury
- S. Mukhopadhyay
- T. Krishna
- S. Sitaraman
- C. P. Wong
- M. Losego
- J. Moon

T. Kakutani (VE)
A. Kubo (VE)
GRA (10); UG (1)

TBD (H. Torun)
ML

Faculty

- S. Lim
- A. Raychowdhury
- K. Roy

GRA (5); UG (3)

V. Smet
Power

Faculty

- Y. Joshi
- D. Divan
- H. Sharma
- R. Pulugurtha (FIU)
- RE (TBD)

N. Ogura (VE)
GRA (13)

TBD (A. Watanabe)
mmWave

Faculty

- Y. Joshi
- H. Wang
- M. Tentzeris
- R. Pulugurtha (FIU)
- S. Graham
- C. P. Wong

N. Ogura (VE)
K. Kanno (VE)
GRA (13); UG (1)

F. Liu
Emerging Tech.

Faculty

- A. Adibi

GRA (3)

C. White
Facilities

Faculty

- L. Dahal
- M. Kathaperumal
- V. Smet
- F. Liu

Note: Faculty Lead for each area TBD

System Scaling

Scaling

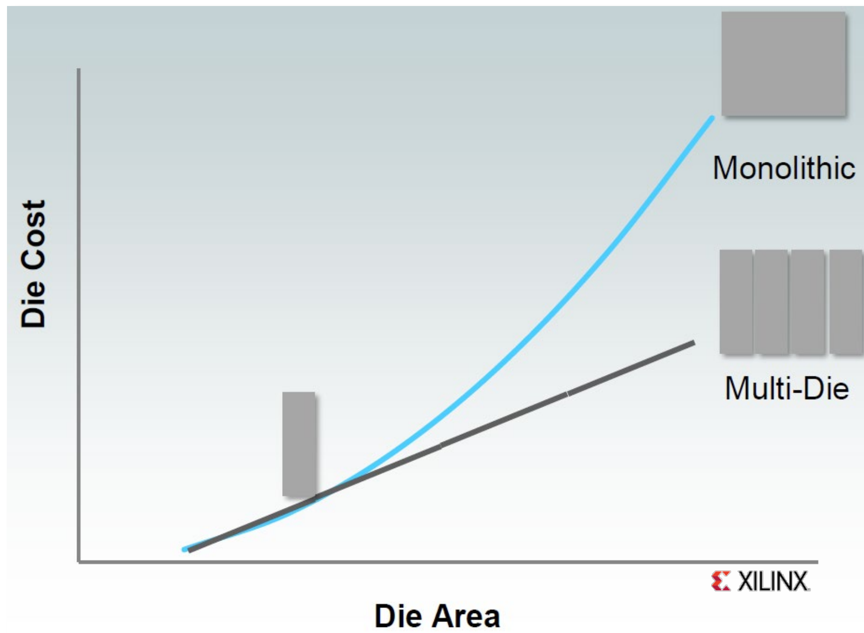
Size → Performance → Functionality

Vision – System Scaling through Heterogeneous Integration

M. Swaminathan and K. Han, "Design and Modeling for 3D ICs and Interposers", WSPC 2013
Modified: Arijit Raychowdhury, GT

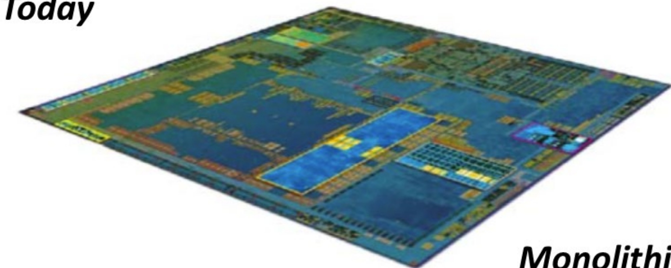
From Monolithic to Polylithic (Heterogeneous) Integration

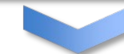
Cost of Monolithic Integration



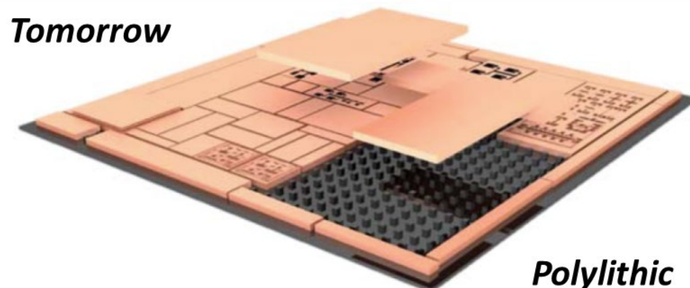
Shift to packaging as most cost-effective path to further system scaling

DARPA CHIPS Program Vision





New paradigm – chiplets & interconnect fabric



System on Package (SOP) Heterogeneous Integration Platform

NANO-BIO-SENSORS
THERMAL
SYSTEM-IN-PACKAGE (SIP)
Nanoscaled Interconnects
Nano-devices
Thinfilm Build-up Dielectric
SOC
GaAs
OPTOELECTRONIC
Embed IC
DIGITAL
RF
Ultra-fine pitch wiring & vias
Core
BATTERY
ULTRA HIGH DENSITY I/O INTERFACE

- ❑ Advanced Devices
  - ❑ 3D Memory, Spintronic Logic/Memory, Ultra WB, Compute Logic
- ❑ Assembled onto an Integrated Package with functional layers @ fine pitch
  - ❑ RF, Optical, Inductors, Capacitors, Sensors, Battery, Thermal
- ❑ Leading to scaled systems

PRC Membership & Benefits

PRC Membership
- $100K – Full
- $65K – Student
- $25K – Supply Chain

Large Multi-year Programs

Program	Cost	Focus
NSF CAEML	$50K	Package Design via Machine Learning
SRC JUMP	N/A	Heterogeneous Integration
DoD SHIP (I)	N/A	RF Center
DARPA CHIPS	N/A	Vertical Integrated Tools
DARPA DRBE	N/A	HPC
DoD	N/A	RF
DoE	N/A	ARPA - E

PRC Membership research areas: HPC & AI; Power Electronics; 5G & 6G Wireless

GT Proprietary Information to Center or Program Members:

- NERF IP Licenses
- Advanced Access
- Project Mentorship
- Supply Chain Engagement
- Targeted Student Access

Knowhow and Information published in public domain:

- New Technical Info
- More Student Access
- Expanded Faculty Expertise
- Available without added $

Devices and Components
Substrates and Wiring
Assembly, Reliability & Thermal

Design Methods, Machine Learning, Tools
Semiconductors
Power Delivery Networks and Devices

Research & Application Matrix

Applications

Research

	AI/HPC	Power		5G/6G	Extreme Computing (New)
		Comp	Auto (New)		
Design	Well Covered	Well Covered	Well Covered	Well Covered	Seed (Photonics+RF +Digital)
Materials	Partially Covered	Well Covered	Partially Covered	Partially Covered	
Process	Well Covered	Well Covered	Well Covered	Well Covered	
Assembly	Well Covered	Well Covered	Partially Covered	Well Covered	
Thermal	Partially Covered	Well Covered	Well Covered	Well Covered	
Integration	Well Covered	Well Covered	Well Covered	Well Covered	

Legend: Well Covered (green) · Partially Covered (yellow) · Not Covered (red)

- ❑ Matrix used to engage Industry & Faculty
- ❑ Helps identify investment and expansion areas

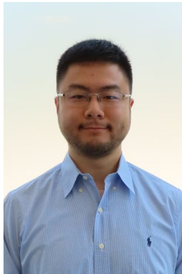
PhD Proposals (2019)

Shreya Dwarakanath, RDL, June '19 (joining Intel)

Tong-Hong Lin, RF, May '19

Kashyap Moh

Rui Zhang, Optoelectronics, Oct '19



Atom Watana
RF

ing,
ct '19

Bart DeProspo, RDL, De

Hakki Torun, Machine Learning, Nov '19

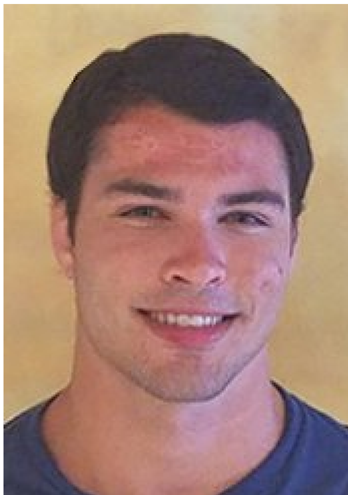
Tailong Shi, RF, Dec '19

Haksun Lee, Automotive, Oct '19

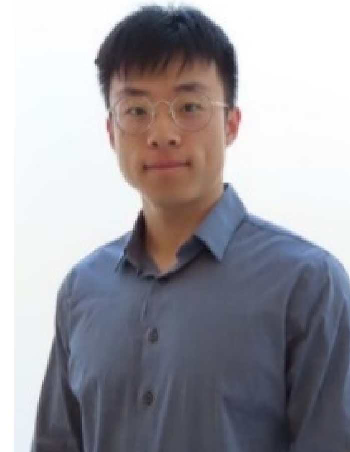
Expected Graduation 2020
Looking for Jobs

PhD Graduations

Dr. Chandrasekhar S. Nair
Modeling, Design, Materials, Processes and Reliability of Multi-Layer Redistribution Wiring Layers on Glass Substrates for Next Generation of High-Performance Computing Applications, May 2019
Employer: Intel Corp.



Dr. Robert G. Spurney
Advanced Materials and Processes for High-Density Capacitors in Next-Generation Integrated Voltage Regulators, Aug 2019
Employer: TI



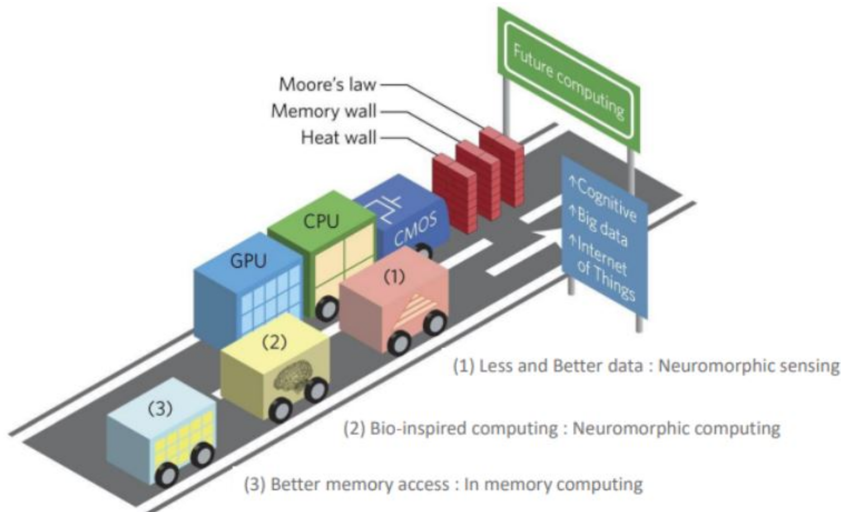
Dr. Huan Yu
Behavioral Modeling of Drivers and Oscillators using Machine Learning, Oct. 2019
Employer: Apple

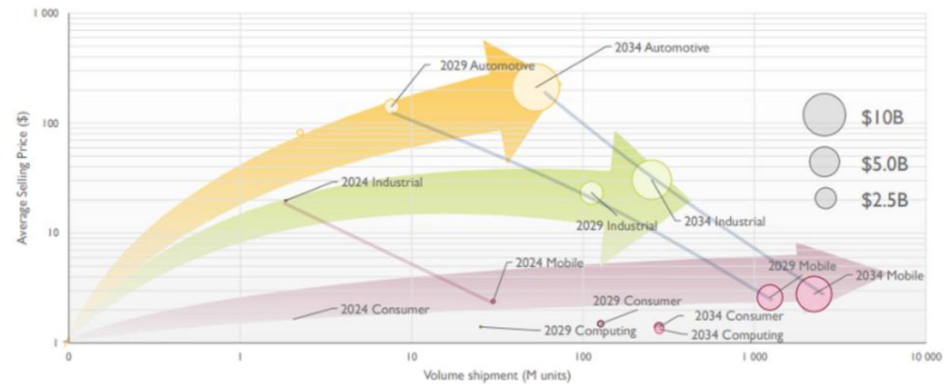
Student Summer Internships

1. Huan Yu: Apple, 2019
2. Hakki Torun: Intel, 2019
3. Nithin Nedumthakady: Intel, 2019
4. Kashyap Mohan: TI, 2019
5. Atom Watanabe: Qualcomm, 2019
6. Muhammad Ali: Apple, 2019

Several students looking for Internship during Summer 2020. Please interact with students during poster session!

Neuromorphic Computing





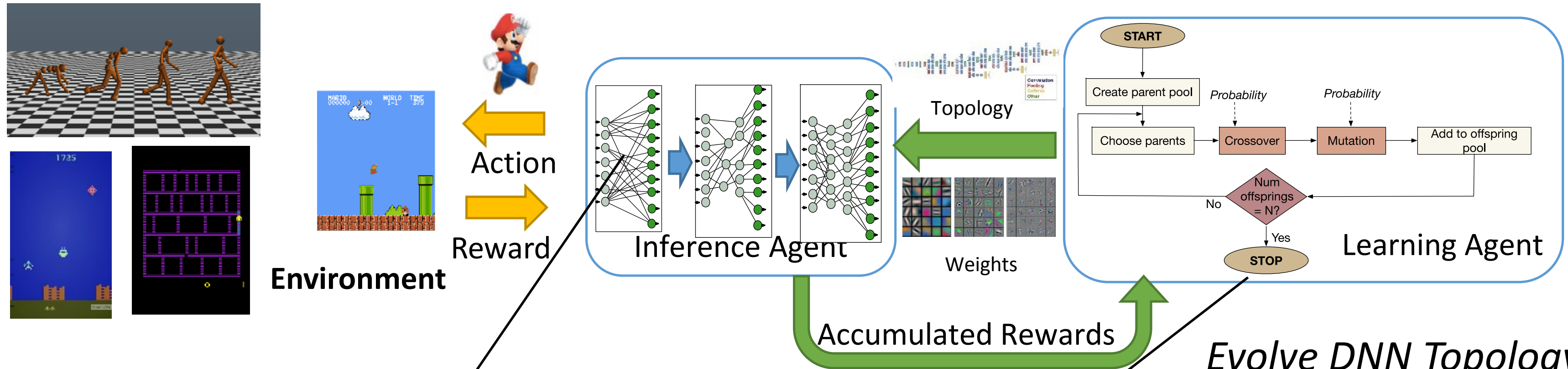
Adapted from "The future of electronics based on memristivesystems" Mohammed A. Zidan,John Paul Strachan & Wei D. Lu, Nature Electronics 2018

Courtesy: Yole Development

- ❑ Future of Computing
  - ❑ GPU+CPU+CMOS limited by Moore's Law, Memory Wall & Heat Wall
  - ❑ Move towards Neuromorphic sensing/computing with better memory access
- ❑ Large emerging market in Automotive, Industrial & Consumer segments over next decade

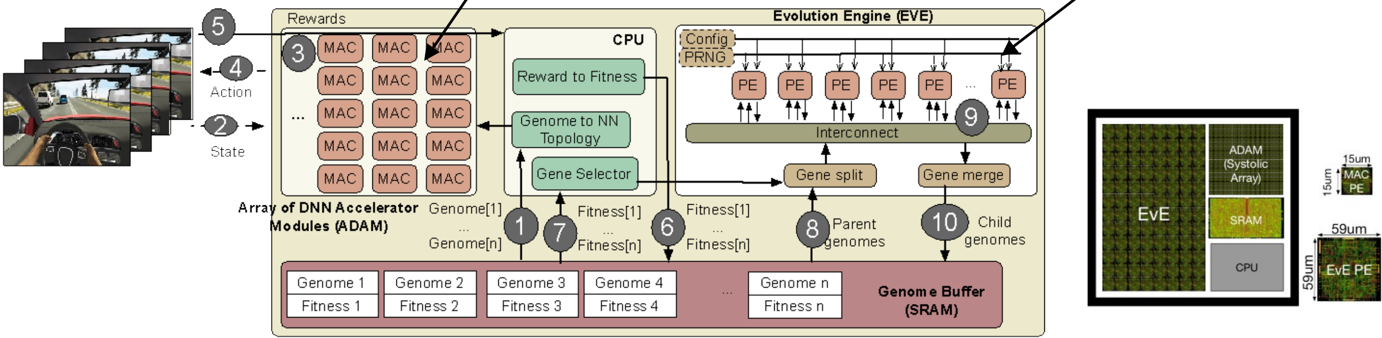
GeneSys: Enabling Continuous Learning using Neuro-evolution in Hardware

How do we learn at the edge in the absence of a (i) trained DNN model (ii) labeled data sets or (iii) connectivity to a backend cloud server



HW-SW Co-Design
Exploit Parallelism

Evolve DNN Topology continuously in response to rewards using Evolutionary Algorithm.



2 to 5 orders more energy efficient than CPUs and GPUs

Ananda Samajdar, Parth Mannan, Kartikay Garg, and Tushar Krishna,
GeneSys: Enabling Continuous Learning through Neural Network Evolution in Hardware, MICRO 2018

System Architecture – Digital/Wireless Convergence

Integrated Substrate
400mm x 400mm ?

RF Frontend

IVR
IVR

Dense Short Wires

5G/6G

RF Frontend

L2
L2
3D
L2

Long Wire

400, 000 Cores
18GB SRAM
15 to 50kW
AI/ML Processing

Cerebras WSE
1.2 Trillion transistors
46,225 mm² silicon

L2
L2
3D
L2

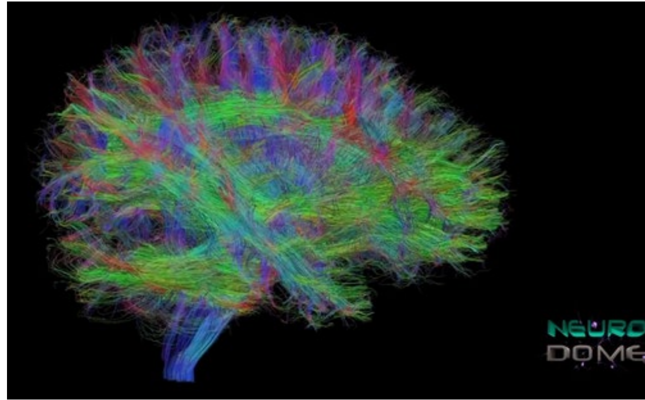
RF Frontend

5G/6G

IVR
IVR

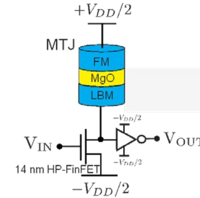
RF Frontend

AI & High Performance Computing

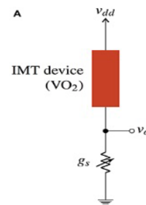


Courtesy: ASCENT, JUMP

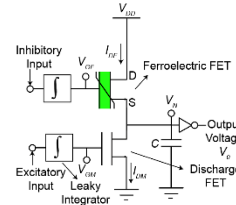
Spin Neuron

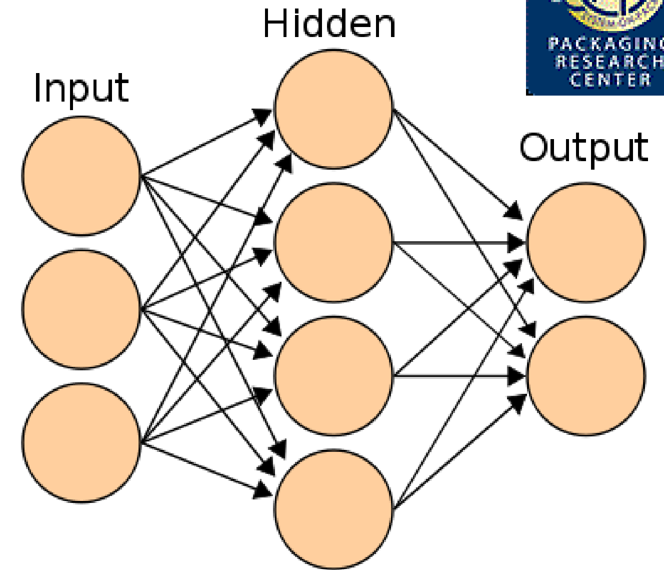


IMT Neuron



Ferro Neuron





- ❑ Limited by memory bandwidth where read/writes are performed at course granularities
- ❑ Massively parallel architecture supported by dense connectivity
- ❑ Suitable for life long learning and decision making in changing environment
- ❑ Co-located logic and memory (<u>In Memory & Near Memory</u>)
- ❑ Vertical CMOS & Beyond CMOS device technologies
- ❑ <u>Heterogeneous Integration with large substrate sizes (A better approach)</u>

Substrate Size driven by Artificial Intelligence

Heterogeneous Integration on TSV Interposer (L/S <1um)

Heterogeneous Integration
Fanout RDL Chip First (L/S >5um)
TSV Less Interposer Bridge (L/S >2um)
Fanout RDL Chip Last (L/S >2um)
Organic Substrate (L/S >10um)

Solenoid Inductor w/ Magnetic Core
IVR (3.6V/1V)
CHIPLET
Low Frequency Capacitors
S
S
G/P
P/G
Glass Interposer
VRM
Medium Frequency Cap

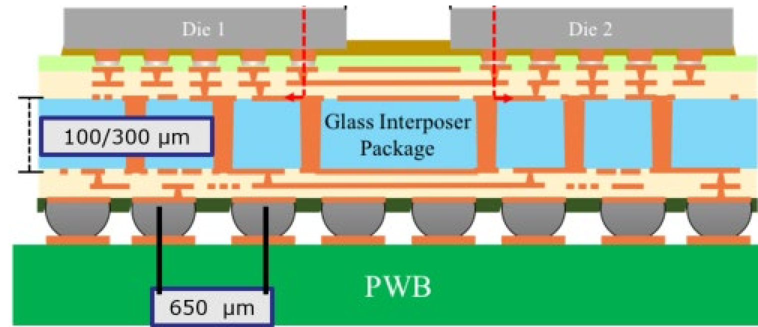
PRC

Pin Count: 0, 1000, 2000, 3000, 4000, 5000, 6000, 40000

Substrate Size (mm^2): 0, 500, 1000, 1500, 2000, 2500, 3000, 5000, 10000

Acknowledgement: John Lau, IEEE EPS tutorial, Malaysia (partial)

AI & High Performance Computing



Research Focus Areas

Research Focus Areas

Design

- Mach. Learn
- Optimization

High Aspect Ratio TGV

- 300um glass
- 2:1 to 10:1

Panel Scale RDL

- 1um L/S
- High AR

Cu-Cu Bonding

T < 250 °C
< 20 MPa

- <20um pitch
- Chip-Substrate

Reliability

- Large body size
- Double sided

Reliability Test Plans for Large Substrate Sizes

Package size

18.5 mm x 18.5 mm

Demonstrated reliability for 4ML symmetric package

Thermal cycling (-40 C to 125 C) passed 1000 h

Board-level assembly

Glass Package

Die

PCB

40 mm x 50 mm

Predicted reliability for 4ML symmetric package (May IAB)

Predicted reliability for 8ML asymmetric package (Nov IAB)

Ongoing demonstrator fabrication of 8ML asymmetric package

Thermal cycling test (-55 C to 125 C) planned

Glass (300 µm)

100 mm x 100 mm

Solenoid Inductor w/ Magnetic Core

IVR (3.6V/1V)

CHIPLET

Low Frequency Capacitors

S

S

G/P

P/G

Glass Interposer

VRM

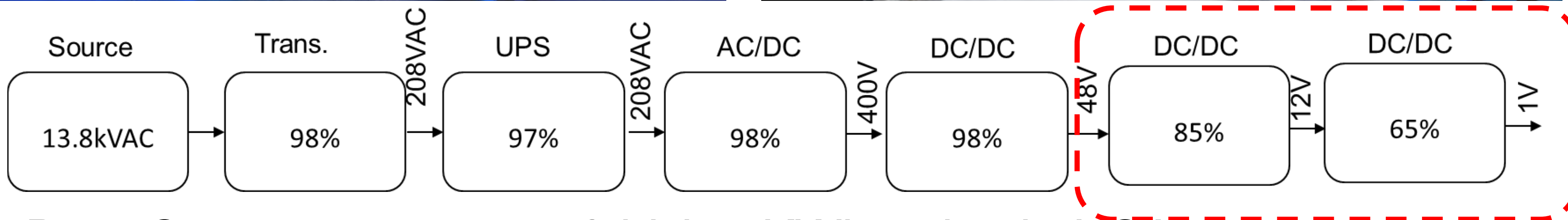
Medium Frequency Cap

Completed | Ongoing | TBD

2017 | 2020 | Near Future

Time

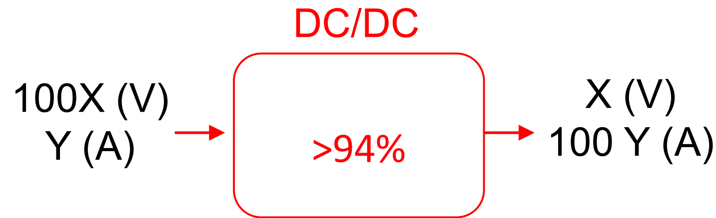
Data Centers & Energy



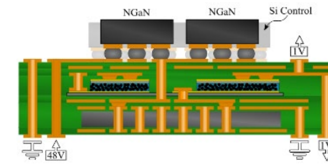
- Data Centers consume 70 billion KWh today in USA
- For every 2W drawn from the grid only 1W is used by the Data Center
- 20% improvement in efficiency can translate to 20% reduction in energy consumption

Source: Dept. of Energy, USA

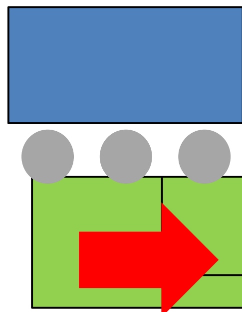
Efficient Power Delivery in Microsystems



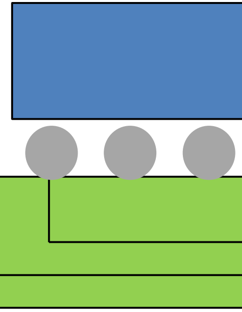
Single Stage Conversion



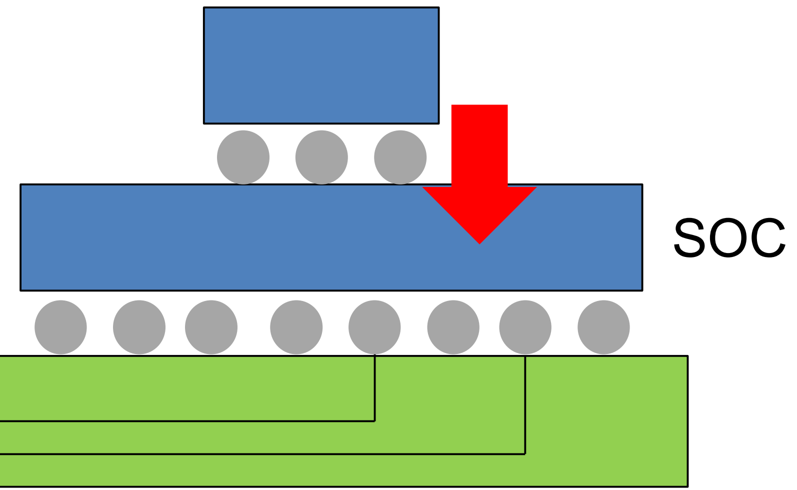
Buck Converter



Buck Converter

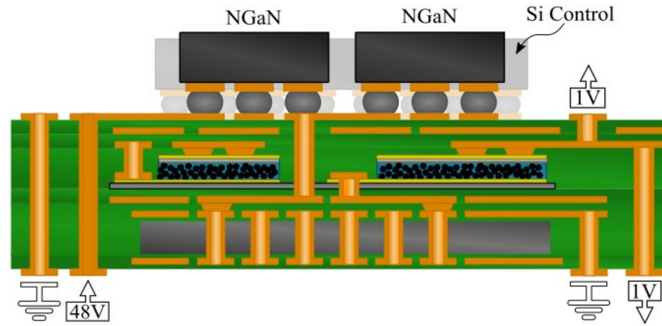


Buck Converter



- ❑ Bring the converter (power source) in close proximity to SOC
  - Significantly reduce Cu losses due to shorter current paths
- ❑ Need: High Efficiency, Highly Integrated, Highly Miniaturized, High Conversion Ratio, Single Stage Converters
- ❑ Low energy circuits

Power Electronics - Computing



Research Focus Areas

Research Focus Areas

Design

- Topologies
- Embedded L & C

Modeling

- Machine Lear
- Predictive
- Optimization

Process

- $>50nH/mm^3$
- $>2A/mm^2$
- $10m\Omega$

Embedded Capacitors

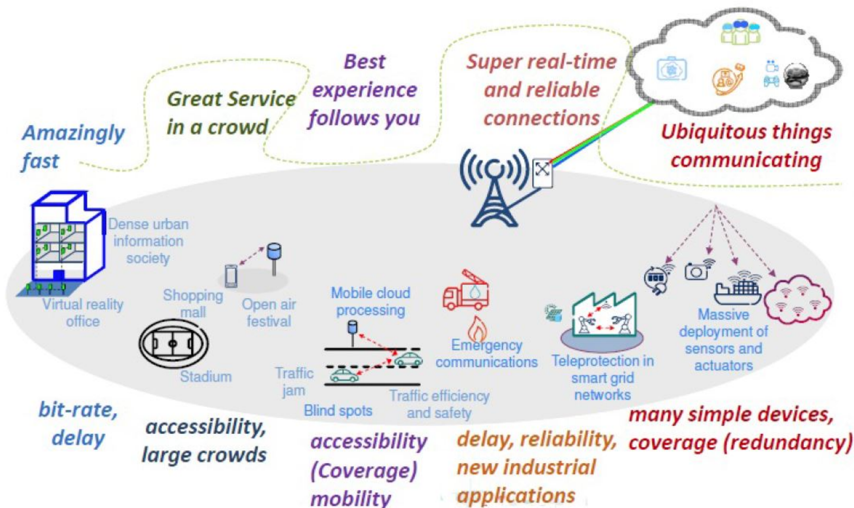
- $>0.1uF/mm^2$
- 100um thick
- 10MHz

Thermal Management

- Joule Heating
- Coupling
- Max. η

5G & 6G Wireless

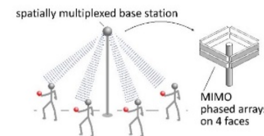
5G



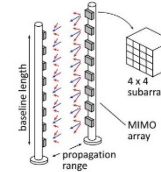
Courtesy: M. A. M. Albreem, I4CT '15

6G

MIMO hub: 256 beams/face, 10Gb/s/beam
140GHz, 220GHz

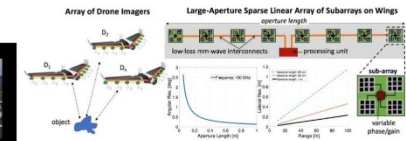


Point-point MIMO: 340GHz: 640Gb/s (650GHz: 1.3Tb/s)



Hardware-efficient 340GHz imaging
300 meters, 512× 64 image, 60Hz, 15 dB SNR

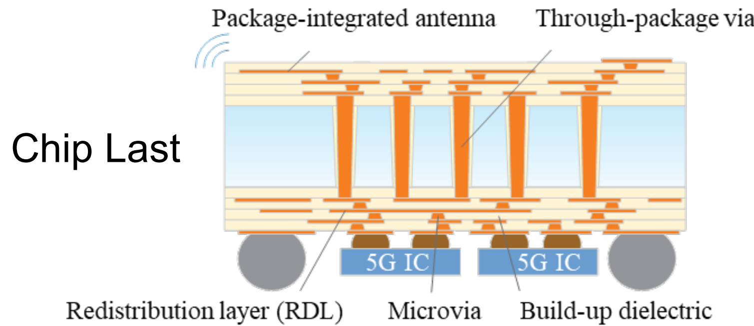
Cooperative / sparse 220 GHz imaging

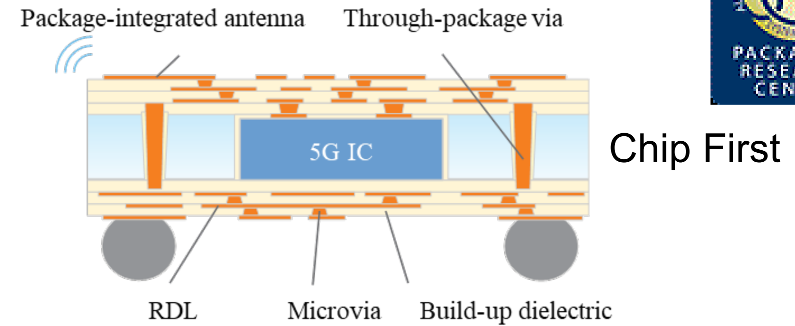


Courtesy: ComSenTer, JUMP

- 5G mmWave 24GHz – 86GHz
  - High levels of attenuation
  - Increase the data bandwidth available over smaller, densely populated areas
  - increase data capacity, decrease latency and connect many more devices
- 6G sub-THz (0.1 – 0.5 THz)
  - MIMO, Imaging, Non-destructive testing, Virtual Reality ….
- <u>Requires new materials & package integration technologies</u>

5G & 6G Wireless

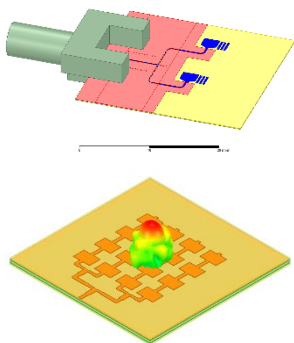




Research Focus Areas

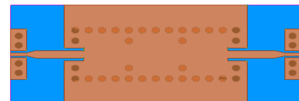
Research Focus Areas

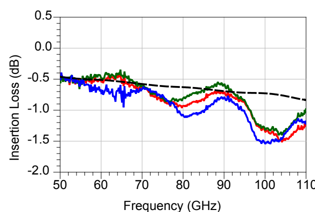
Antennas



- High Gain & BW
- 5G & D-Band

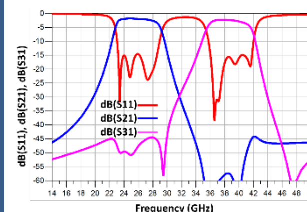
Interconnects





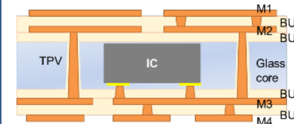
- Microstrip, CPW, SIW
- 5G & D-Band

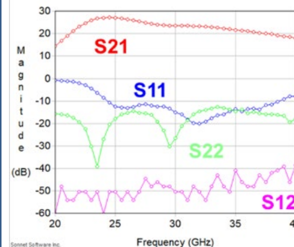
Passives



- Filter, Divider, Coupler….
- 5G & D-Band

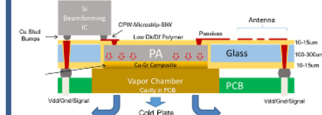
FOPLP/FEM

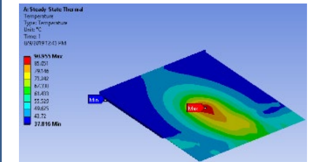




- Panel Embedding
- 5G & D-Band

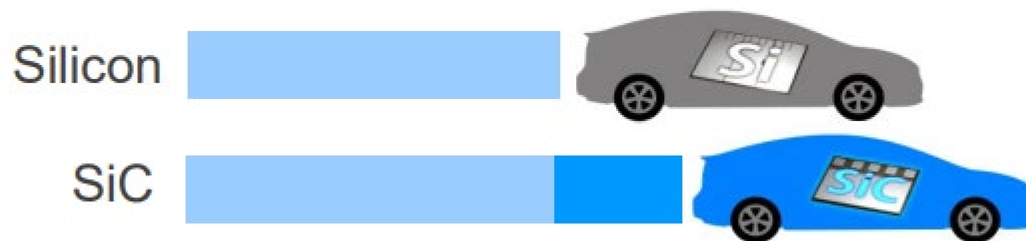
Thermal Management

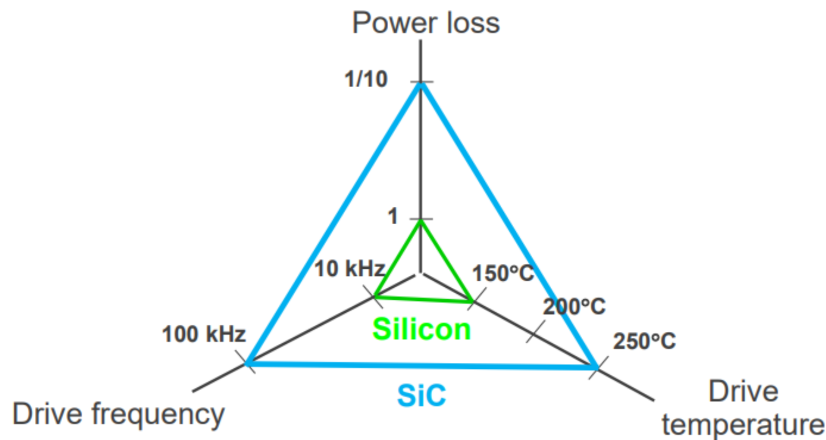




- 20-200 W/cm^2
- 5G & D-Band

Power Electronics – Automotive (New)



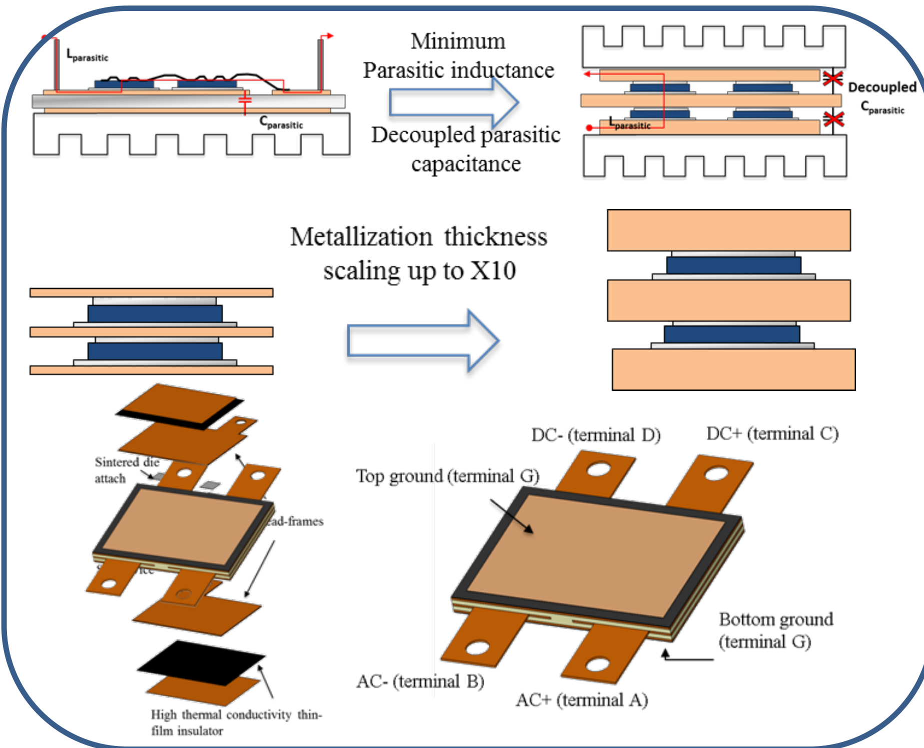


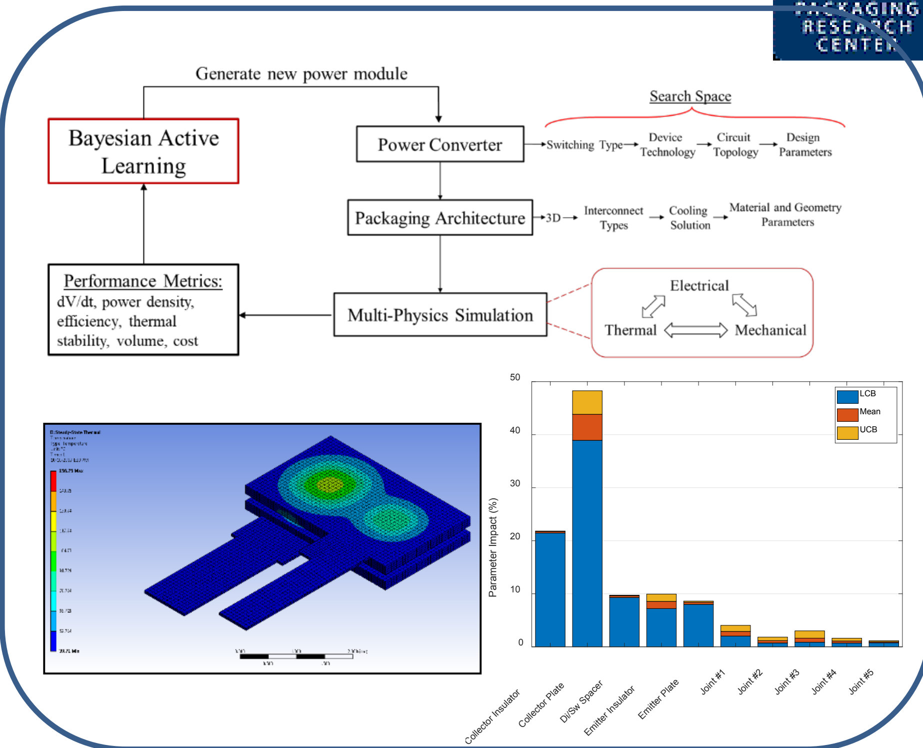
B. K. Chakravarthy and G. Sree Lakshmi, "Power Savings with all SiC Inverter in Electric Traction applications," *E3S Web Conf.*, vol. 87, pp. 1-14, 2019.

SiC-Based Drive Inverters

- Move towards SiC based modules
- Need for 3D Integrated Packaging that reduces parasitics & improves thermal performance
- Exploration of new package architectures required!

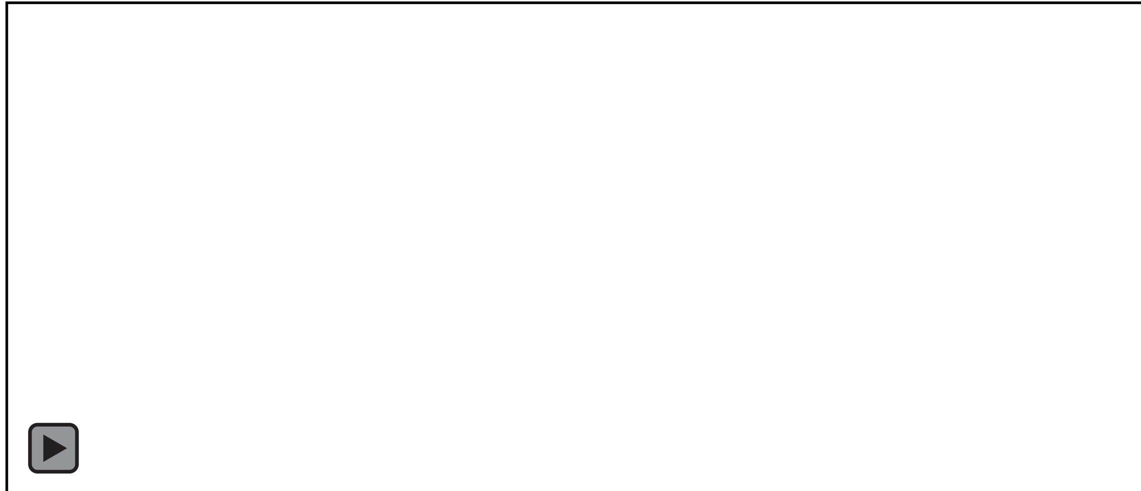
3D Integrated Packaging & Machine Learning





- 3D Integrated Packaging for:
  - High speed switching
  - High thermal capacitance
  - Double-sided large area interconnect
  - Minimized thermal gradient within the package
  - Highly modular solution for manufacturing
- Use of Machine Learning to:
  - Develop new package architectures
  - Optimize structures to minimize design cycle time
  - Remove human out of the loop
  - Investigate new materials and interfaces

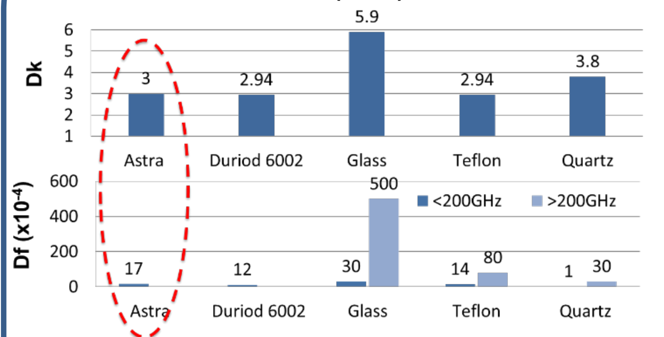
Thin Glass as a Substrate Material

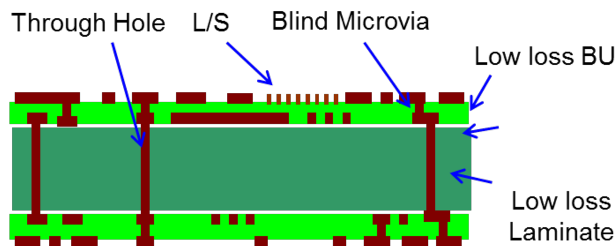


Courtesy: Martin Letz, Schott AG

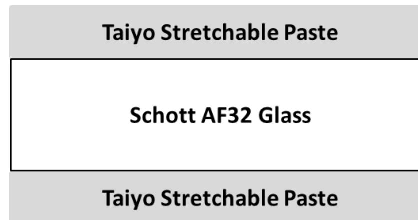
Emerging Technologies (New)

- ❑ Organic Packaging for D-Band (6G)

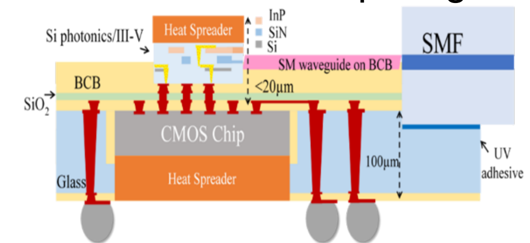


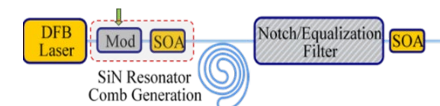


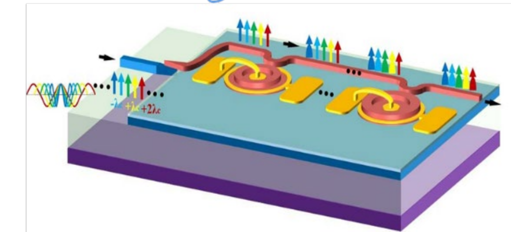
- ❑ Flex on Glass for mmWave



- ❑ Photonics for Extreme Computing







- ❑ Session IV
  - Based on industry feedback from May ’19 IAB
  - Industry – please provide feedback on your interest level in these areas

IAB Meeting Format

- Four Sessions
  - Session I: AI & HPC
  - Session II: Power Electronics
  - Session III: 5G & 6G
  - Session IV: Emerging Technologies
- Sessions I, II & III
  - Oral Presentations
  - One Slide Poster Introduction
  - Poster Session
  - Session IV (Oral Presentation only)
- Industry feedback after each session
- PRC Membership Details on Nov 8 (AM)

Thank you