Glass Packaging Technology: Status & Update

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Industry Partners: AGC, Corning, Schott, Intel, TOK, Taiyo, Panasonic, Brewer Science, Nagase, AMAT, Ajinomoto, Disco, Atotech, Samtec, Unimicron, SKC, Murata, TSMC

Outline

- ☐ Goals & Objectives
- ☐ Technical Approach
- ☐ Results & Key Accomplishments
- ☐ Comparison with Prior Art
- ☐ Schedule
- ☐ Summary

Goals and Objectives

Glass Based Technologies at PRC

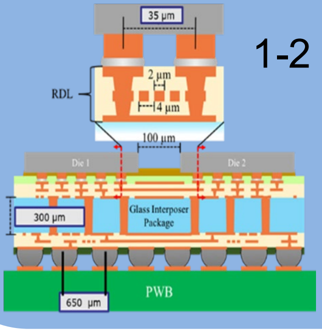
HPC

Flexible Glass
(Session III)

5G/6G, mm Wave
(Session IV)

Glass Interposer

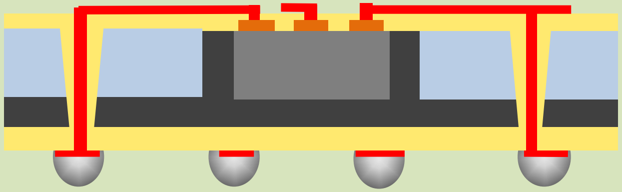
- ☐ TGVs
- ☐ Microvias
- ☐ Leakage Current Measurements
- ☐ Large Body Size
- ☐ Thermal Simulations



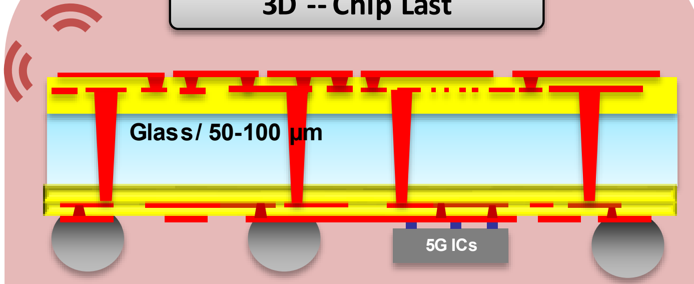
1-2 µm L/S

GPE

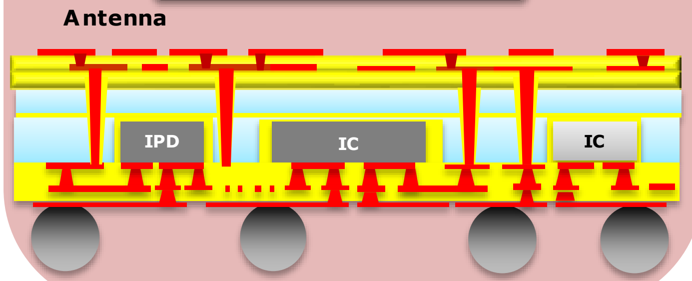
- ☐ Fine Line/Space
- ☐ MCMs-Embedded
- ☐ Ultra-thin GPE package



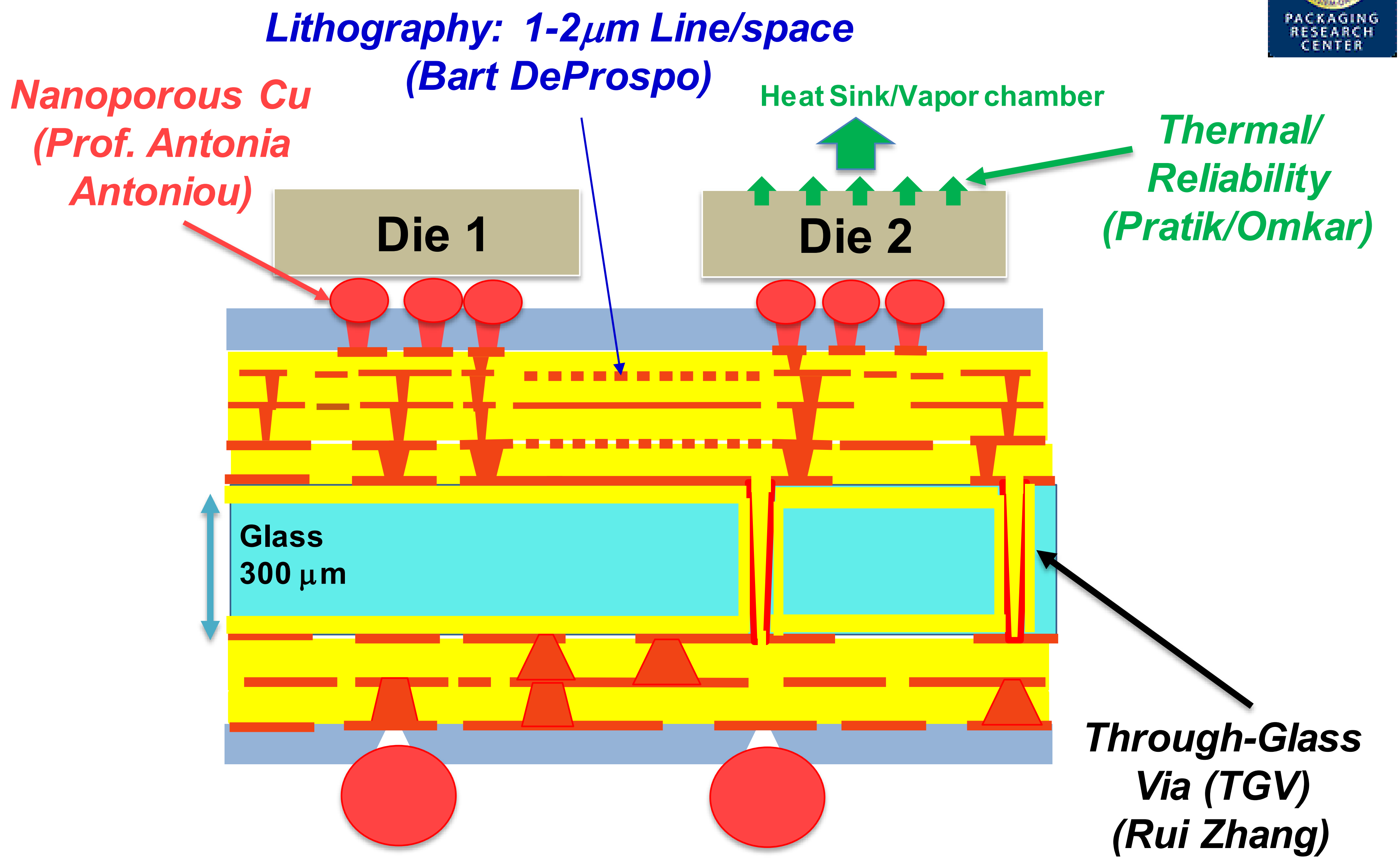
3D -- Chip Last



GPE – Chip first



Technical Approach



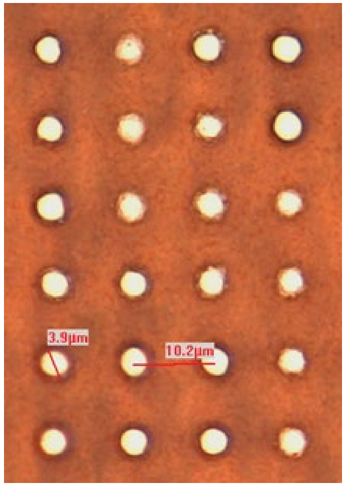
Technical Challenges for High AR Through Vias and Microvias

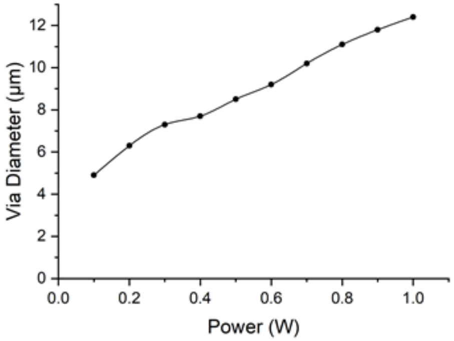
- Anisotropic etching for high aspect ratio structures
  - Bosch instead of DRIE on silicon
  - Laser assisted HF etching instead of HF etching
- Tapered sidewalls limiting the aspect ratio

- Challenges for TGVs
  - Brittle for mechanical drilling
  - Anisotropic chemical etching
  - Tapered shape diffuses laser power

Femtosecond laser based drilling method used to fabricate < 100 μm (Rui Zhang)

Microvias by Picosecond UV laser. Microvia diameter: 5 μm with 10 μm pitch





Liu et al. Innovative Sub-5 micron microvias by Picosecond UV laser for 2.5D Interposers and Fan-out Packages, IEEE CPMT, 2019.

Rui, Fuhan

Results: 1 µm L/S Mini-Consortium

CORNING
Glass Substrate

AJINOMOTO
Dielectric material

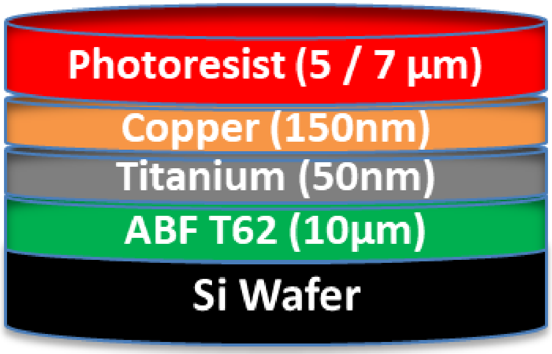
APPLIED MATERIALS
Sputter

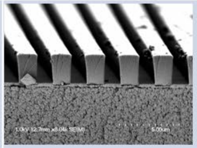
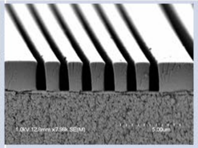
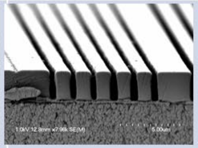
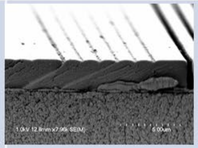
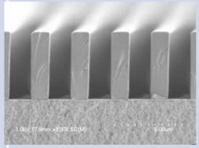
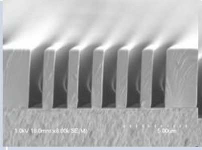
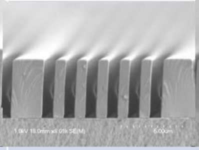
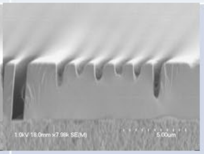
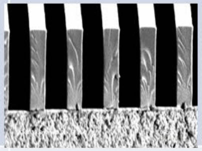
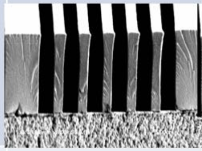
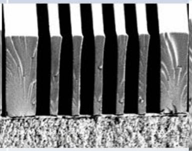
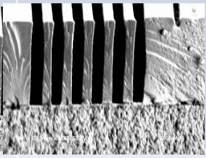
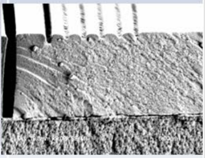
intel
End User

tok
Resist

Canon
Projection Stepper

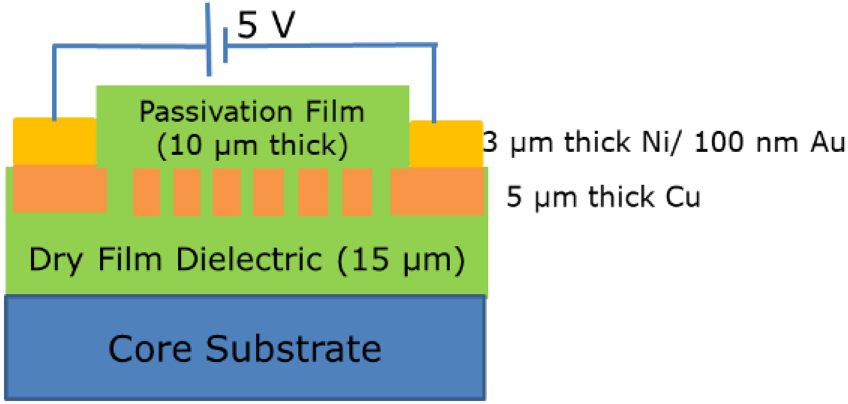
- Goal: to fabricate and build 1 µm Electronics Packaging RDL in conjunction with our industry consortium
- Each of these companies is providing input and services into this study to demonstrate successfully 1 µm RDL on a 12”×12” glass panel for supply chain and end user interest.
- These samples will be fabricated all the way through metallization and reliability

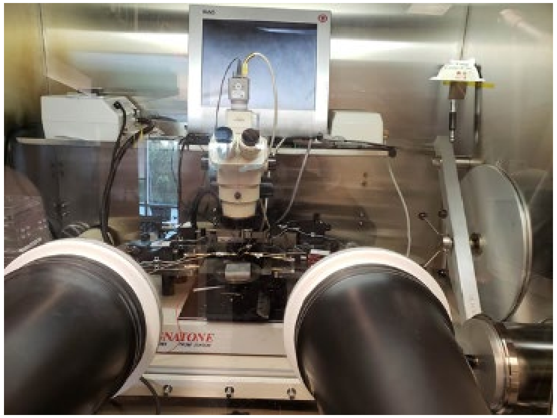


Mask L/S (um)	2.0	1.5	1.0	0.9	2.5
PC-0471W F-5 (CA system) Liquid 3um					
CD measurement Top and Bottom	T=1.72 um B=1.55 um	T=1.19 um B=0.99 um	T=1.12 um B=0.97 um		
PC-0471W (CA system) Liquid 5um					
CD measurement Top and Bottom	T=1.35 um B=1.41 um	T=0.85 um B=0.85 um	T=0.94 um B=0.85 um		
PC-0471W (CA system) Liquid 7um					
CD measurement Top and Bottom	T=1.36 um B=1.24 um	T=1.07 um B=0.84 um	T=0.99 um B=0.74 um	T=0.80 um B=0.61 um	

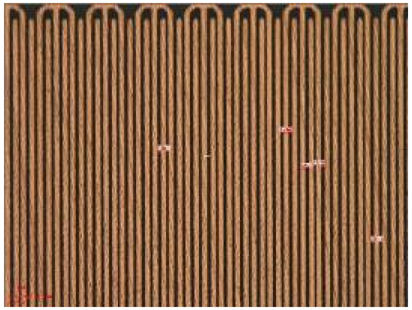
- Resolution: 0.8 – 0.9 µm Line?
  - Reproducibility
  - Yield

Results: Reliability of Fine Pitch Traces

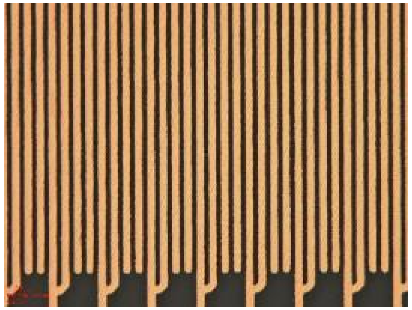




Leakage Measurements inside a Glove Box before and after bHAST (130 ^{0}C, 85 % RH, 100 hrs, 5 V)



Design: 3 µm width/ 4 µm space
Fabricated: 4.5 µm width/ 2.5 µm space (min space ~ 1.5 µm)

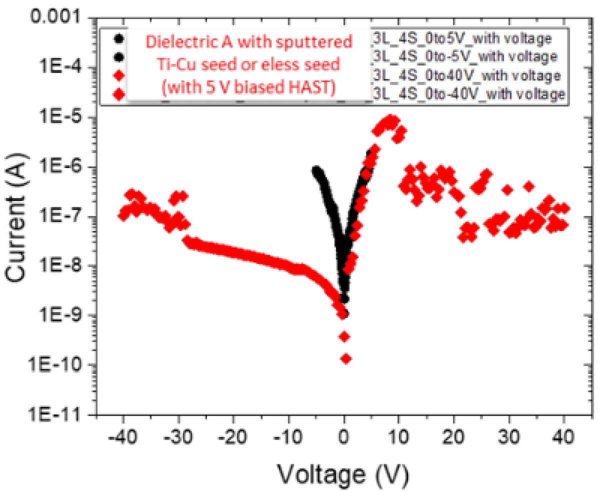


Design: 4 µm width/ 6 µm space
Fabricated: 5.5 µm width/ 4.5 µm space (min space ~ 3 µm)

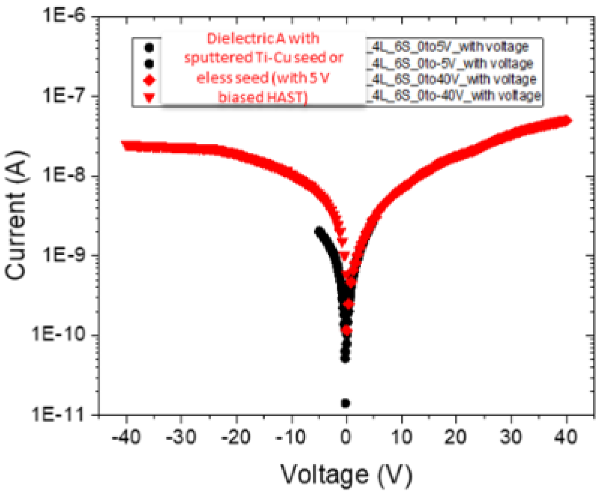
Chandra, Emanuel, Mohan

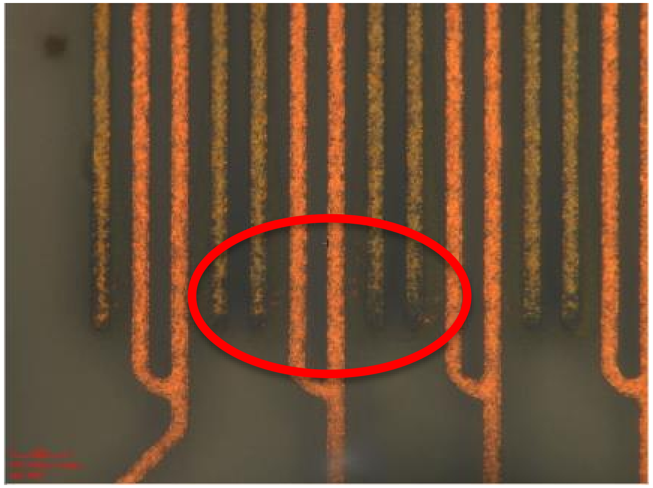
Results: Reliability of 2 µm RDL and Below

1.5 µm space

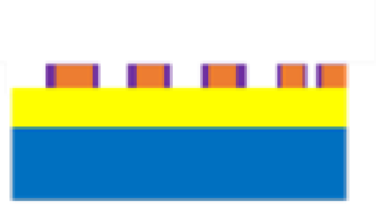


3 µm space



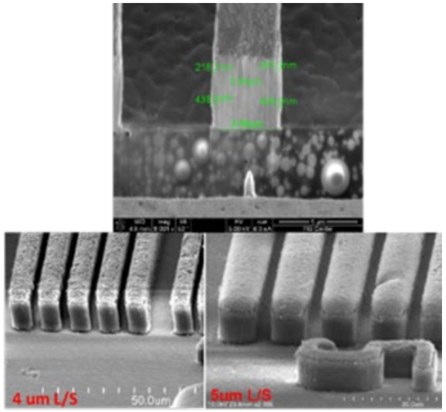


ECM failure in 1.5 µm space polymer RDL (0.6 wt.% moisture absorption)



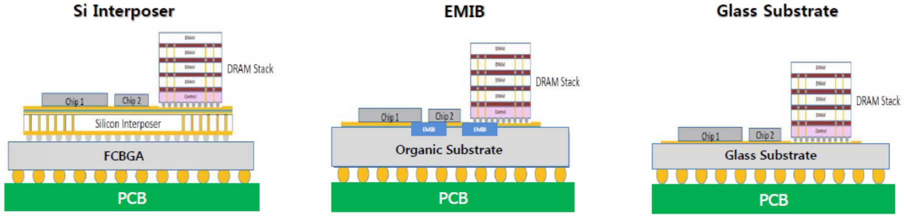
High aspect ratio copper traces with zero side etch (low R)- The thin parylene stays as a permanent dielectric in the RDL (low C)

- ✓ Copper particles in between polymer dielectrics ECM failure
- ✓ As spacing decreases to 2 µm and below, there is a need for a barrier to protect the migration of copper traces



Chandra, Emanuel, Mohan

Thermal Modeling



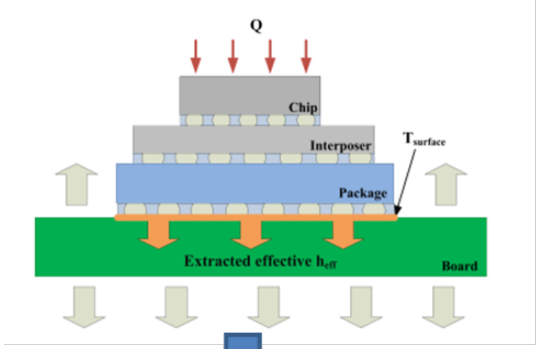
	Si Interposer	EMIB	Glass Substrate
Package Size	50x65mm^2	50x65mm^2	50x65mm^2
GPU	20x20.5mm^2	20x20.5mm^2	20x20.5mm^2
HBM2	7.7x11.5mm^2	7.7x11.5mm^2	7.7x11.5mm^2
Si Interposer	32x32mm^2	N/A	N/A
Si Bridge (EMIB)	N/A	6x6mm^2	N/A
FCBGA	50x65mm^2	50x65mm^2	N/A

Layer	Thickness (µm)	Thermal Conductivity (W/mK)	Specific Heat (J/K.Kg)	Mass Density (KG/m^3)
Case/Lid	150	350	385	8690
TIM (Case to die)	50	3	1000	2900
GPU/HBM	500	148	705	2329
Solder	-	50	234	7400
Underfill	-	0.28	915	1790
ILD	-	0.6	915	1790
Copper	-	400	385	8960
Glass Core (Glass Interposer)	540	1.1	480	2500
Silicon Core (Si Interposer)	500	148	705	2329
FCBGA Pkg (Si Interposer)	721	Kx=30.4 Ky=0.38	600	1850
PCB	1000	Kx=27.4 Ky=0.35	600	1850

Boundary Conditions

Ambient Temperature	40 °C
Forced Convection – Case 1: Air	100 W/m^{2}K
Forced Convection – Case 1: Liquid	1000 W/m^{2}K

Simplification of thermal model: Impact of BGA and PCB is simplified as **H_{eff}** (Only assuming forced air convection for PCB-side)



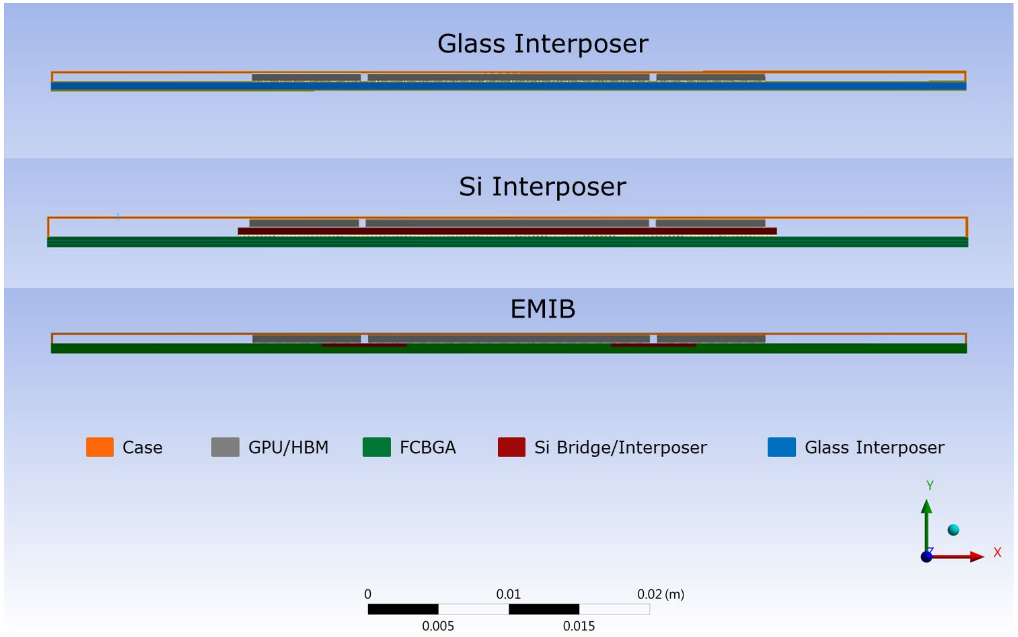
$$R = \frac{1}{h_{\text{eff}} \cdot A} = \frac{T_{\text{surface}} - T_{\text{amb}}}{Q}.$$

H_{eff} = 850 W/m^{2}K

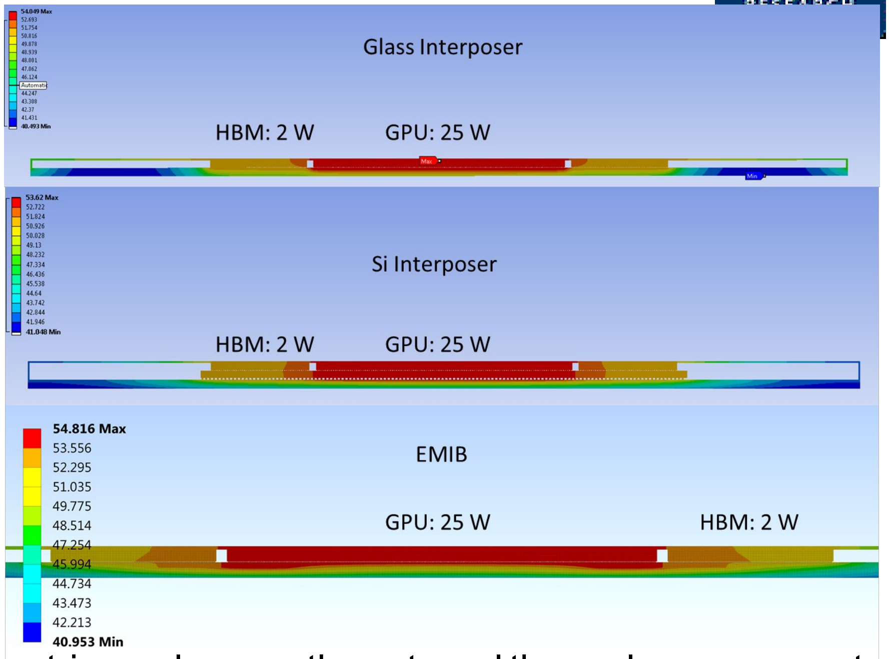
(Zhang. Y, et al. "Thermal Evaluation of 2.5-D Integration Using Bridge-Chip Technology: Challenges and Opportunities," IEEE Trans. on Components, Packaging and Manufacturing Technology, Vol 7, No. 7, July 2017).

Results (Preliminary) : Thermal Modeling

Package Geometries

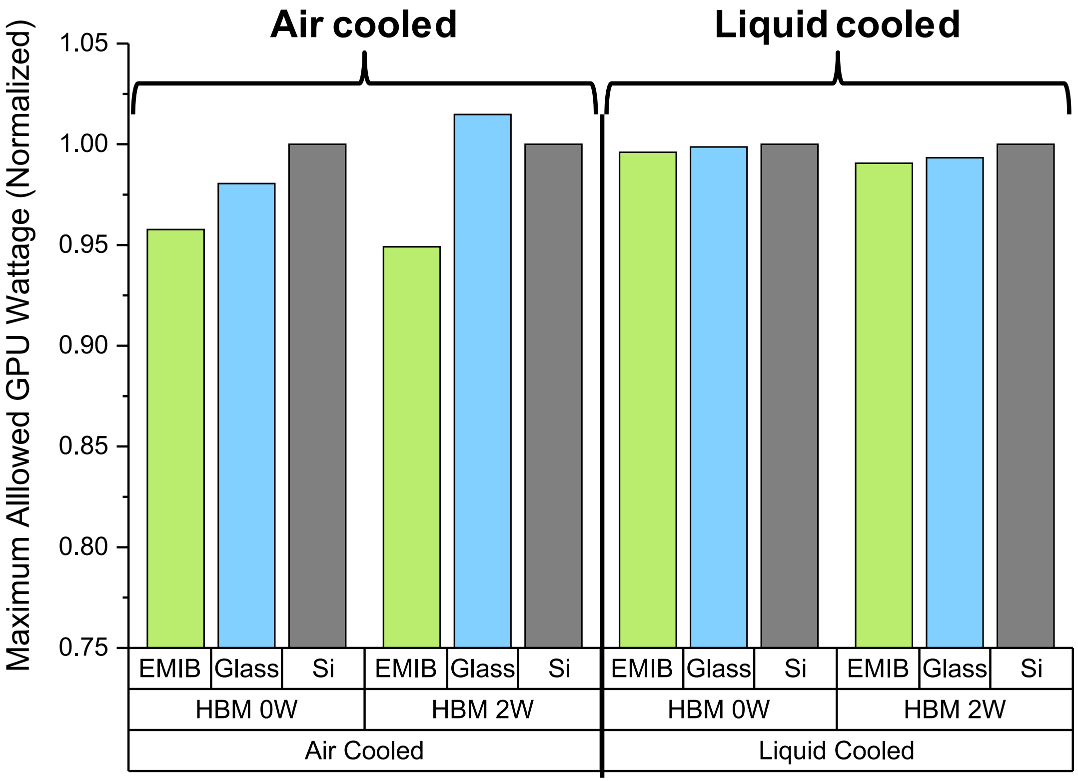


Temperature Maps



- ☐ Thermal performance of interposers similar to other geometries as long as the external thermal management is sufficient
  - ☐ Surface area of the lid/case used as a heat spreader in the model, plays an important role in heat exchange
  - ☐ Impact of the forced convection > thermal conductivity of the substrate
- ☐ Thermal isolation of the HBM is expected to be better in Glass which can be seen in the temperature map
  - ☐ HBM reaches 85^{0}C faster in Glass because of coupling through the TIM and Case. Thicker TIM/case with Glass may help avoid this problem
  - ☐ Modeling study including different thickness of TIM/case in Glass may help further understanding

Results (Preliminary): Thermal Modeling



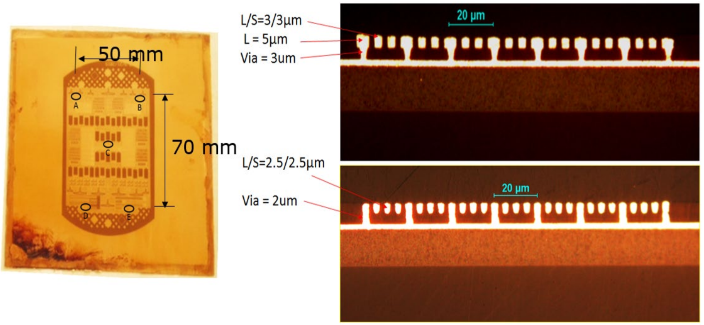
- ☐ Impact of cooling solution is more important than substrate material
- ☐ Large body size Interposers: Glass with ready availability at Panel scales and lower cost

Interposer Size: Opportunities and Challenges

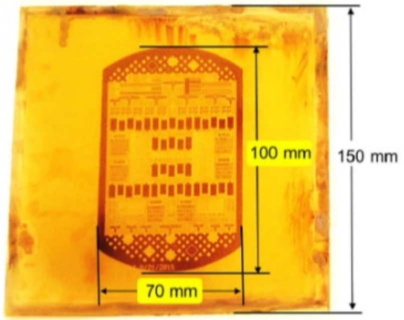
- AI systems require Large Interposers (> 1200 sq. mm)
- Great potential to increase the Glass interposer size
  - Glass has advantages over other materials in terms of Cost, and ready availability of Large Panels

- Challenges:
  - Materials
  - Lithography
  - Yield of L/S on Large Panels
  - Reliability

20-µm fine pitch RDL trench-to-via registration. (6” × 6” test vehicle)



70 mm × 100 mm test structures on 150-µm-thick glass with a single exposure



Ushio UX-44101: NA lower than 0.16. The resolution for the stepper is 2 µm.
Maximum Exposure region in Single Shot: 100 mm × 100 mm

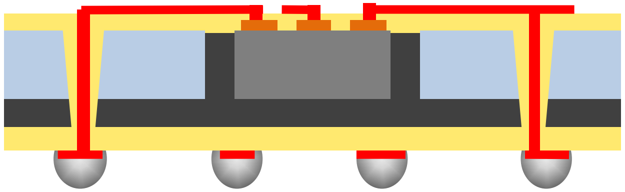
- *John H. Lau, “Overview and Outlook for Heterogeneous Integrations,” Chip Scale Review, 34-40, Sep-Oct, 2019.*
- *F. Liu, et al. “Low-Cost 1-µm Photolithography Technologies for Large-Body- Size, Low-Resistance Panel-Based RDL” IEEE Trans. On Components, Pkg and Manufacturing Technology, Vol. 9, No. 7, p 1426-1433, July 2019.*

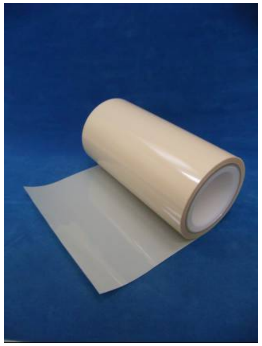
Results: Glass Panel Embedded (GPE) Package with Sheet type Molding Compound (SMC)

Advantages of the GPE Package

- ☐ Thin glass core: 100 mm x 100 mm x 60 µm thickness
- ☐ Chip Embedding: Small form factor & Low transmission Line Loss
- ☐ Robust PKG: Sheet type Epoxy Molding Compound

GPE with One chip





Ogura et al. IMAPS, Boston, September 30 - October 3, 2019.

Results: Glass Panel Embedded (GPE) Package with Sheet type Molding Compound

Glass core by Schott
  Glass size :100 x 100mm^2 x 60µmt
  Cavity size:7.4 x 7.4mm^2
  Via size :170-220µmφ

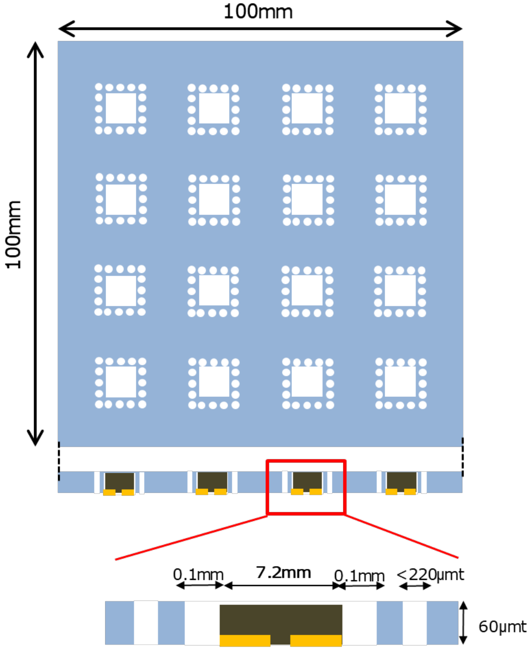
Chip by Global Foundry
  Chip Size :7.2 x 7.2mm^2 x 90µmt

Glass Carrier by AGC
  Glass Thickness: 1.1mm

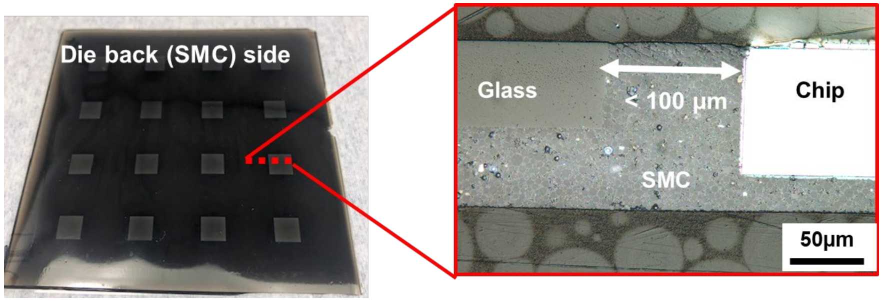
Temporary adhesion by Nitto
  Thermal release type: 170, 200 °C

SMC by Nagase ChemteX
  Sheet thickness: 20-40µmt

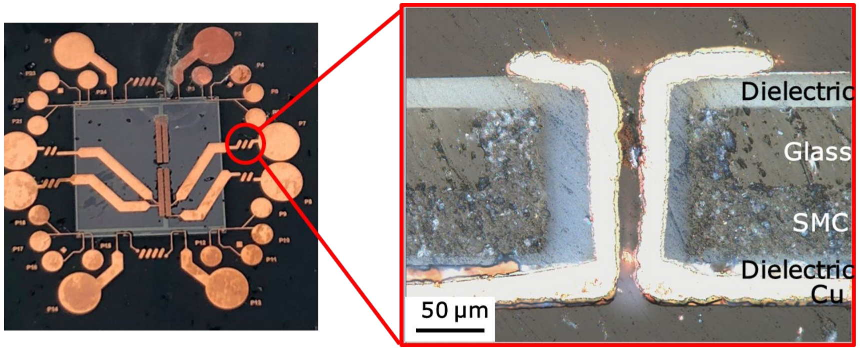
Materials



SMC was filled into a gap between Glass and Chip w/o void



RDL and Conductive Through Via

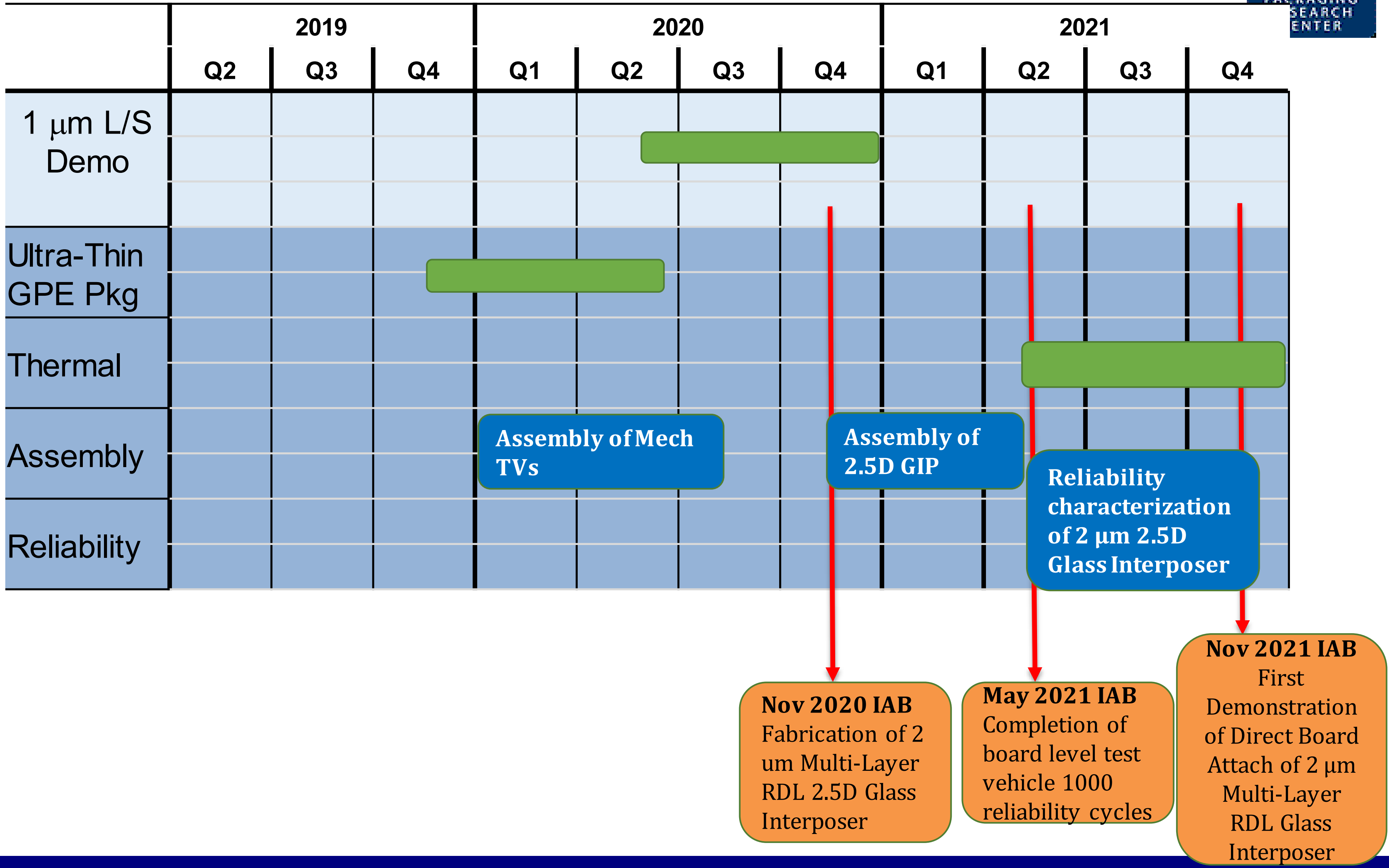


First demonstration of Glass Panel Embedded Package with 4" x 4" x 60 µm thick glass

Ogura et al. IMAPS, Boston, September 30 - October 3, 2019.

Schedule

🟩 Completed 🟨 Ongoing 🟦 Future task



Assembly of Mech TVs

Assembly of 2.5D GIP

Reliability characterization of 2 µm 2.5D Glass Interposer

Nov 2020 IAB
Fabrication of 2 um Multi-Layer RDL 2.5D Glass Interposer

May 2021 IAB
Completion of board level test vehicle 1000 reliability cycles

Nov 2021 IAB
First Demonstration of Direct Board Attach of 2 µm Multi-Layer RDL Glass Interposer

Summary

- Received the 12” wafer samples exposed at Canon: Cross-sectional SEM work in progress
- Thermal modeling suggests that Glass can have good thermal performance with good external thermal management.
- Larger GIPs has the potential to become the interposer choice for AI systems
- Glass Panel Embedded Package with 4” x 4” x 60 µm thick glass has been demonstrated for the first time.