2.5D Glass Interposer Application Test Vehicles: Status

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Outline

- Goals & Objectives
- Technical Approach
- Results
- Future Plan
- Summary

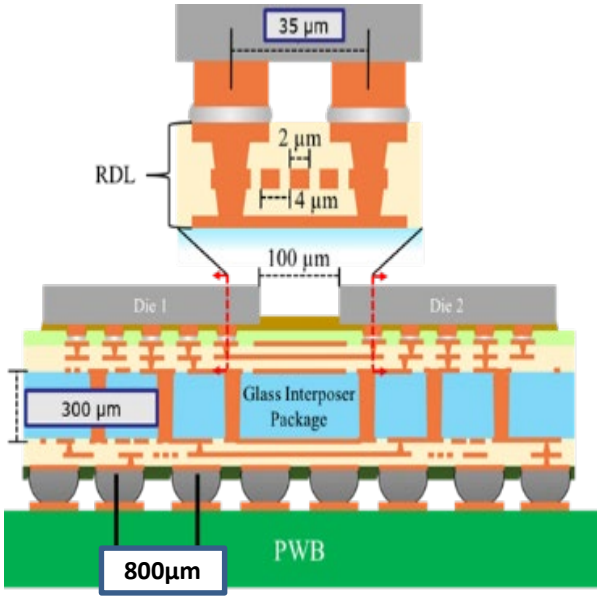
Goals and Objectives

- **Design and demonstrate a power efficient, higher bandwidth, lower-cost and higher reliability large body size 2.5D glass interposer as next generation to Si interposer**

Enabling Basic Technology Targets (2018-2020)

Parameter	Objective	Prior Art (Silicon Interposer)
Materials	Low-k dielectrics: k ~ 3	SiO_2: k ~ 3.8-4.0
Process	Double Sided SAP	Wafer Scale BEOL
Interconnect IO density	225 IOs/mm/layer (Low R and C)	250-400 IOs/mm/layer (High R and C)
Bump pitch (Chip level)	35 um (TCB)	45 um (TCB)
Body Size (Board Level)	40 mm x 50 mm (Mass Reflow)	28 mm x 36 mm (Mass Reflow)
Thermal	Advanced Direct Cu plated heat sink	Std. Heat Sink
Relative Cost	Low (Panel-Scale Processes) Large Body Size Feasible	High (Wafer-scale processes) Small Body Size feasible
Board Level Reliability	Direct Board Attach	Need Organic Package substrate

- ***RDL interconnects*** **approaching BEOL RDL with *lower R and C***
- **Fine pitch *chip-level interconnects***
- ***Direct attachment*** **to board**
- ***Low-cost large body size substrate***



Technical Approach

Materials

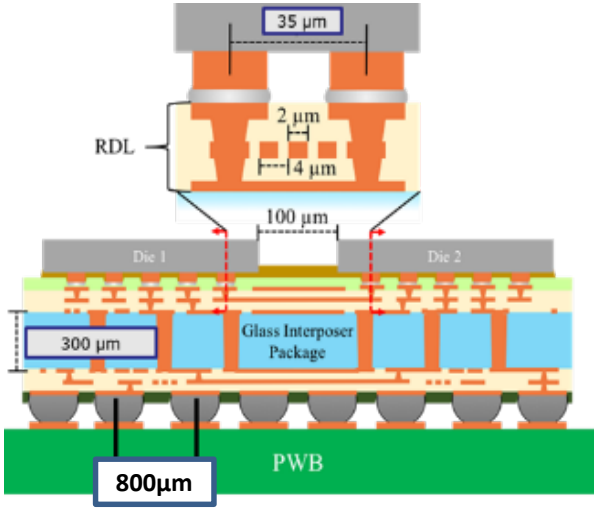
- Ultra-Thin, Low D_k Dielectrics
  - Panel Processable
  - Low CTE, Low Modulus, High Elongation to Break

Processes

- Panel-Scale Semi-Additive Process
  - Surface Planarization for High Yield RDL formation
  - End Point Seed Etch Detection

Low Cost

- Low Cost, Panel Scale Processes
- Large Body Size Substrates



Interconnects

- Low R, Low C 2 µm Multi-Layer RDL with 50 ohms impedance matching

Reliability

- RDL Reliability
  - Fine pitch traces and u-vias
  - Multi-Layer RDL Reliability on Glass
- Interconnect
  - Chip Level interconnects at 35 µm pitch
  - Board Level with 7 ppm/K CTE Glass core

Thermal

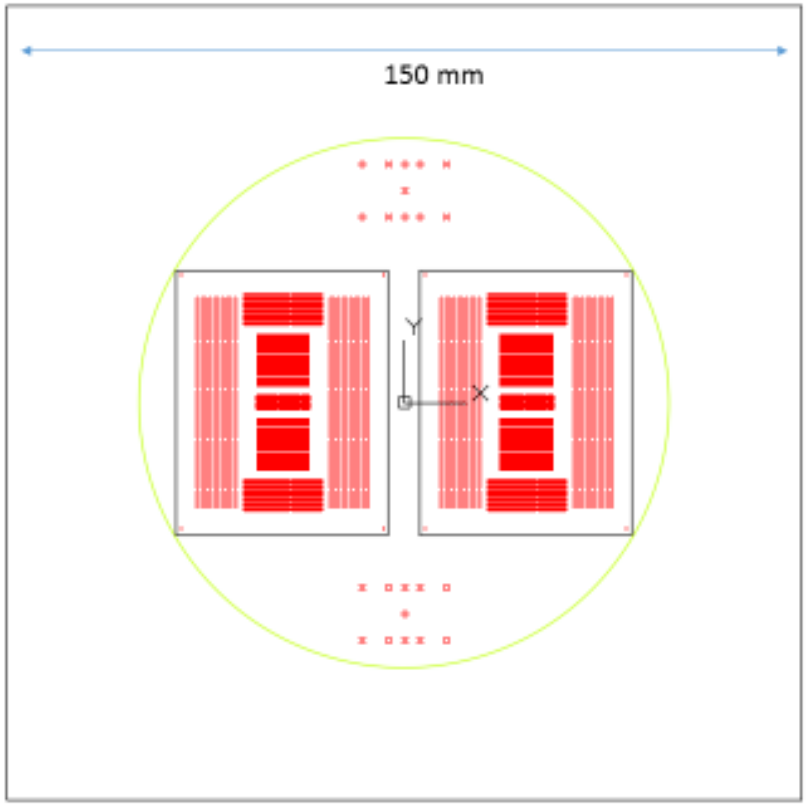
- Advanced Direct Cu plated heat sinks

Assembly

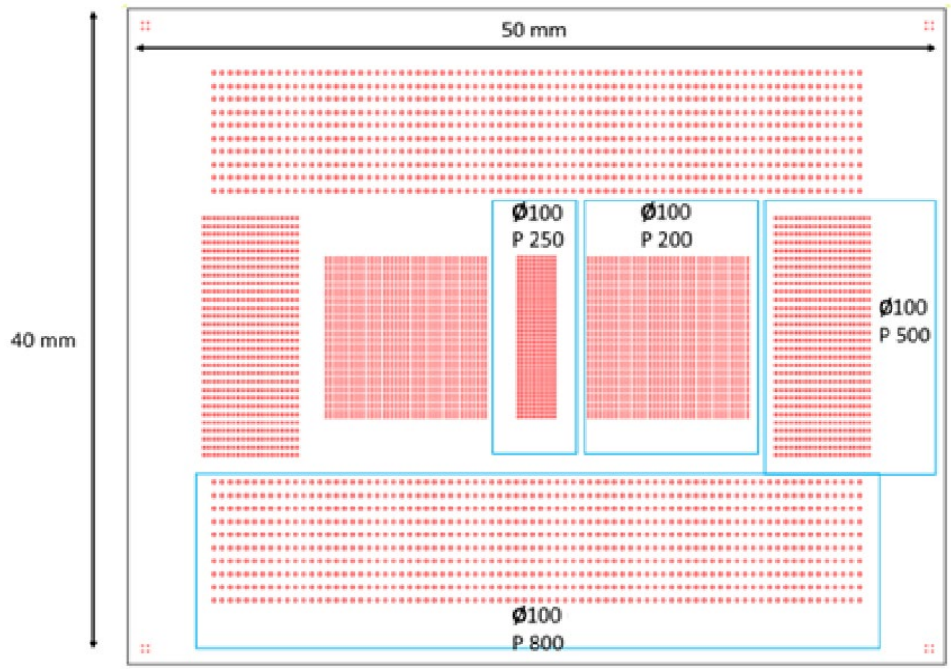
- Chip-level interconnect
  - TCB Cu pillar
- Board-level interconnect
  - Large body 30 mm x 40 mm SMT

Results: TGV Design

Lead: Siddharth



TGV map for 6”x6” glass panel



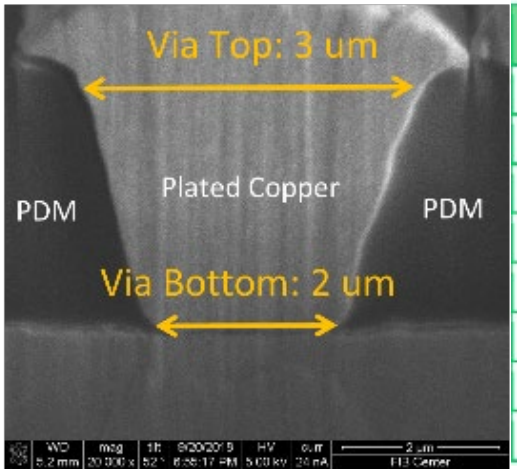
TGV map for single interposer

- **100 µm TGVs with pitch varying from 200-500 µm**
- **Optimized through via filing for vias down to 50 µm diameter and 300 µm substrate (6:1 aspect ratio)**
- **Study of metallization of TGVs to be done**

Results: Photo-Imageable Dielectric for fine line RDL

Lead: Kenny K (Taiyo), Pratik

- **Novel photo-dielectric for high resolution vias and L/S**
- **Good balance between low CTE and high resolution**
- **With low % elongation to break and smaller tensile strength, the goal is to maintain via taper angles between 64^0-90^0**
- **Low roughness thus optimization of sputtering needed for better adhesion and reliability**



Properties	Unit	PDM
Tg (@TMA)	(deg.C)	180 - 185
CTE alpha 1	(ppm)	30-35
Elastic Modulus	(GPa)	3.5 - 4.0
Tensile Strength	(MPa)	90 - 95
Elongation	(%)	5.5 – 6.0
Dk (10GHz)		3.3
Df (10GHz)		0.019
Water absorption	(%)	0.84

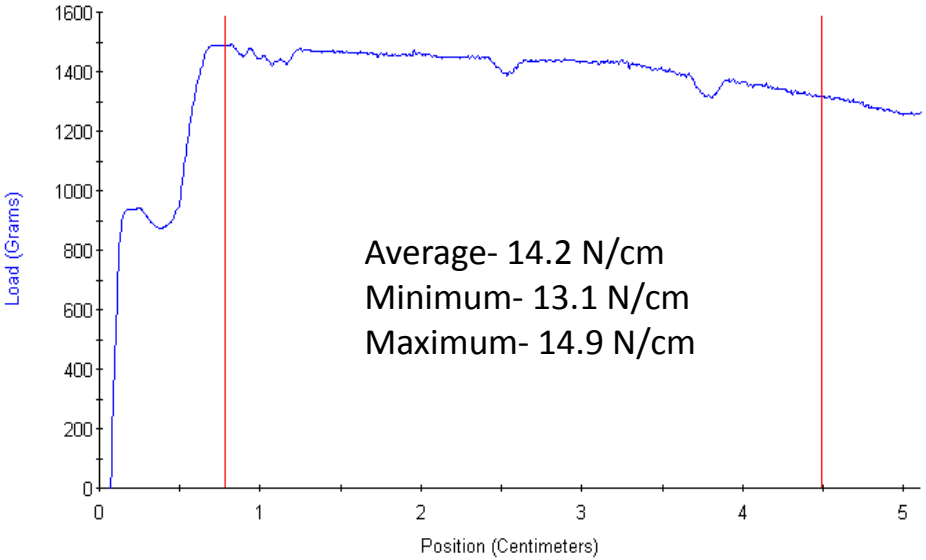
Conditions-

1) Plasma Treatment:

- **Ar plasma- 8.5 mins**
- **O_2 plasma- 2 mins**

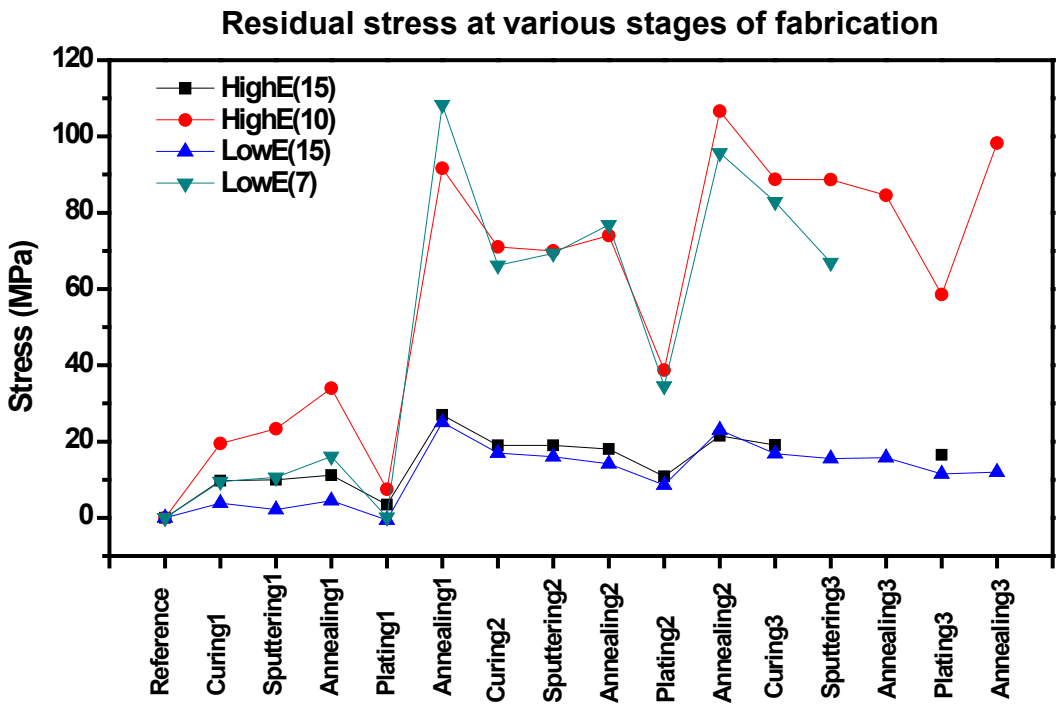
2) Pre-bake:

- **Temperature- 125°C**
- **Duration- 30 mins**
- **Pressure- $5x10^{-3}$ Torr**

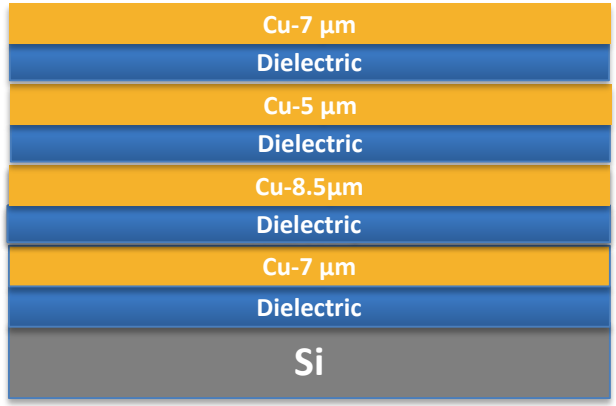


Results: ML-RDL Residual Stress Analysis

Lead: Pratik



Schematic stack up of dummy ML RDL

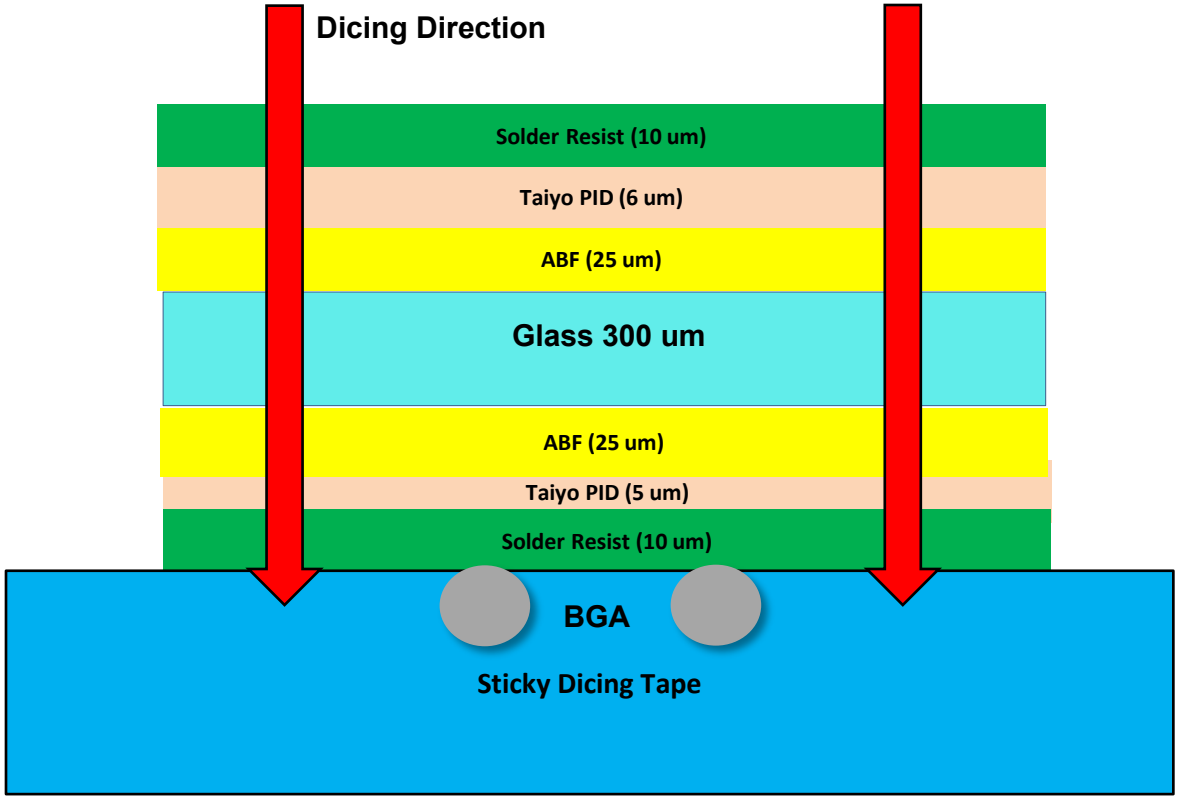


- **A thicker dielectric provides more stress relaxation as compared to thin dielectric**
- **For a dielectric having lower tensile modulus, stress is lower up to formation of the first metal layer**
- **As the number of metal layers goes on increasing, the stress starts levelling out**

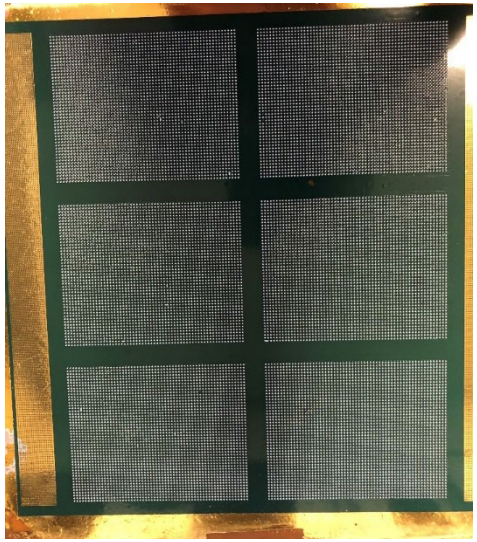
Results: Dicing Test Vehicle

Lead:
Pratik (Fabrication)
Omkar (BGA Balling)
Disco (Dicing)

Objective: Understand challenges and optimize the dicing conditions for glass BGA package with no over mold

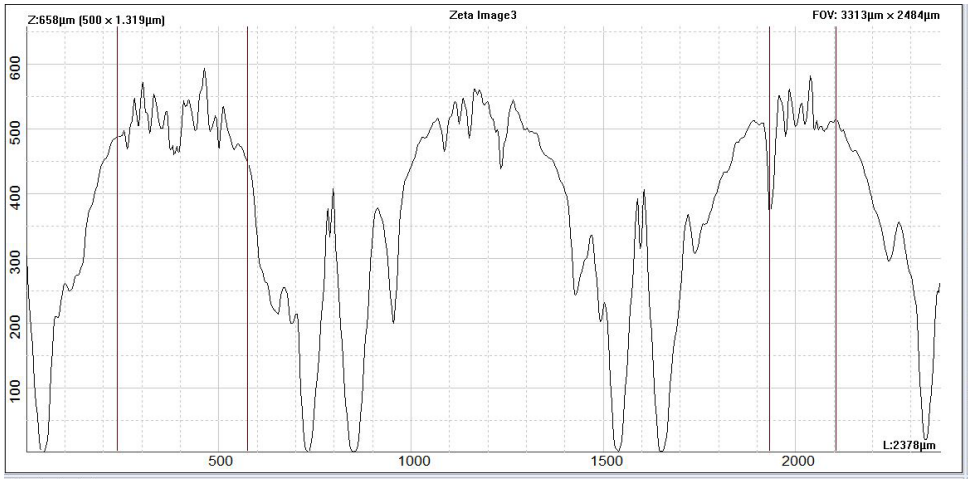


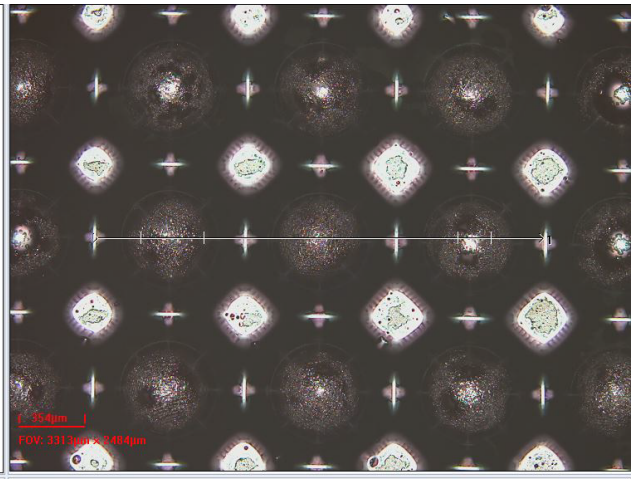
Good alignment with minimal ball bridging



- ✓ **Test Three Different Glass CTEs (3.4, 7.8 and 9 ppm/K) replicating Mechanical TV**
  - **300 µm thick glass with dielectric stacks**
  - **Only top and bottom metal layers**
  - **Fabrication completed**

Results: Dicing TV





Solder balls fabricated using solder paste printing and reflow

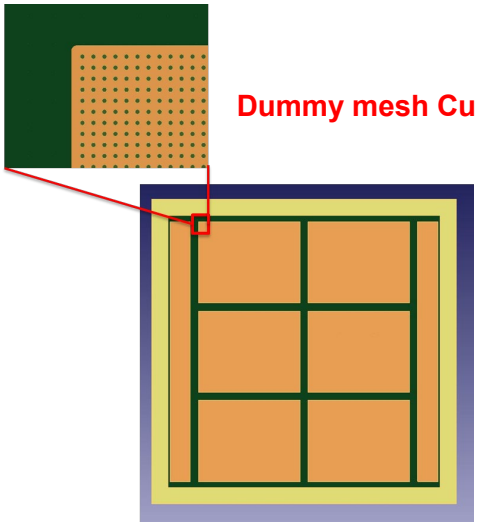
Solder ball diameter: 500 µm; BGA pitch: 800 µm

Solder ball height variation: 450 µm – 550 µm

Current TV status: Panels sent to Disco for dicing test on 10/30/2019

Results: Mechanical Test Vehicle - Board-Level Reliability

Lead:
Pratik (Fabrication)
Vanessa (Assembly)

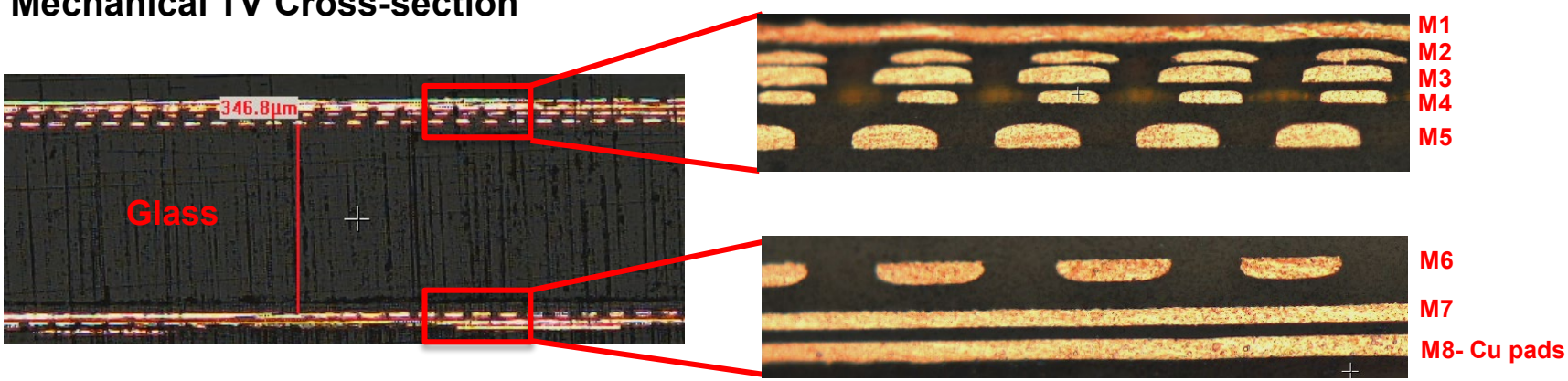


% Cu per layer

M1= 3 um thick	73 %
M2= 3 um thick	72 %
M3= 3 um thick	78 %
M4= 3 um thick	67 %
M5= 10 um thick	84 %
Glass 300 um	
M6= 10 um thick	84 %
M7= 5 um thick	87 %
M8 = 5 um thick	87 %

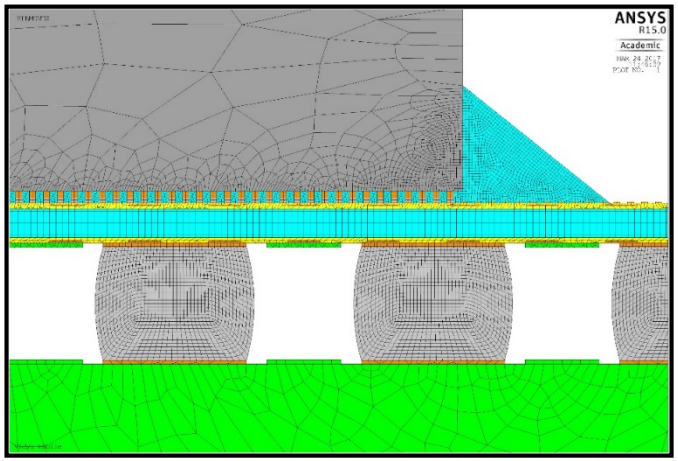
- ✓ **Test three different glass CTEs (3.4, 7.8 and 9 ppm/K) for board-level reliability**
  - **300 µm**
  - **No TGVs**
  - **Electrical routing structures to test board-level interconnections post thermal cycling reliability**

Mechanical TV Cross-section



Results: Prior Work

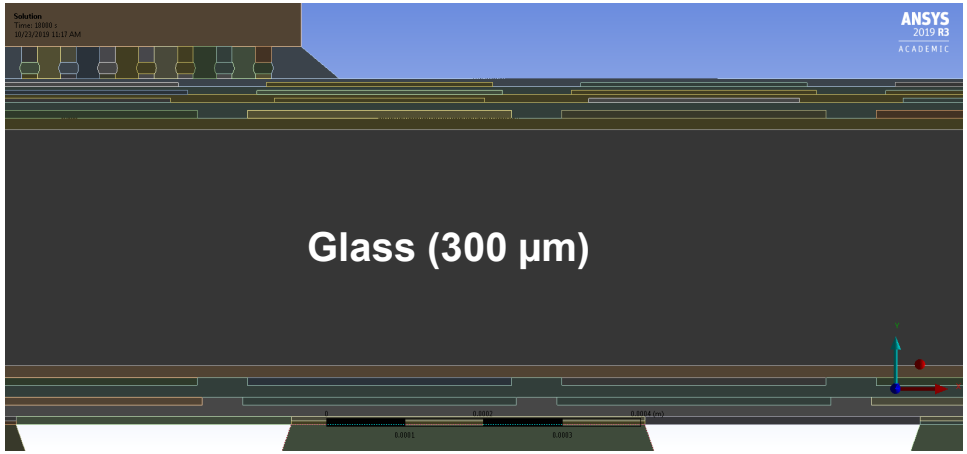
Reliability modeling for 2.5D glass interposer with 4 ML symmetric RDL stack-up



Glass CTE (ppm/K)	Package size (mm)	BGA diameter (um)	BGA pitch	Package thickness (um)	Nf (Coffin Manson)	Nf (Engelmaier Wild)
3.4	40 x 30	350	650	300	106	104
9	40 x 30	350	650	300	918	1389
9	40 x 30	350	650	100	1162	1844
9.8	40 x 30	350	650	300	1099	1724
9	50 x 40	350	650	300	928	1408
9	60 x 50	350	650	300	1097	1721
9	50 x 40	500	800	300	1395	2295
7.8	50 x 40	500	800	300	1283	2076
3.4	50 x 40	500	800	300	520	703

Thermomechanical modeling

Thermomechanical modeling with 8 ML asymmetric RDL stack-up



- FEA model with 8 ML asymmetric stack-up to understand the effect of glass CTE on the board-level and chip-level reliability
- The model doesn't account for the warpage considerations during the process

BGA pitch: 800 µm
BGA diameter: 500 µm

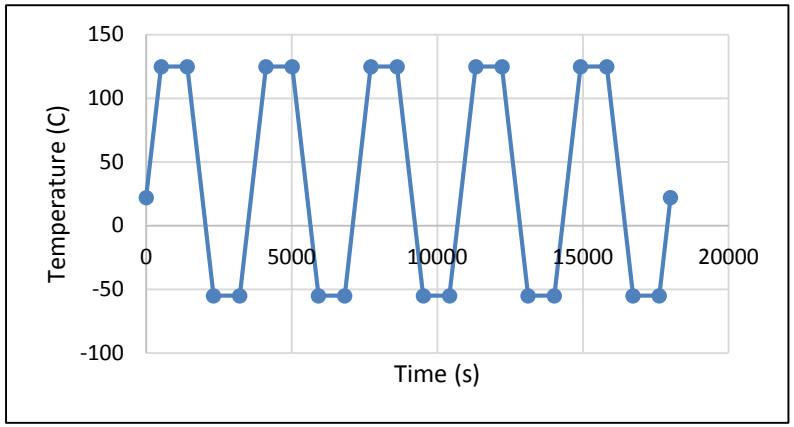
Model assumptions:

- Quarter symmetric 2D model along the diagonal of the chip and package
- Considered the bump pitch (35µm) and dimensions of the GPU die
- Geometry modeled with plane strain elements

Material parameters and assumptions:

- Chip level solder: Sn3.5Ag with Anand viscoplasticity
- Board level BGA: SAC305 with Anand viscoplasticity
- Copper: Bilinear kinematic hardening

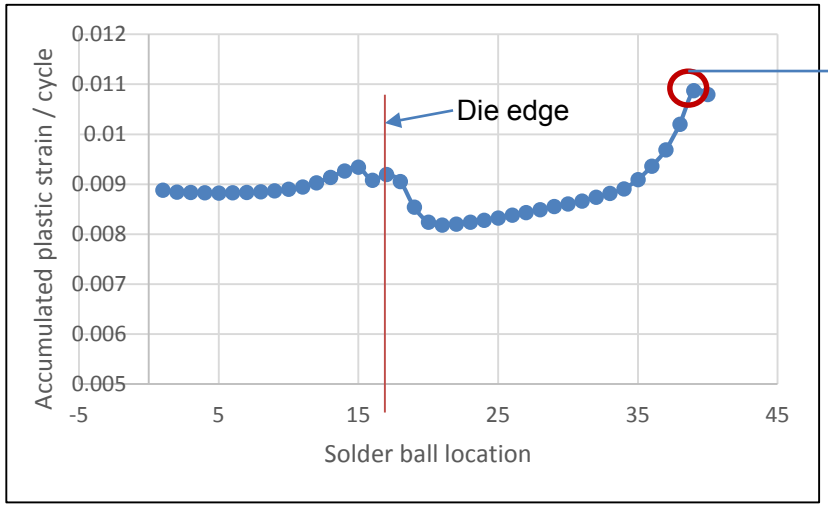
Thermal loading profile



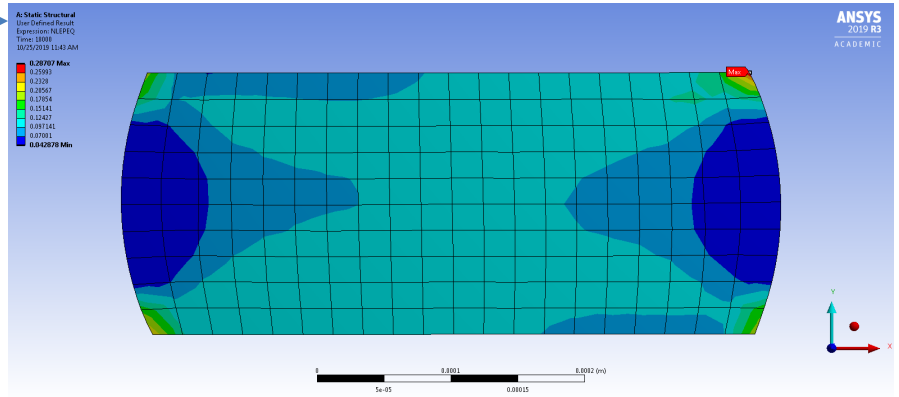
Results: Thermomechanical modeling

Thermomechanical modeling with 8 ML asymmetric RDL stack-up – Board level

Accumulated plastic strain per cycle in BGA with solder ball location



Distribution of accumulated plastic strain in the second last solder ball for high CTE (9 ppm/K) glass substrate



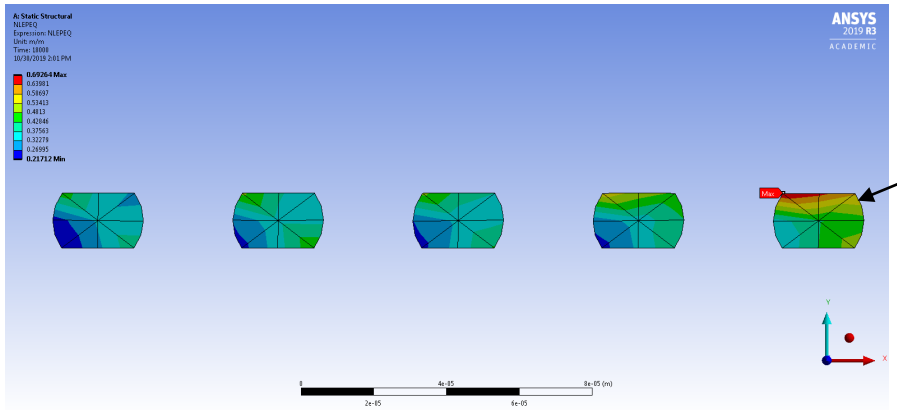
Glass CTE (ppm/k)	Package size (mm)	BGA diameter	BGA pitch	Nf (Coffin Manson)	Nf (Engelmaier Wild)
3.4	40 x 50	500 µm	800 µm	781	>5000
7.8	40 x 50	500 µm	800 µm	1133	>5000
9	40 x 50	500 µm	800 µm	1171	>5000

Actual number of cycles typically lie between the predictions of the two theoretical models

Results: Thermomechanical modeling

Thermomechanical modeling with 8 ML asymmetric RDL stack-up – Chip level

Accumulated plastic strain distribution in chip-level solder interconnects



Last solder bump (at die edge)

Size factor used to compare chip-level and board-level reliability

Glass CTE (ppm/K)	Package size (mm)	Solder bump height	Solder bump pitch	Nf (Coffin Manson)
3.4	40 x 50	15 µm	35 µm	19728
7.8	40 x 50	15 µm	35 µm	5112
9	40 x 50	15 µm	35 µm	4539

Expected to pass chip-level reliability with all CTEs

Summary

- TGV design is complete
- Optimized sputtering conditions for improved adhesion and reliability of RDL
- Dicing test vehicle fabrication has been completed and panel sent to Disco for dicing test on 10/30/2019
- Mechanical test vehicle fabrication is ongoing
- Thermomechanical modeling: packages with 8 ML asymmetric stack-up and high CTE glass core (7.8 and 9 ppm/K) expected to pass 1000 thermal cycles

Schedule

Completed | Ongoing | Future task

	2019			2020				2021			
	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Design	Fully Integrated 2.5D GIP with bump pitch 35 µm & board pitch 800 µm										
Fabrication	Fabrication of Mech TVs with 3 different CTE glass cores				Fabrication of 2.5D Interposer with 2 µm RDL						
Assembly				Assembly of Mech TVs		Board-level reliability tests with Mech TVs	Assembly of 2.5D GIP		Reliability characterization of 2 µm 2.5D GIP		

Nov 2020 IAB Fabrication of 2 um Multi-Layer RDL 2.5D Glass Interposer

May 2021 IAB Completion of 1000 thermal cycles for Mech TV reliability

Nov 2021 IAB First Demonstration of Direct Board Attach of 2 µm Multi-Layer RDL Glass Interposer