Advanced Panel RDL Technologies for High Performance Computing (HPC) Applications

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- ❑ Prior Work
- ❑ Technical Approach
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Goals and Objectives

❑ Modeling, Design and Demonstration of 1μm Low RC Panel RDL Technology for HPC

	Parameters	Si BEOL RDL	Current Panel RDL	Proposed RDL
Modeling	• Aspect Ratio	• 1-2	• 1-2	>4
	• Conductor Width/Spacing	0.8/0.8 μm	6/6 μm	1/1 μm
Design	• Single-Ended Impedance (Z_o in Ω)	• 47	• 55	• 50
	• Data Rate Per Channel (Gbps)	• 2	• 2-5	>10
Materials • (Photoresist)	• Thickness • Chemical Composition • Exposure Mechanism • Type • Substrate Compatibility	• Ultra-thin <1 μm • Chemically Amplified • Polarization • Liquid PR • Wafer	• Thick >10 μm • Non-Chemically Amplified • Polymerization • Dry Film PR • Panel	• Thin < 7 μm • Chemically-Amplified • Polarization • Dry-film PR • Panel
Tools (Lithography)	• NA • DOF	• >0.28 • ±1.88 μm	• <0.13 • ±10 μm	• 0.18 – 0.24 • ±4.2 μm
Processes	• RDL Formation • Metallization	• Dual Damascene • PVD Seed	• SAP • Electroless Seed	• Advanced SAP • PVD Seed

Prior Work

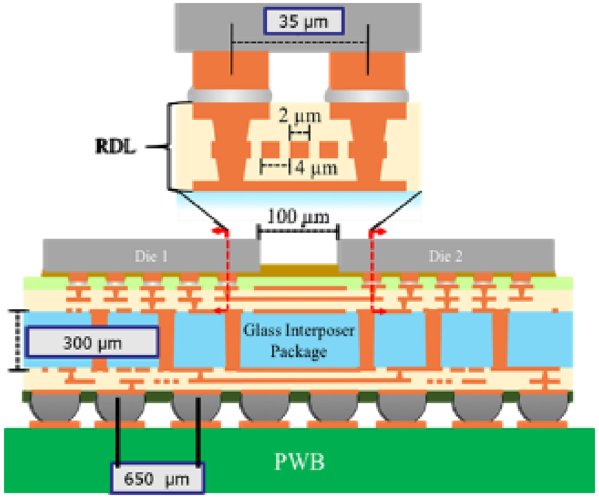
- **Explored the difference between Liquid and Dry films specifically around performance on rough dielectric surfaces**
- **Demonstrated planarized multi-layer SAP with 4 µm diameter microvias**
- **Demonstrated 2 µm microvias in no filler dielectrics and nano-sized filler dielectrics**
- **Worked with AMAT to develop a new highly selective wet chemistry for seed layer etch**

Technical Approach

Materials
- Ultra-Thin, Low D_k Dielectrics
  - Panel Processable
  - Low CTE, Low Modulus, High Elongation to Break

Processes
- Panel-Scale Semi-Additive Process
  - Surface Planarization for High Yield RDL formation
  - End Point Seed Etch Detection

Interconnects
- Low R, Low C 2 um Multi-Layer RDL with 50 ohms impedance matching



Low Cost
- Low Cost, Panel Scale Processes
- Large Body Size Substrates

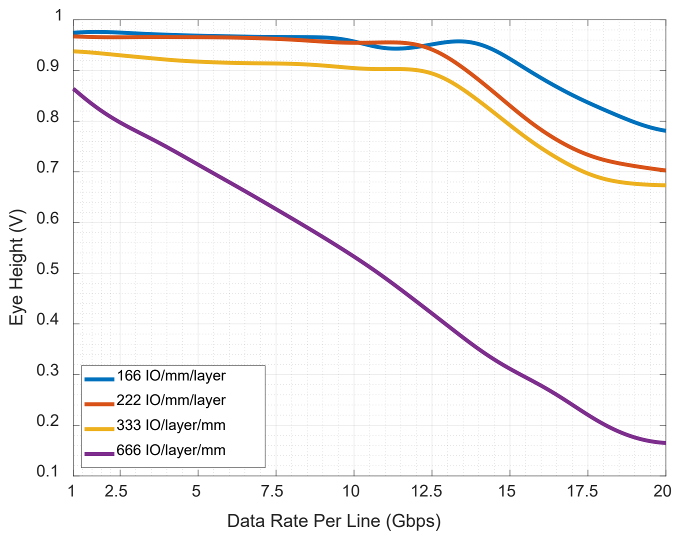
Reliability
- RDL Reliability
  - Fine pitch traces and u-vias
  - Multi-Layer RDL Reliability on Glass
- Interconnect
  - Chip Level interconnects at 35 um pitch
  - Board Level with 7 ppm/K CTE Glass core

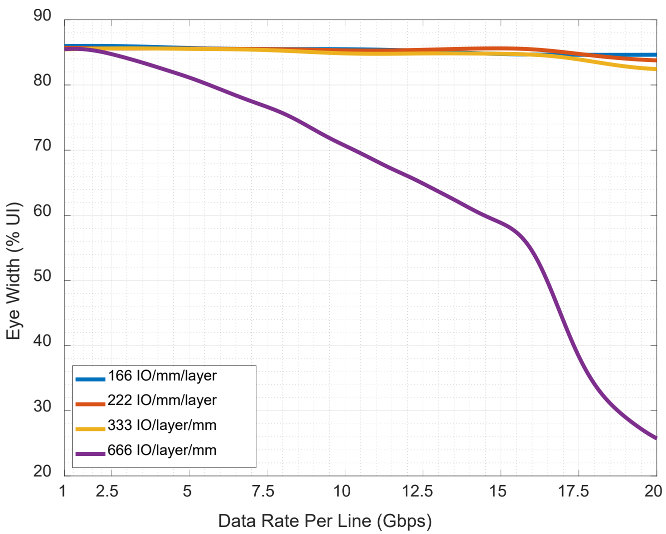
Assembly
- Chip-level interconnect
  - TCB Cu pillar
- Board-level interconnect
  - Large body 30 mm x 40 mm SMT

Thermal
- Advanced Direct Cu plated heat sinks

Results & Key Accomplishments

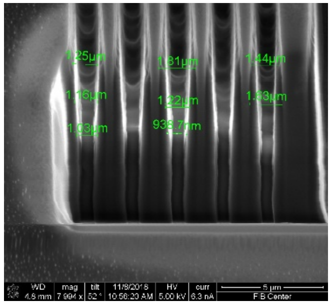
- Optimal I/O Density Design Rules for Maximum Data Rate per Channel – Hakki Torun



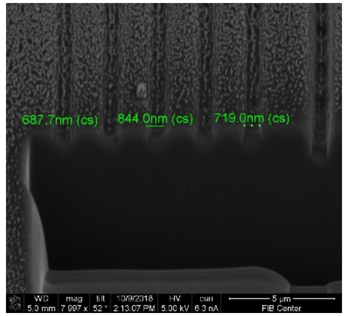


IO Density	Optimal Width/Spacing/Aspect Ratio	Max Data Rate per Line	Achievable Aggregated Bandwidth
166 IO/mm/layer	$1\mu m/10\mu m/1.2$	18.9 Gbps	3.14 Tbps/mm/layer
222 IO/mm/layer	$0.5\mu m/8\mu m/3.6$	15.6 Gbps	3.46 Tbps/mm/layer
333 IO/mm/layer	$0.5\mu m/5\mu m/4.2$	14.8 Gbps	4.93 Tbps/mm/layer
666 IO/mm/layer	$0.5\mu m/2\mu m/3.0$	2.4 Gbps	1.59 Tbps/mm/layer

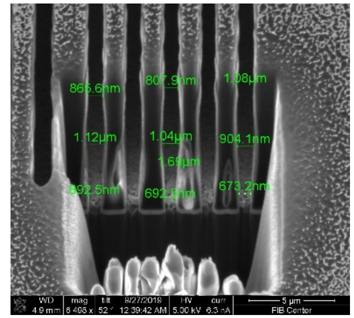
Results: Seed Layer Reflectivity Study



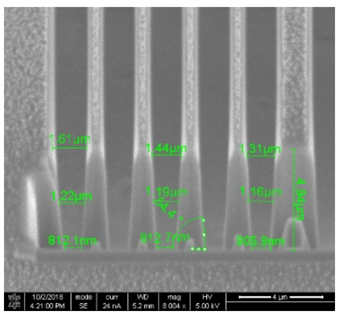
Cu @ 1200 J/m²



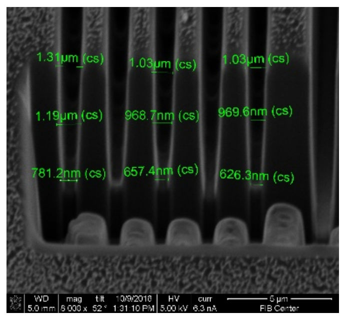
Cr @ 1200 J/m²



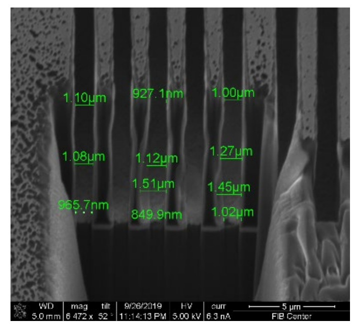
Ag: 1200 J/m²



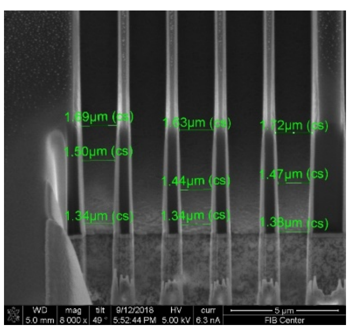
Cu @ 1600 J/m²



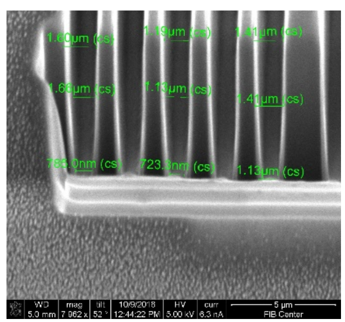
Cr @ 1600 J/m²



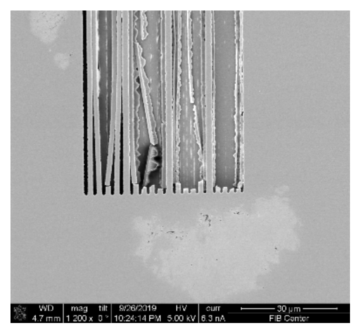
Ag @ 1600 J/m²



Cu @ 2000 J/m²



Cr @ 2000 J/m²



A @ 2000 J/m²

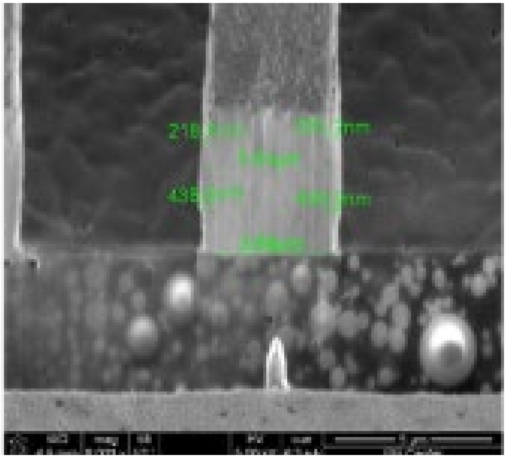
- **Copper Reflects at 45%, Chromium at 23% and Silver reflects above 95% at 365 nm**
- **Optimum dose increases with a reduction in reflectivity**
- **Optimum dose decreases with an increase in reflectivity**

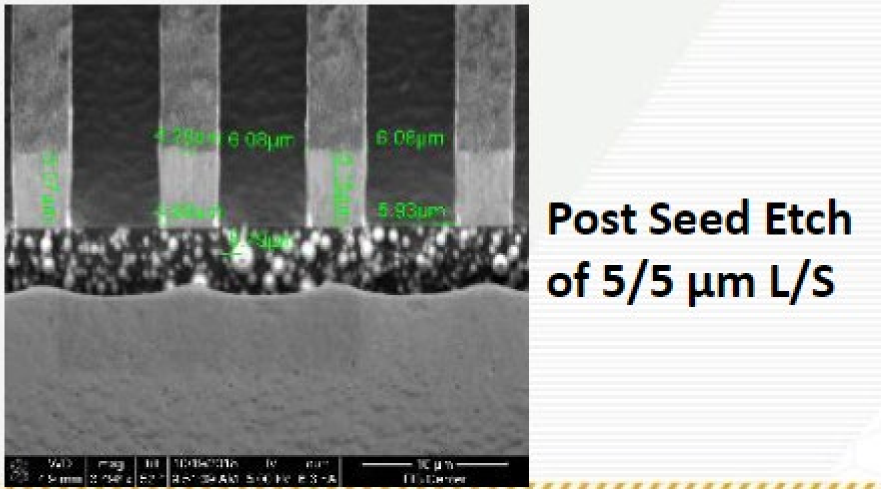
Results and Accomplishments: Provisional Patents

- Provisional Patent 1: SP – SAP (Sidewall Protected SAP)
  - Chandra Nair, Bart DeProspo, Omkar Gupte, Rao Tummala
  - Wet chemical etching is extremely isotropic and attacks all portions of the RDL traces during seed layer removal. This disclosure is designed to induce an anisotropic aspect to this process for extending SAP to 1 μm and beyond.

- Provisional Patent 2:SAV – SAP (Self-Aligned Via SAP)
  - Bart DeProspo, Chandra Nair, Emanuel Surillo, Rao Tummala
  - Electronics packaging utilizes laser technology to define the layer to layer via connections. The resolutions of these technologies is beginning to reach their limitations and taper angles are extremely high and require large pads for scaling. This disclosure's main benefit is around using a PR To scale via resolution and also to try and remove the large pad structures.

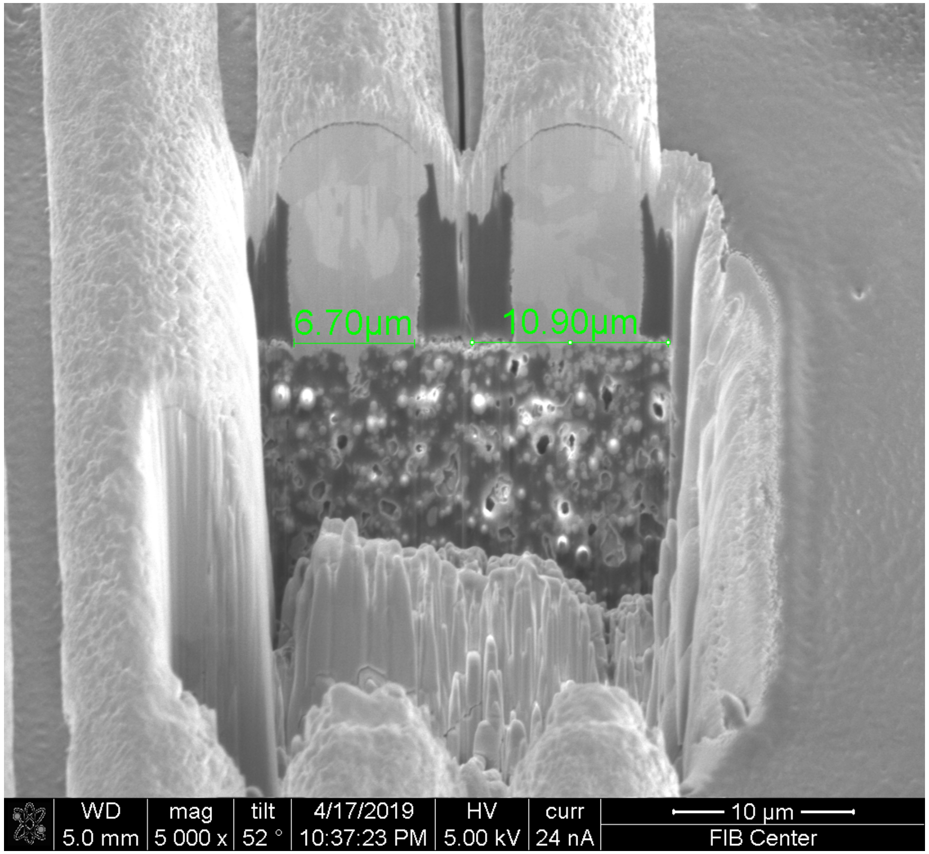
Results: SP – SAP First Process Demonstration



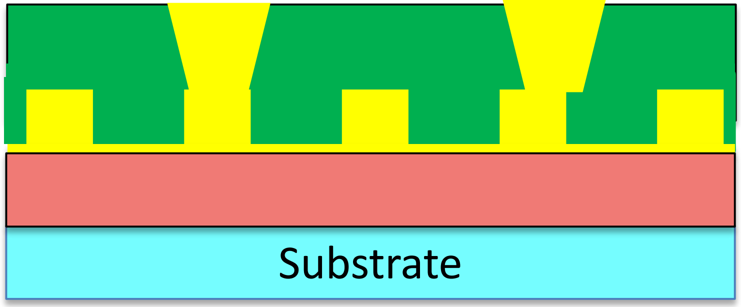


- Deposited 500 nm of parylene film onto the sidewall of copper traces using a CVD room temperature process
- The dielectric constant of parylene film is ~2.4 enabling low capacitance RDL
- As seen across the images there was no undercut of the trace during this process.
- Goal is to demonstrate this process in the future on line and space features that are ≤ 1µm CD working with partner companies.

Results: SAV – SAP First Process Demonstration

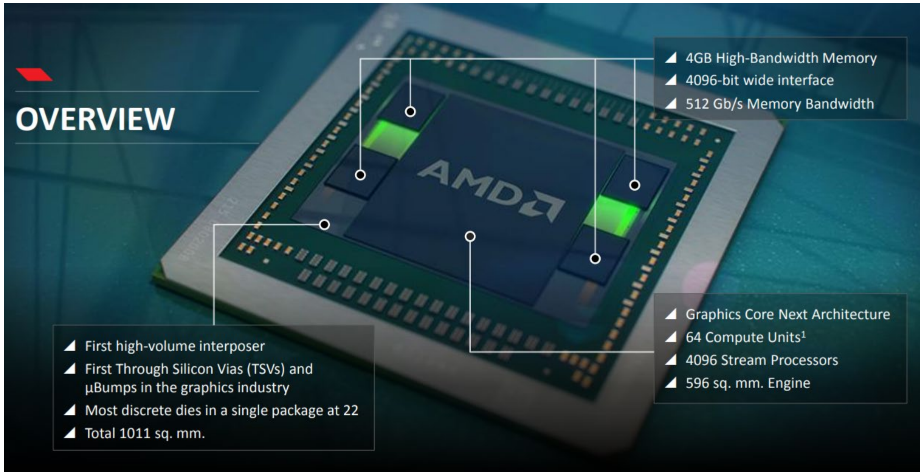


Strip Photo-imageable material and deposit dielectric

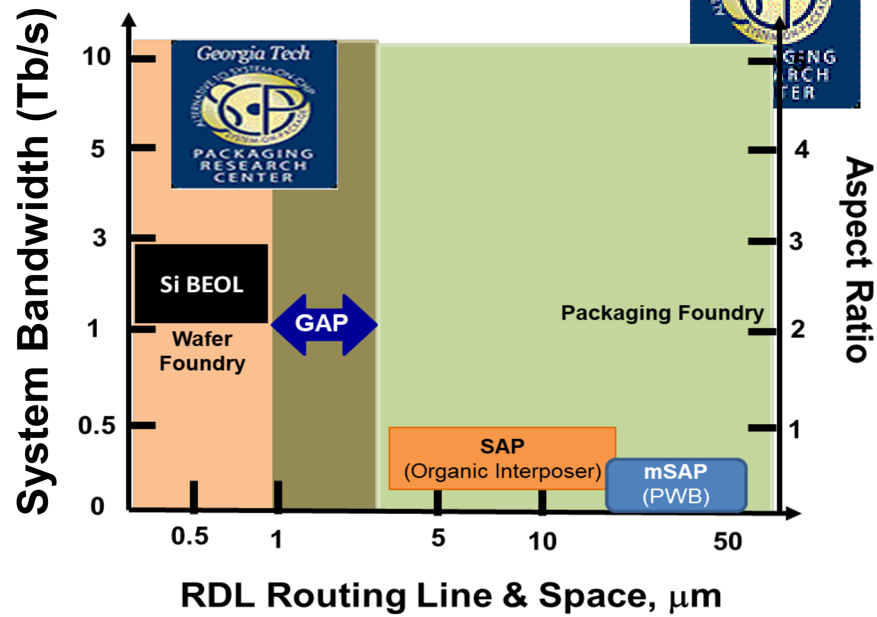


- **Goal for this work is to induce some misalignment at GT and test the limit of this process**
- **Design work suggests that highest performance system isn't necessarily matched in terms of line and space**

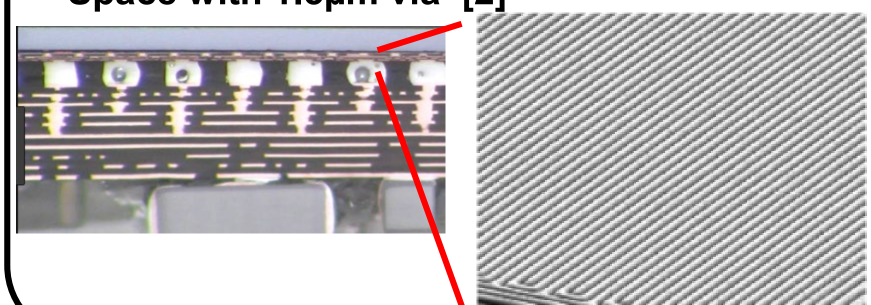
HPC Computing Landscape



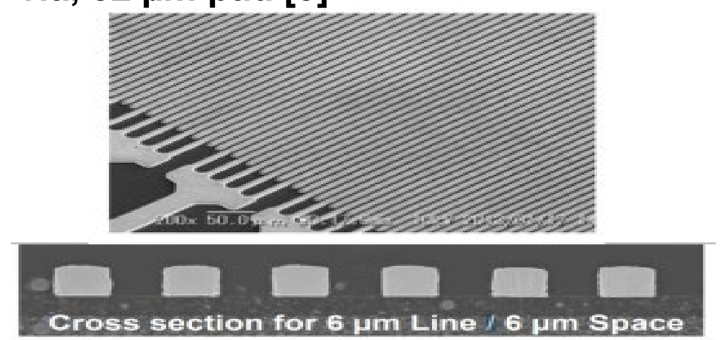
AMD Fiji GPU [1]



Current Silicon BEOL RDL: 0.8 µm Line and Space with 1.5µm via [2]

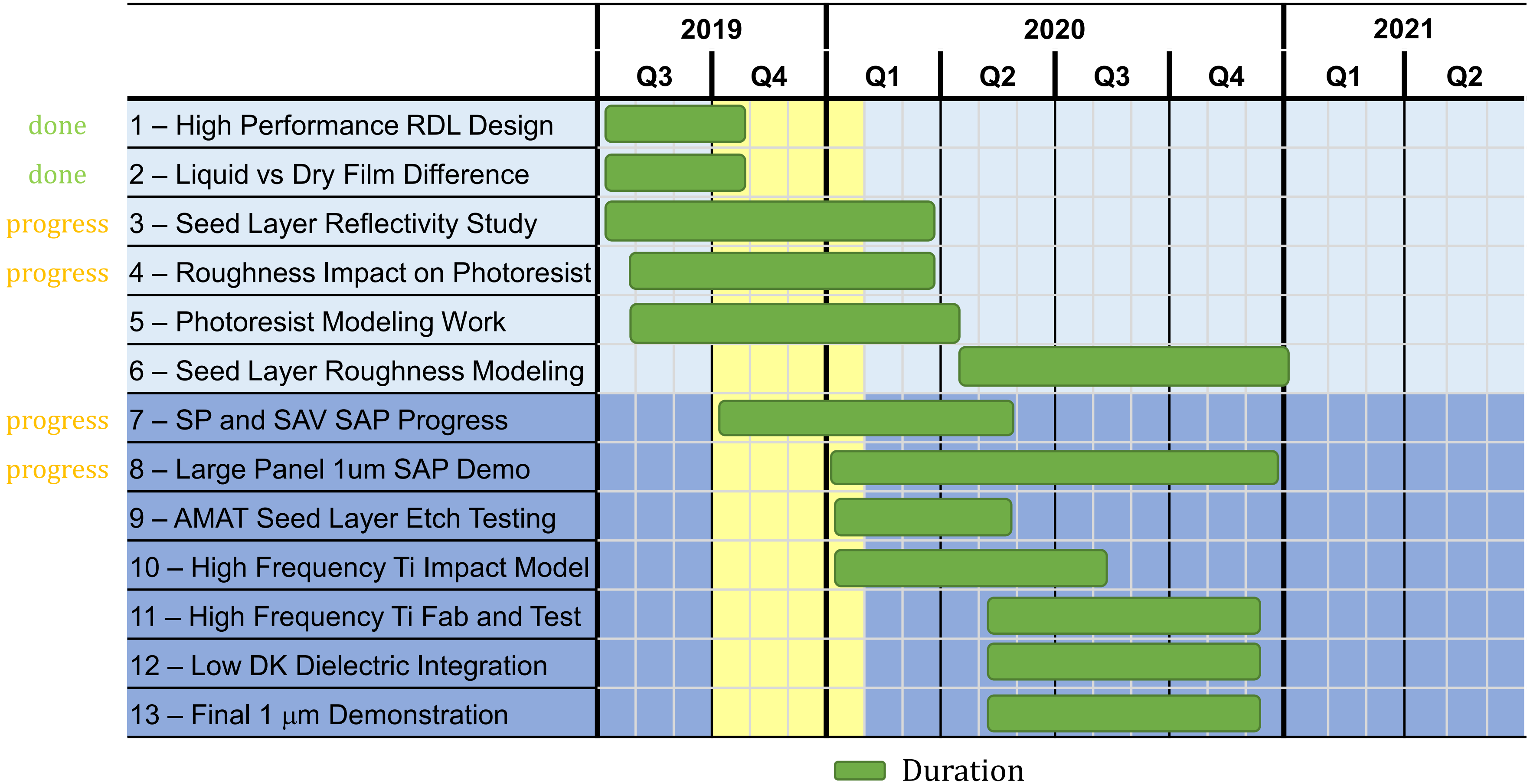


Current Panel RDL: 6 µm L/S, 20 µm via, 32 µm pad [3]



Require High I/O Density RDL with Low Resistance capable of enabling High Bandwidth Systems on Panel RDL

Schedule


2019
2020
2021
Q3
Q4
Q1
Q2
Q3
Q4
Q1
Q2
done
1 – High Performance RDL Design
done
2 – Liquid vs Dry Film Difference
progress
3 – Seed Layer Reflectivity Study
progress
4 – Roughness Impact on Photoresist
5 – Photoresist Modeling Work
6 – Seed Layer Roughness Modeling
progress
7 – SP and SAV SAP Progress
progress
8 – Large Panel 1um SAP Demo
9 – AMAT Seed Layer Etch Testing
10 – High Frequency Ti Impact Model
11 – High Frequency Ti Fab and Test
12 – Low DK Dielectric Integration
13 – Final 1 μm Demonstration
Duration

Summary

- Completed Electrical Design work for high performance RDL design
  - Courtesy of Hakki Torun
- Fabricated and analyzed impact of seed layer reflectivity on photoresist performance
- Filed provisional patent on new sidewall protected semi additive process