Ultra low-k (<3) panel RDL dielectric materials, processes and characterization

Student: Shreya Dwarakanath
Faculty: Prof. Tummala, Prof. Swaminathan, Prof. Losego

Industry Partners:
Takenori Kakutani (Taiyo), Atsushi Kubo (TOK), Shohei Fujishima (AJT),
Kimiyuki Kanno (JSR)

Outline

- ☐ Goals & Objectives
- ☐ Strategic Need
- ☐ Technical Approach Beyond Prior Art
- ☐ Research Highlights
- ☐ Results
- ☐ Summary
- ☐ Project Plan

Objectives

GOAL: Develop RDL dielectric materials and processes to meet next generation interconnect needs for high bandwidth.

		Parameters	Target	Prior Art	Research Tasks
Materials	Electrical	D_k	<3.0 (1 MHz-GHz)	>3.0	1. Evaluating performance improvement with low D_k dielectric materials for HPC architectures
		D_f	<0.001	>0.014	
	Physical	Thickness	0.5-5 µm	10-75 µm	
	Mechanical	Elongation to failure	>30%	2.5– 45%	
	Chemical	Moisture absorption	< 0.2 wt. %	0.2 – 1.5 wt.%	
Process	Planarity	DOP	<1-3 µm	-	2a. Fabrication of test-structures to quantify DOP with upfront material candidates
	Lithography	Resolution	< 2 µm line/space	> 2 µm line/space	2b. Develop RDL patterning and metallization processes for low D_k dielectrics
		Via	1-5 µm via	> 5 µm via	
Characterization	Electrical	Crosstalk	0.1 mV	0.3 mV	3a. Characterize electrical performance metric with low-k, ultra-thin dielectrics
	Physical	Dielectric height	<2 µm	>10 µm	
	Mechanical	Residual Stress	<25 MPa	-	3b. Characterization of maximum tolerance of residual stress in dielectric lamination and metallization
	Chemical	Adhesion	>0.3 kgf/cm	0.2 – 1 kgf/cm	3c. Investigating surface modification to improve adhesion of low D_k materials to seed layer

Strategic Need:

Ultra-low D_k dielectrics materials for high-speed and ultra-thin dielectrics for impedance matching

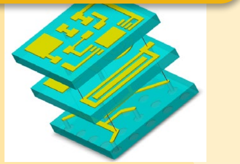
Dielectric thickness

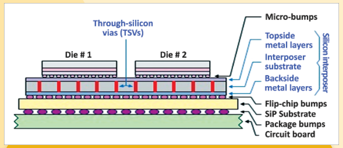
<2 µm | 7 µm | 15 µm | 20 µm | >100 µm

Dielectric constant: 9, 4, 3, 2.5

Signal Speed (cm/ns): 10, 15, 17, 20

Ceramic based packages with metal oxides as dielectric





Silicon interposers based packaging with SiO_2

Polymers for printed circuit boards and other laminate based packages

Thin-film polymers for high-density organic substrates

Need for ultra high-bandwidth

Advanced Polymer Dielectrics

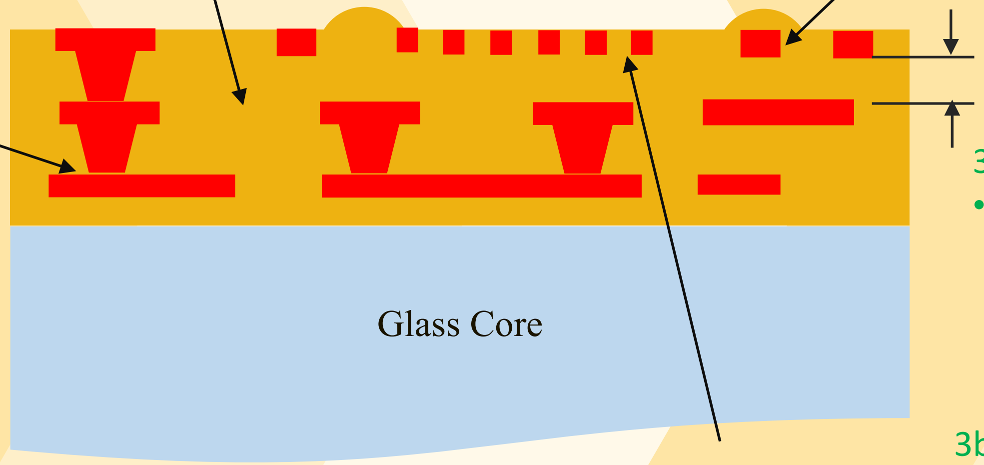
~500 | ~250 | ~50 | ~35 | ~7

Wiring density (IOs/mm/layer)

Technical Approach beyond prior art

1. Material Structure-Property correlation to move towards low-k materials

2a. (Planarity) Process optimization for
- **Ultra-smooth surface with**
- **thin dielectrics**
- **fine-features**



Low D_k (< 3.0), D_f (< 0.01) polymer dielectric

Planarizability

Cu/polymer Adhesion

2 – 5 µm Thickness

3c. (Characterization)
- Surface modification for adhesion enhancement

3a. (Electrical and Physical)
- Characterize electrical performance benefits with ultra-thin low-k dielectrics

3b. (Mechanical)
- Characterize critical compressive stress for RDL

2b. (Lithography)
- RDL Patterning for fine-pitch with low-k materials

Research Highlights

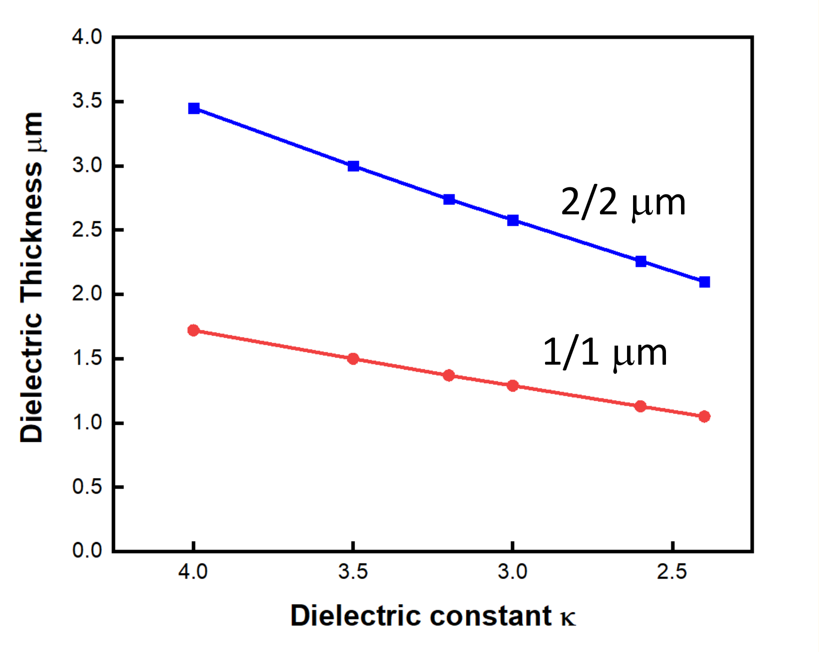
	Challenges	Research Tasks	Stoplight
Materials	Epoxy based dielectrics cannot support high data rates	1. Evaluating performance improvement with low D_k dielectric materials for HPC architectures	🟡
Process	DOP tolerance range is < 5 μm TTV of each layer for fine-pitch patterning	2a.Fabrication of test-structures to quantify DOP with upfront material candidates	**Focus** 🟡
	Thicker dielectrics with micron-sized fillers not suitable for scaling	2b.Develop RDL patterning and metallization processes for low D_k dielectrics	🟡
Characterization	Fine-pitch RDL are limited by high capacitive losses	3a. Characterize electrical performance metric with low-k, ultra-thin dielectrics	🟡
	Delamination because of increased interfacial stresses	3b.Characterization of maximum tolerance of residual stress in dielectric lamination and metallization	**Focus** 🟢
	Popcorning during solder reflow or delamination	3c.Investigating surface modification to improve adhesion of low D_k materials to seed layer	🟢

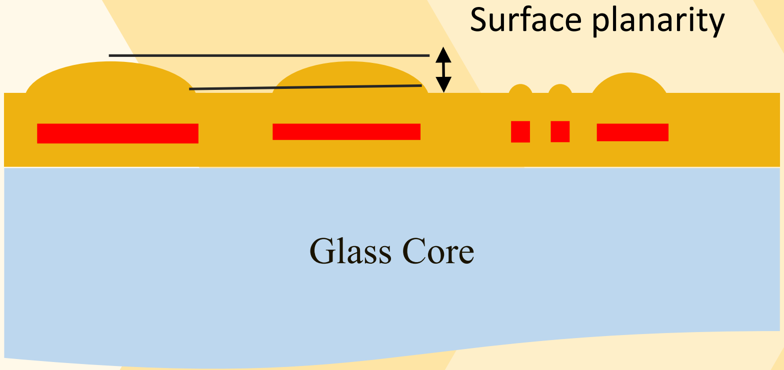
Material Selection

Characteristic	Ideal Properties	Polymer Family							
		Epoxy		BCB	Polyimide	Polybenz-oxozole (PBO)	Fluro-polymer	Hydro-carbon	Metal Oxide
		Non PID	PID						
Electrical	Low loss Low D_k	🟨	🟨	🟩	🟨	🟨	🟩	🟨	🟥
Physical	Ultra thin dry film (2-5 µm) Planar	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩
Thermal	Low-CTE Withstand 260 ^{0}C solder reflow	🟩	🟩	🟩	🟩	🟩	🟨	🟨	🟩
Mechanical	High Elongation Low modulus	🟩	🟩	🟨	🟨	🟨	🟨	🟨	🟨
Chemical	Resistance to chemicals Good adhesion	🟩	🟩	🟥	🟥	🟥	🟥	🟥	🟩
Cost	Low Material and Processing Cost	🟩	🟩	🟨	🟨	🟨	🟨	🟨	🟥
Reliability	Low Stress Low moisture absorption	🟨	🟨	🟨	🟨	🟨	🟨	🟨	🟨

Epoxies and BCB materials are an attractive choice for low-k dielectrics with the optimal properties

Task 1. Surface Planarity of dry-film and liquid ultra-thin dielectrics



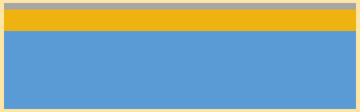


Task:

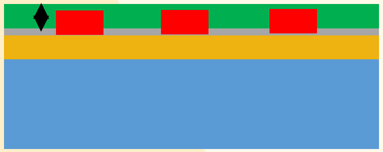
To quantify the surface planarity with upfront material candidates and evaluate tolerance required for fine-pitch multilayer RDL

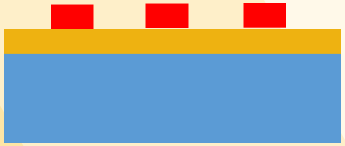
Process flow and characterization methodology

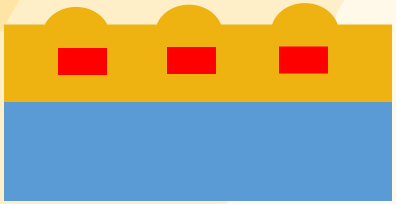

1. Dry-film/spin coating and curing

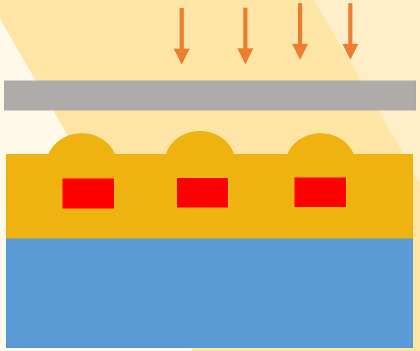

2. Seed layer metallization (Sputtered Ti/Cu)

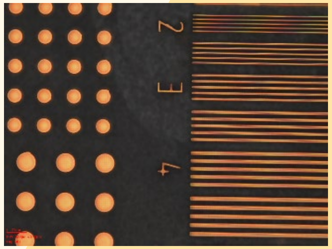

3. Photoresist Lamination and exposure

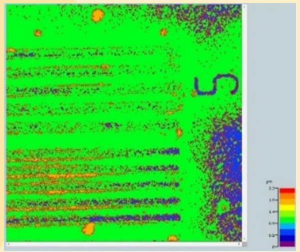

4. Electroplating


5. PR Stripping and seed-layer etching


6. Lamination/Spin Coating of second layer

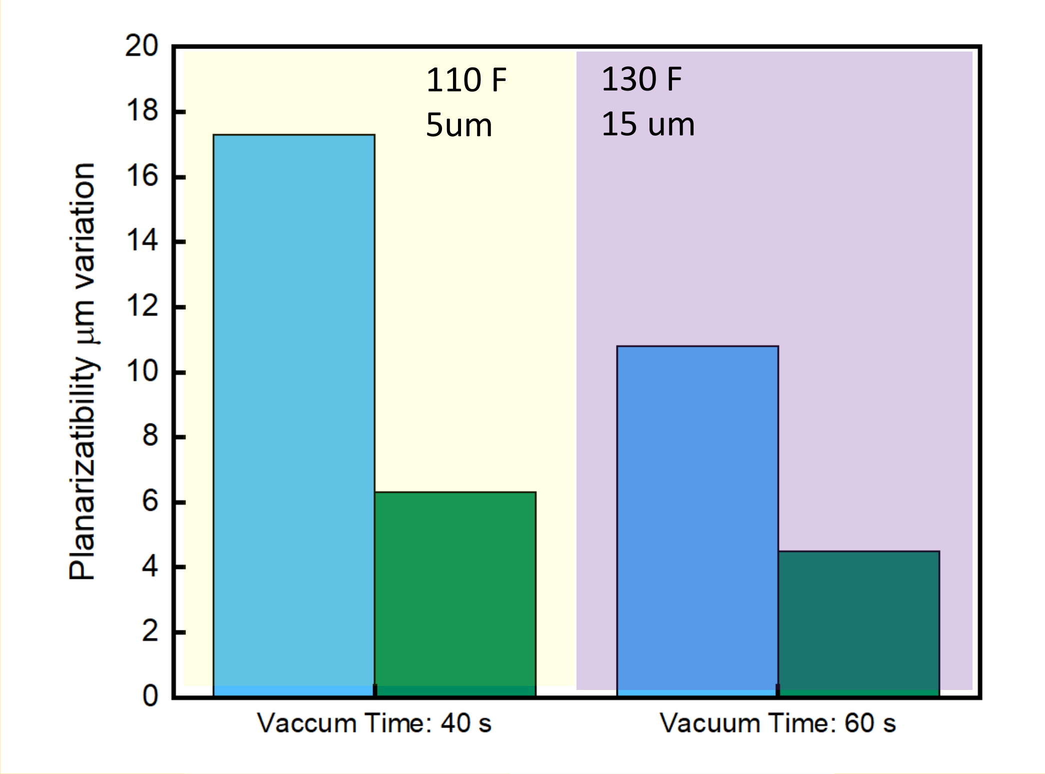

7. Hot press for vacuum lamination


Fine-pitch features


Laser Confocal microscopy.

- Highest – lowest in the line/space region

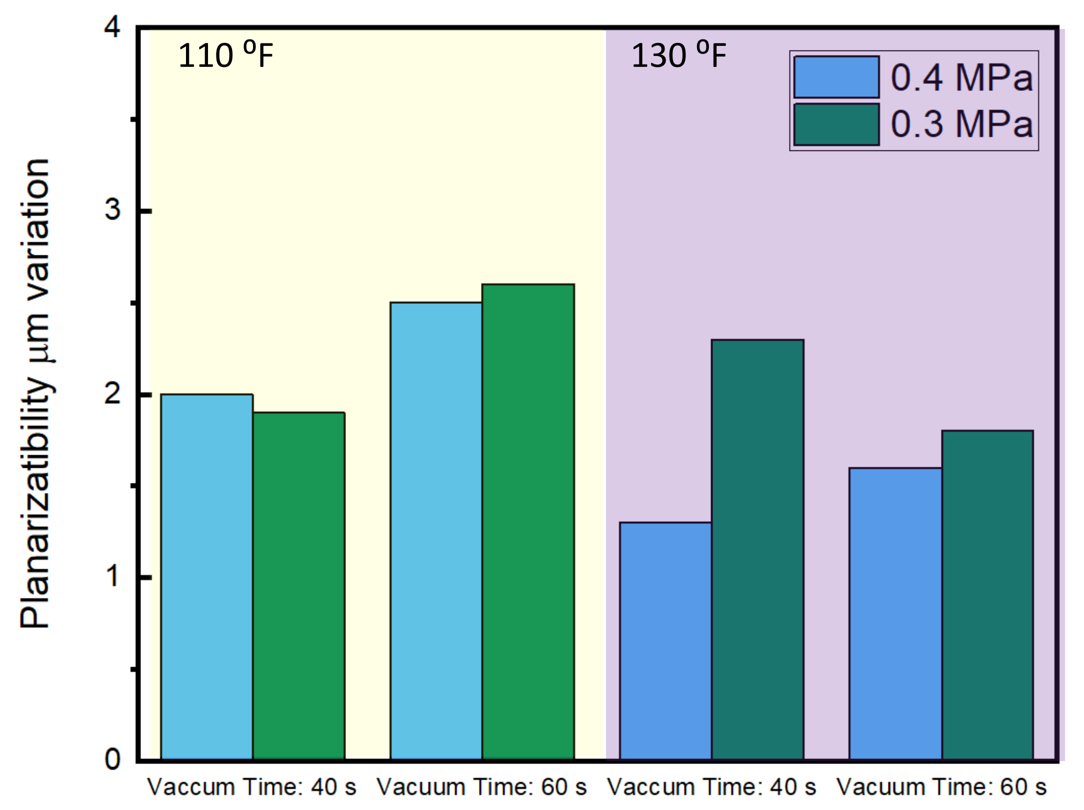
Coarse-pitch Features



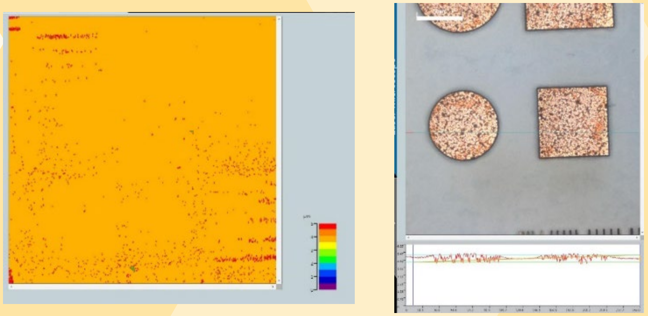
Observations:

- Increase in pressure helps in improving the polymer fill between traces
- Increasing polymer thickness improves co-planarity

Fine-pitch features – dry-film



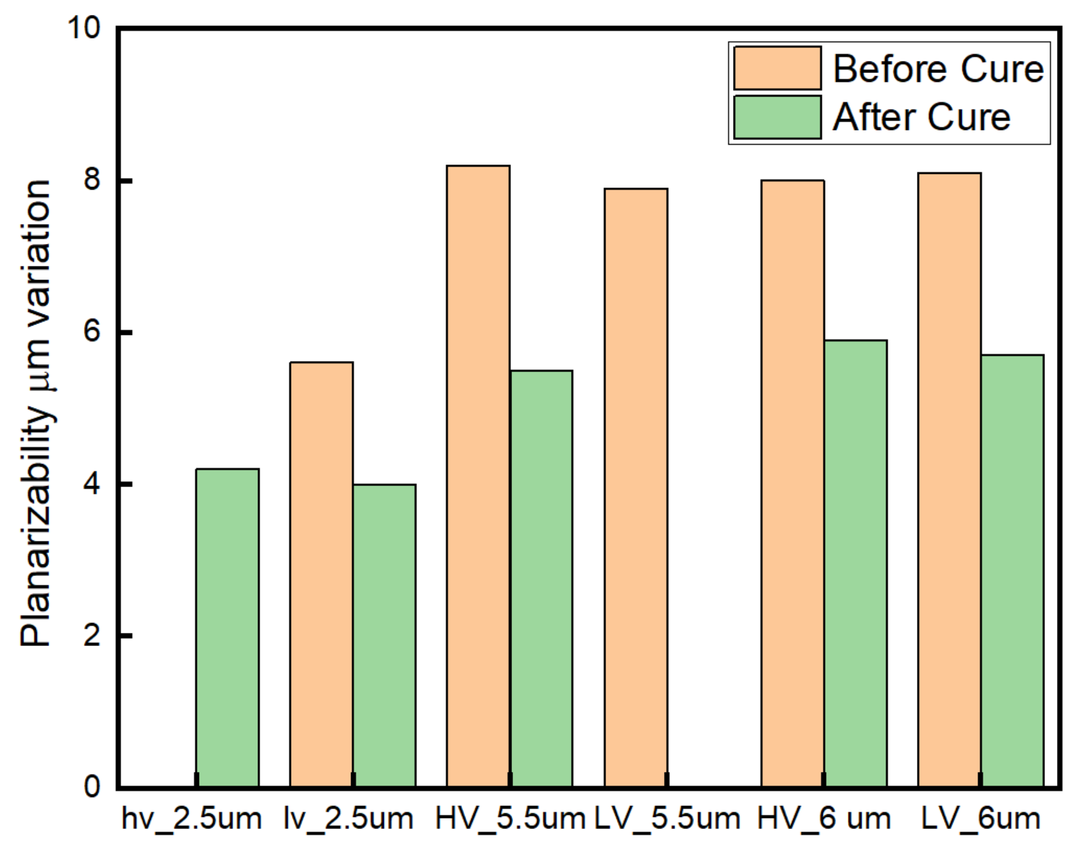
Time: 60 s
Temperature 130 °F
Pressure: 0.5 MPa
~0.74 – 1 μm variation



Observations:

- <3 μm polymer dip variation across feature sizes of 2-5 μm
- Increase in pressure and temperature shows a slight improvement

Liquid dry-film patterned with fine-pitch features



Observations:

- Viscosity does not seem to have a huge influence
- Planarity becomes better after cure as polymer becomes of melt flow
- Taller copper structures see more non-coplanarity initially but it evens out after cure

Summary and Next steps

- Summary:
  - <5% TTV cannot be achieved with process optimization for dry-film and liquid dielectrics
- Next Steps:
  - Explore fly-cut planarization for higher copper thicknesses and dry-film/liquid dielectric polymers