Design and Demonstration of 2.5D Glass Interposer BGA package with 2 µm ML RDL

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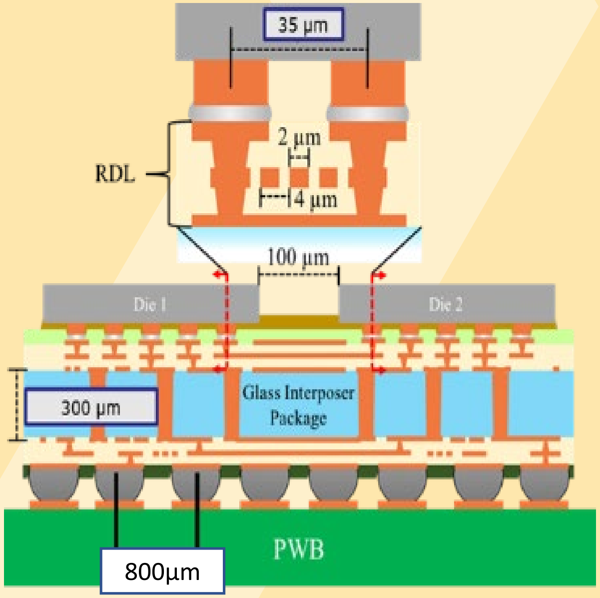
Goals and Objectives

- **Design and demonstrate a power efficient, higher bandwidth, lower-cost and higher reliability large body size 2.5D glass interposer as Next Generation to Si interposer**

Enabling Basic Technology Targets (2018-2020)

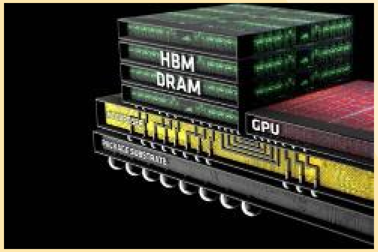
Parameter	Objective	Prior Art (Silicon Interposer)
Materials	Low-k dielectrics: k ~ 3	SiO_2: k ~ 3.8-4.0
Process	Double Sided SAP	Wafer Scale BEOL
Interconnect IO density	225 IOs/mm/layer (Low R and C)	250-400 IOs/mm/layer (High R and C)
Bump pitch (Chip level)	35 um (TCB)	45 um (TCB)
Body Size (Board Level)	40 mm x 50 mm (Mass Reflow)	28 mm x 36 mm (Mass Reflow)
Thermal	Advanced Direct Cu plated heat sink	Std. Heat Sink
Relative Cost	Low (Panel-Scale Processes) Large Body Size Feasible	High (Wafer-scale processes) Small Body Size feasible
Board Level Reliability	Direct Board Attach	Need Organic Package substrate

- ➢ ***RDL interconnects*** approaching BEOL RDL with ***lower R and C***
- ➢ Fine pitch ***chip-level interconnect***
- ➢ ***Direct attachment*** to board
- ➢ ***Low-cost large body size substrate***



Prior Work

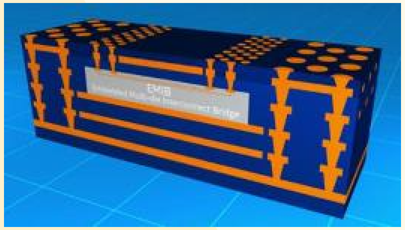
Si interposer
AMD



- High R and C RDL interconnects
- Board Level Reliability (combined with thick organic substrate)
- High Cost for Large Body Size

C. Lee et al., “An Overview of the Development of a GPU with integrated HBM on Silicon Interposer”, ECTC, 2016, 1439.

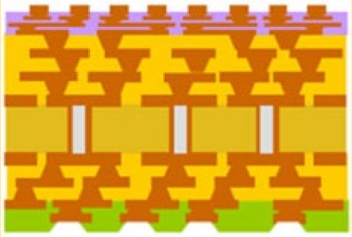
EMIB
Intel



- High R and C RDL and Long interconnects
- Board Level Reliability (combined with thick organic substrate)
- Large Body Size Feasible

R. Mahajan et al., “Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect”, ECTC, 2016, 557.

Organic Interposer
Shinko



- Low R and C RDL interconnects
- Z-height (thick organic core)
- Large Body Size Feasible
- # of fine pitch Metal Layers (RDL yield/cost) > 4

K. Oi et al., “Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-fine Wiring and High Density Bumps”, ECTC, 2016, 557.

Technical Approach

Materials

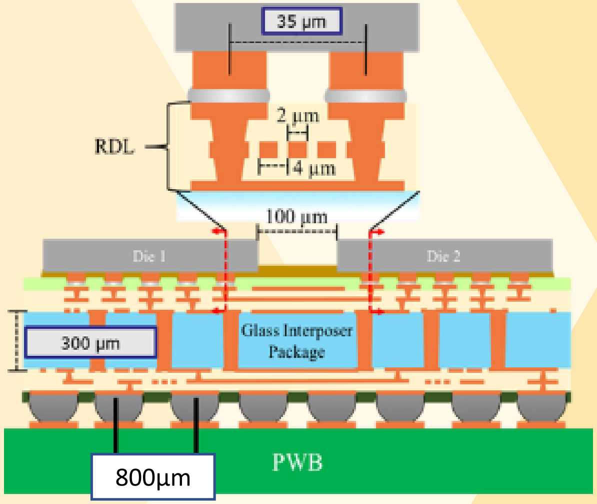
- ➢ **Ultra-Thin, Low D_k Dielectrics**
  - Panel Processable
  - Low CTE, Low Modulus, High Elongation to Break

Processes

- ➢ **Panel-Scale Semi-Additive Process**
  - Surface Planarization for High Yield RDL formation
  - End Point Seed Etch Detection

Low Cost

- ➢ **Low Cost, Panel Scale Processes**
- ➢ **Large Body Size Substrates**



Interconnects

- ➢ **Low R, Low C 2 um Multi-Layer RDL with 50 ohms impedance matching**

Reliability

- ➢ **RDL Reliability**
  - Fine pitch traces and u-vias
  - Multi-Layer RDL Reliability on Glass
- ➢ **Interconnect**
  - Chip Level interconnects at 35 um pitch
  - Board Level with 7 ppm/K CTE Glass core

Thermal

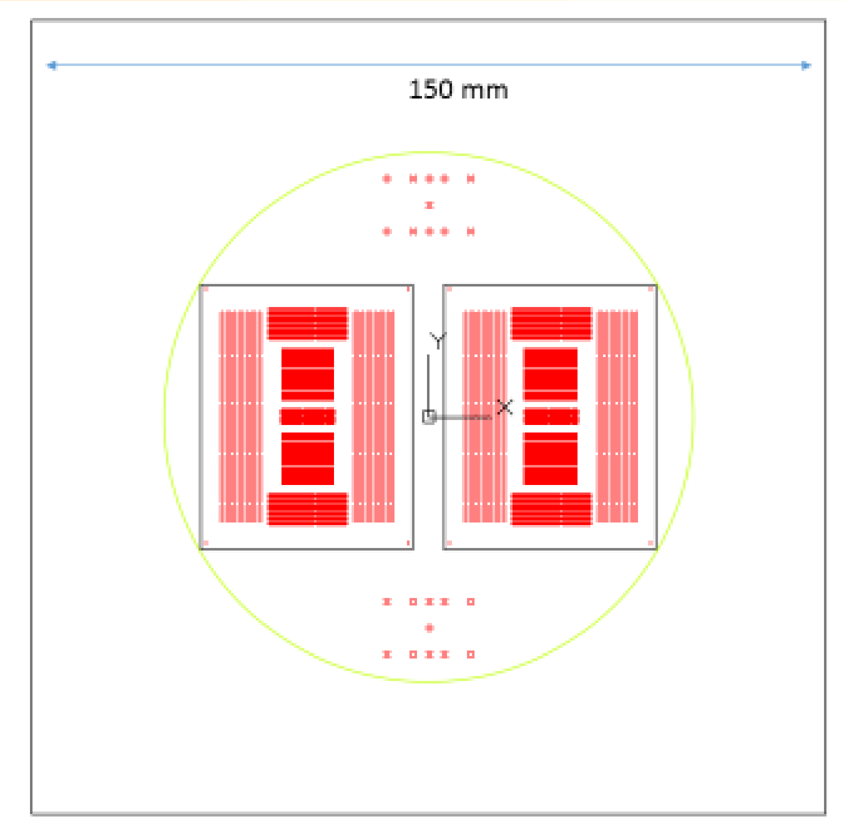
- ➢ **Advanced Direct Cu plated heat sinks**

Assembly

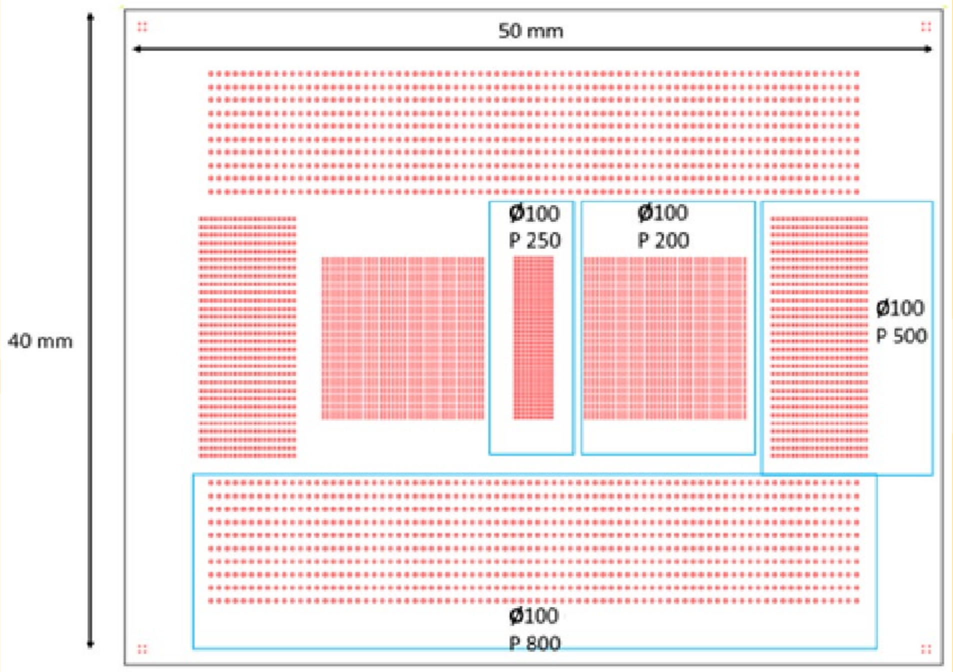
- ➢ **Chip-level interconnect**
  - TCB Cu pillar
- ➢ **Board-level interconnect**
  - Large body 30 mm x 40 mm SMT

Results: TGV Design

Lead: Siddharth



TGV map for 6”x6” glass panel



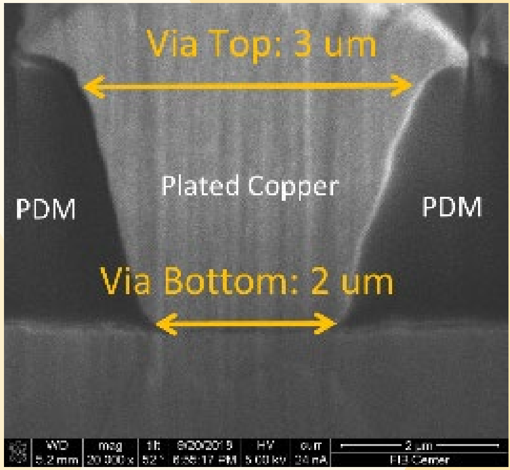
TGV map for single interposer

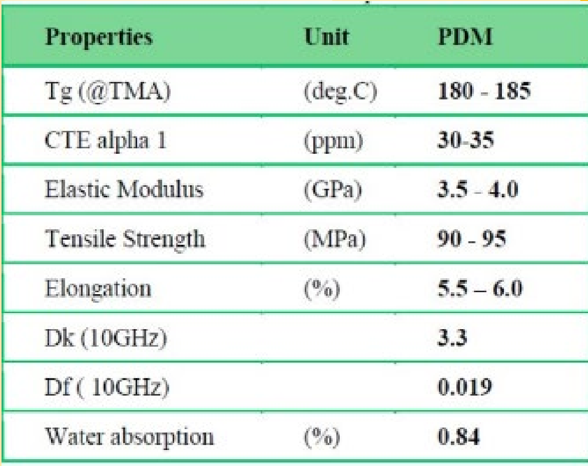
- 100 µm TGVs with pitch varying from 200-500 µm
- Optimized through via filing for vias down to 50 µm diameter and 300 µm substrate (6:1 aspect ratio)
- Study of metallization of TGVs to be done

Photo-Imageable Dielectric for fine line RDL

Lead: Kenny K (Taiyo), Pratik

- **Novel photo-dielectric for high resolution**
- Good balance between low CTE and high resolution
- **With low % elongation to break and smaller tensile strength, the goal is to maintain via taper angles between 64^0-90^0**
- Low roughness thus optimization of sputtering needed for better adhesion and reliability

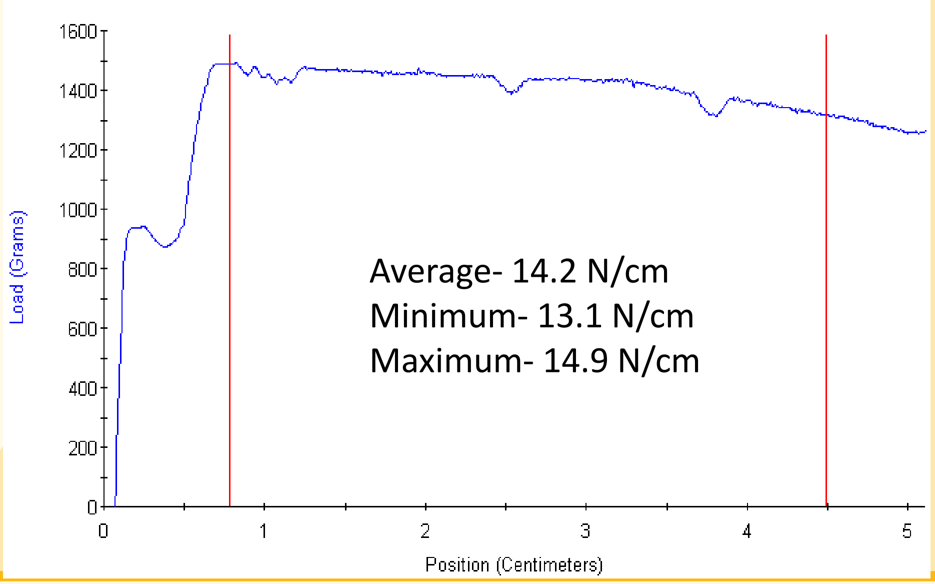




Properties	Unit	PDM
Tg (@TMA)	(deg.C)	180 - 185
CTE alpha 1	(ppm)	30-35
Elastic Modulus	(GPa)	3.5 - 4.0
Tensile Strength	(MPa)	90 - 95
Elongation	(%)	5.5 – 6.0
Dk (10GHz)		3.3
Df (10GHz)		0.019
Water absorption	(%)	0.84

Conditions-

1) Plasma Treatment:
    - Ar plasma- 8.5 mins
    - O2 plasma- 2 mins
2) Pre-bake: 125°C for 30mins in vacuum
3) Sputtering chamber pressure: 10E-6 Torr

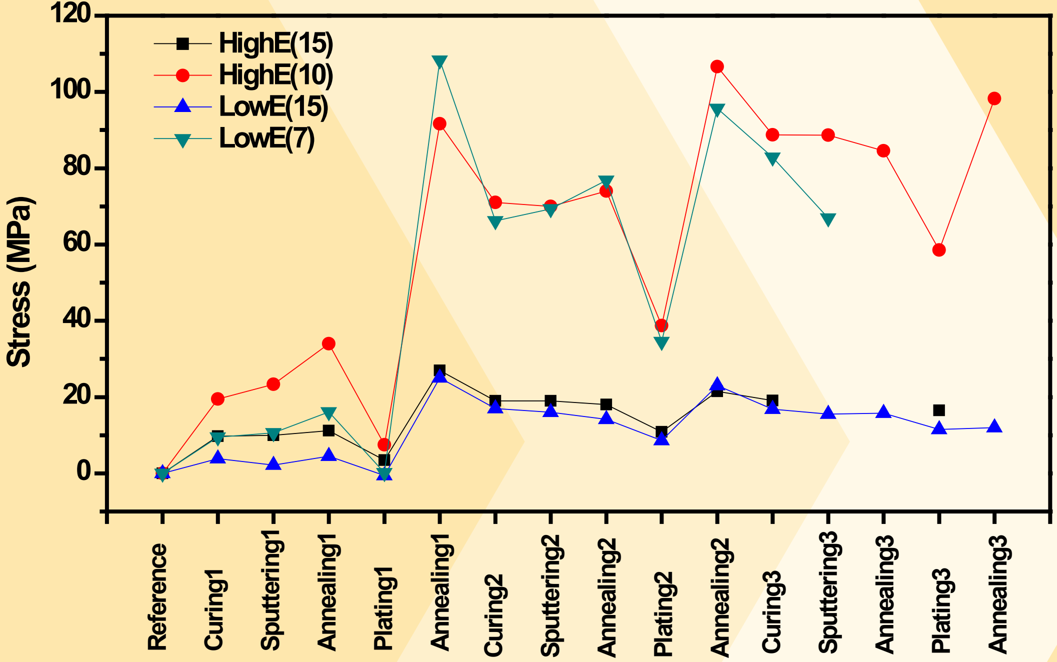


Average- 14.2 N/cm
Minimum- 13.1 N/cm
Maximum- 14.9 N/cm

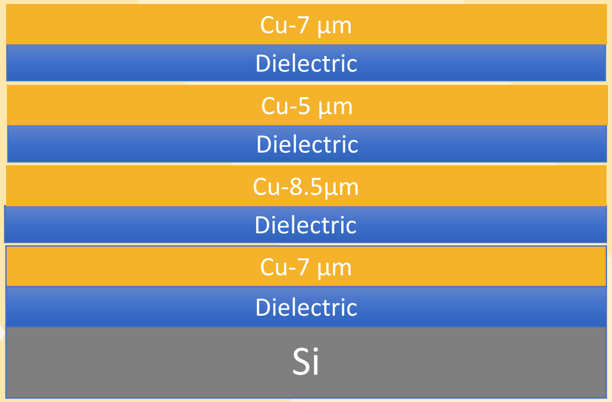
ML-RDL residual stress analysis

Lead: Pratik

Residual stress at various stages of fabrication



Schematic stack up of dummy ML RDL

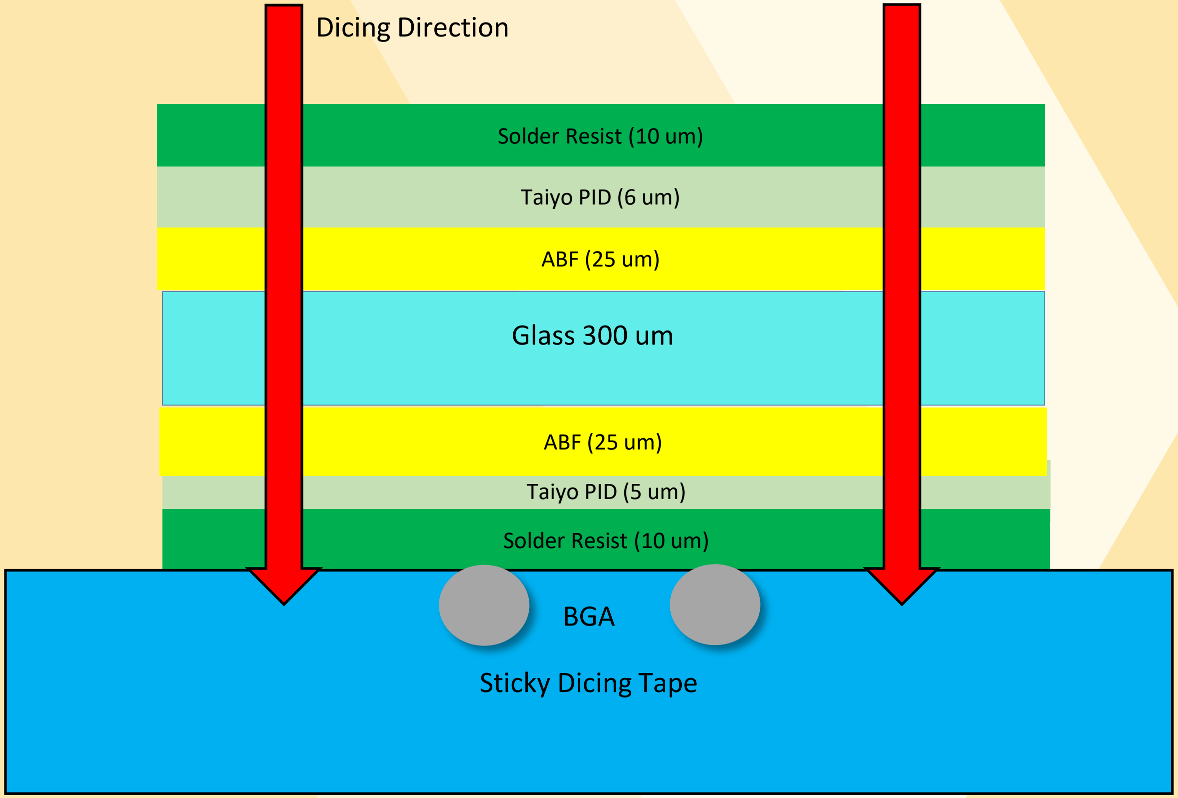


- A thicker dielectric provides more stress relaxation as compared to thin dielectric
- For a dielectric having lower tensile modulus, stress is lower upto formation of the first metal layer
- As the number of metal layers goes on increasing, the stress starts levelling out

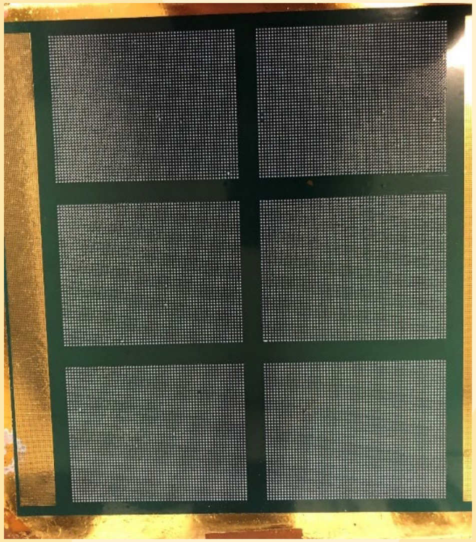
Results: Dicing Test Vehicle

Lead:
Pratik (Fabrication)
Omkar (BGA Balling)
Disco (Dicing)

Objective: Understand challenges and optimize the dicing conditions for glass BGA package with no over mold



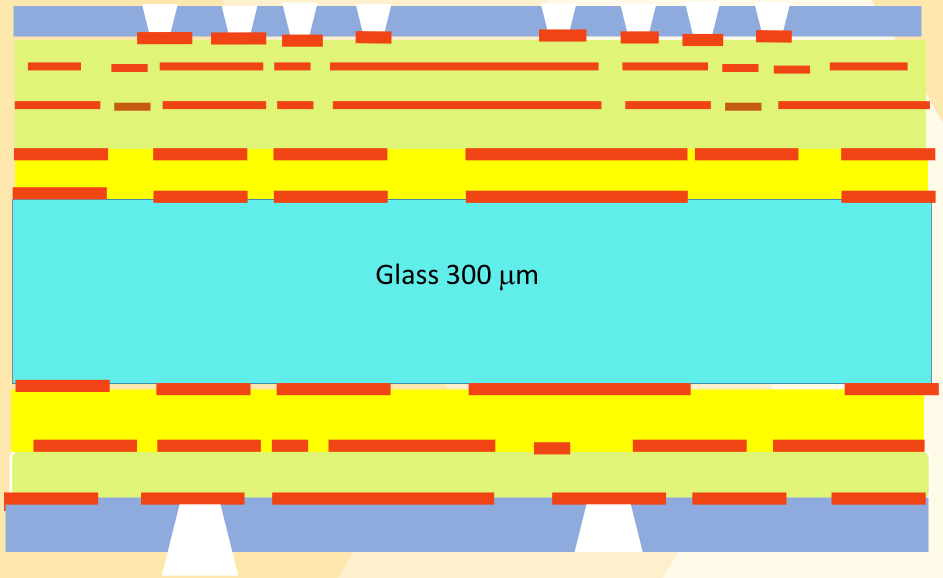
Good alignment with minimal ball bridging



- ✓ Test Three Different Glass CTEs (3.4, 7.8 and 9 ppm/K) replicating Mechanical TV
  - 300 µm thick glass with dielectric stacks
  - Only top and bottom metal layers
  - Fabrication completed

Results: Mechanical Test Vehicle - Board-Level Reliability

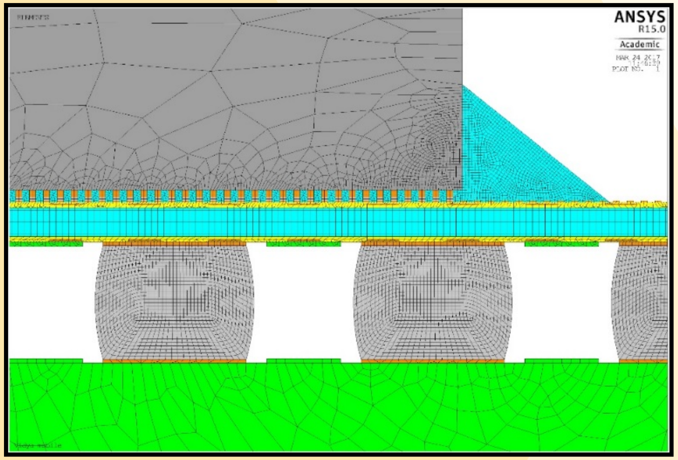
Lead:
Pratik (Fabrication)
Vanessa (Assembly)



✓ Test three different glass CTEs (3.4, 7.8 and 9 ppm/K) for board-level reliability
- 300 µm
- No TGVs
- Electrical routing structures to test board-level interconnections post thermal cycling reliability

Results: Prior Work

Reliability modeling for 2.5D glass interposer with 4 ML symmetric RDL stack-up



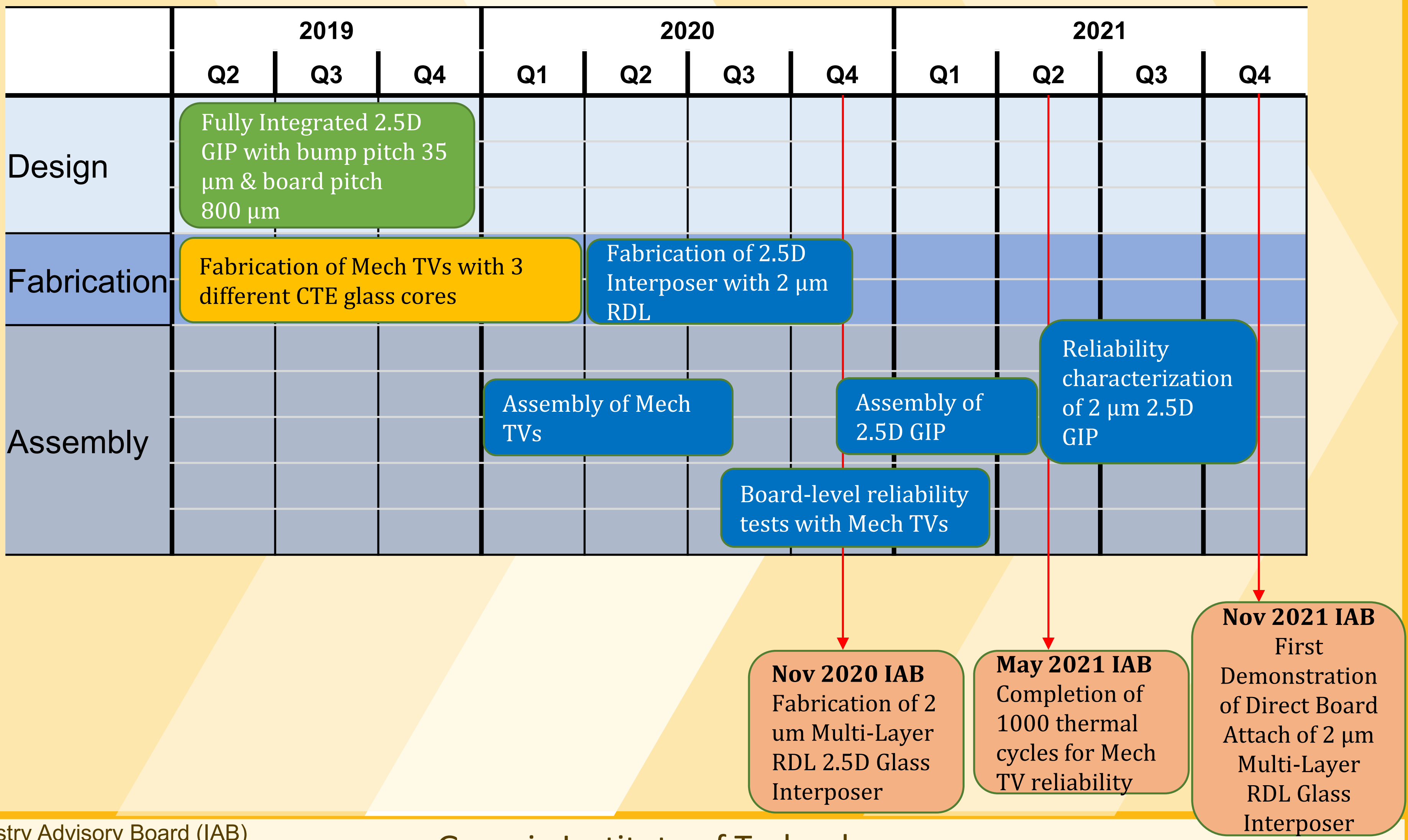
Glass CTE (ppm/K)	Package size (mm)	BGA diameter (um)	BGA pitch	Package thickness (um)	Nf (Coffin Manson)	Nf (Engelmaier Wild)
3.4	40 x 30	350	650	300	106	104
9	40 x 30	350	650	300	918	1389
9	40 x 30	350	650	100	1162	1844
9.8	40 x 30	350	650	300	1099	1724
9	50 x 40	350	650	300	928	1408
9	60 x 50	350	650	300	1097	1721
9	50 x 40	500	800	300	1395	2295
7.8	50 x 40	500	800	300	1283	2076
3.4	50 x 40	500	800	300	520	703

Summary

- TGV design is complete
- Optimized sputtering conditions for improved adhesion and reliability of RDL
- Dicing test vehicle fabrication has been completed and panel sent to Disco for dicing test on 10/30/2019
- Mechanical test vehicle fabrication is ongoing
- Thermomechanical modeling: packages with 8 ML asymmetric stack-up and high CTE glass core (7.8 and 9 ppm/K) expected to pass 1000 thermal cycles

Schedule

🟩 **Completed** 🟨 **Ongoing** ▨ **Future task**



2019: Q2, Q3, Q4 | 2020: Q1, Q2, Q3, Q4 | 2021: Q1, Q2, Q3, Q4

Design

Fully Integrated 2.5D GIP with bump pitch 35 µm & board pitch 800 µm

Fabrication

Fabrication of Mech TVs with 3 different CTE glass cores

Fabrication of 2.5D Interposer with 2 µm RDL

Assembly

Assembly of Mech TVs

Assembly of 2.5D GIP

Reliability characterization of 2 µm 2.5D GIP

Board-level reliability tests with Mech TVs

Nov 2020 IAB
Fabrication of 2 um Multi-Layer RDL 2.5D Glass Interposer

May 2021 IAB
Completion of 1000 thermal cycles for Mech TV reliability

Nov 2021 IAB
First Demonstration of Direct Board Attach of 2 µm Multi-Layer RDL Glass Interposer