Georgia Tech

Georgia Tech PACKAGING RESEARCH CENTER

2.5D and 3D Glass Panel Embedding For High Performance Computing

Student: Siddharth Ravichandran
Faculty: Prof. Rao Tummala, Prof. Madhavan Swaminathan

Liaisons: Nobuo Ogura (Nagase)
TSMC, AGC, AMAT, Schott, Corning, Disco, Honeywell, Brewer Science, Panasonic, Nitto

Outline

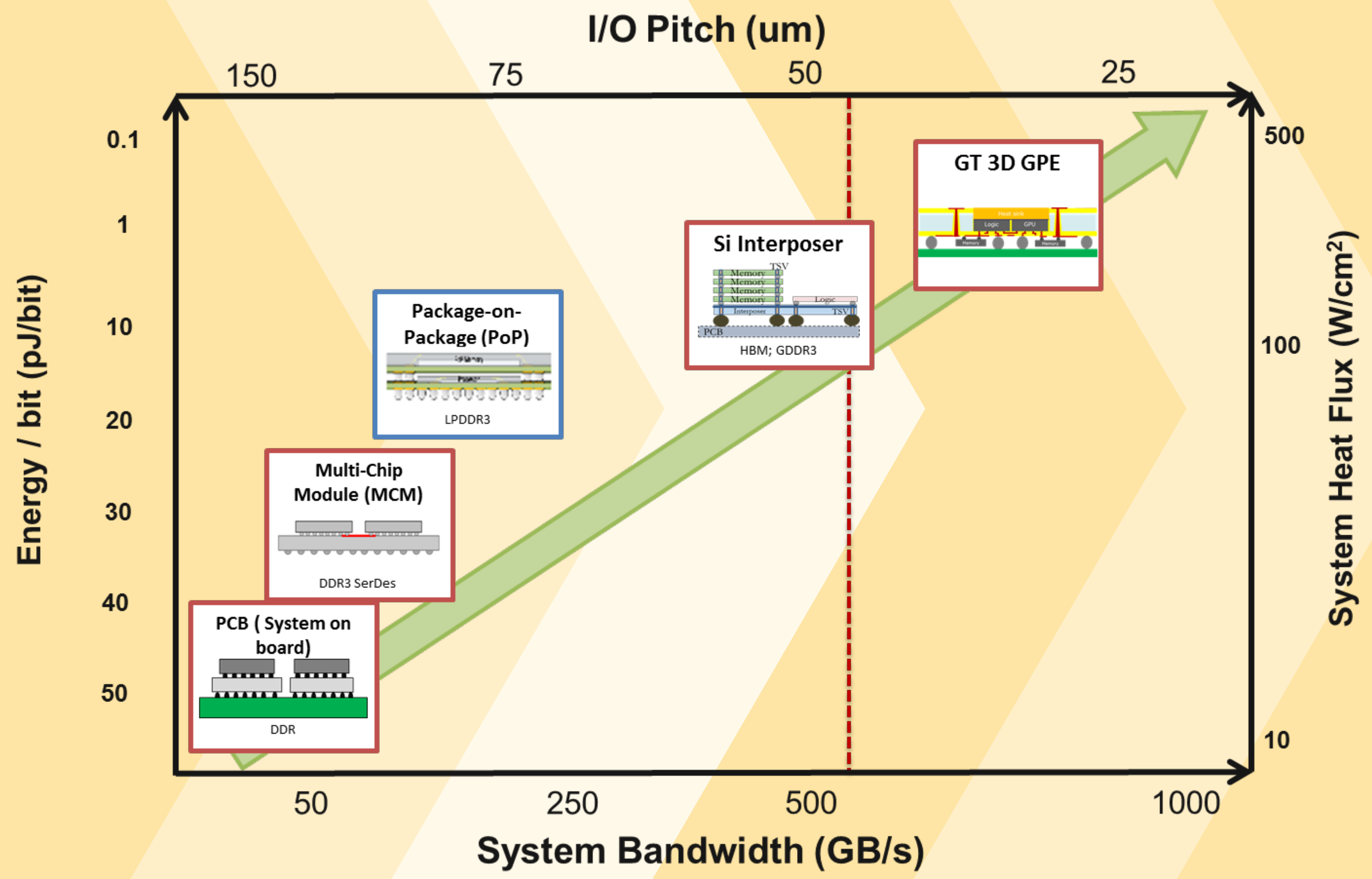
- ❑ Goals & Objectives
- ❑ Strategic Need
- ❑ Research Highlights
- ❑ Results
- ❑ Summary

Goals and Objectives

- Design and demonstration of next generation 3D Glass Panel Embedding with performance beyond 2.5D architectures, superior I/O density and form-factor, enhanced thermal management considering thermomechanical reliability, and low-cost fabrication.

	Parameter	Target	Prior Art	Challenges	Research Tasks
Design	Bandwidth	1 TB/s	250-500 GB/s	• High-Parasitic Package Architecture • Contradicting channel Power and Latency requirements	1. Modeling and Design of 2.5D and 3D GPE 2. Fabrication of 2.5D & 3D GPE a) Embedding with and without carrier b) RDL c) Assembly 3. Thermal Management 4. Reliability
	Power Efficiency	1pJ/bit	10-15 pJ/bit		
Substrate	I/O Pitch	<20 um	~50 um	• Huge die-shifts from EMC shrinkage in inorganic WFO • Poor Through-Mold-via pitch • Increased channel length from MCM approach	
	Interconnect Length	<50 um	Mean Channel Length: ~500 um		
Thermal	T_c	Near-zero	0.03-0.1°Ccm^{2}W^{-1}	• Direct chip copper integration • Stress buffering between chip and copper with near-zero thermal resistance • Large-area plating • Package-level reliability	
	Bulk thermal conductivity	400-460 W/mK	5-399W/mK		
	T_j	< 85°C			
Assembly	Chip-Level (HBM)	~35 um	~55 um	• Panel Warpage • Contradicting chip- and board-level CTE requirements	
	Board-level	<650 um	800-1000 um		

Strategic Need

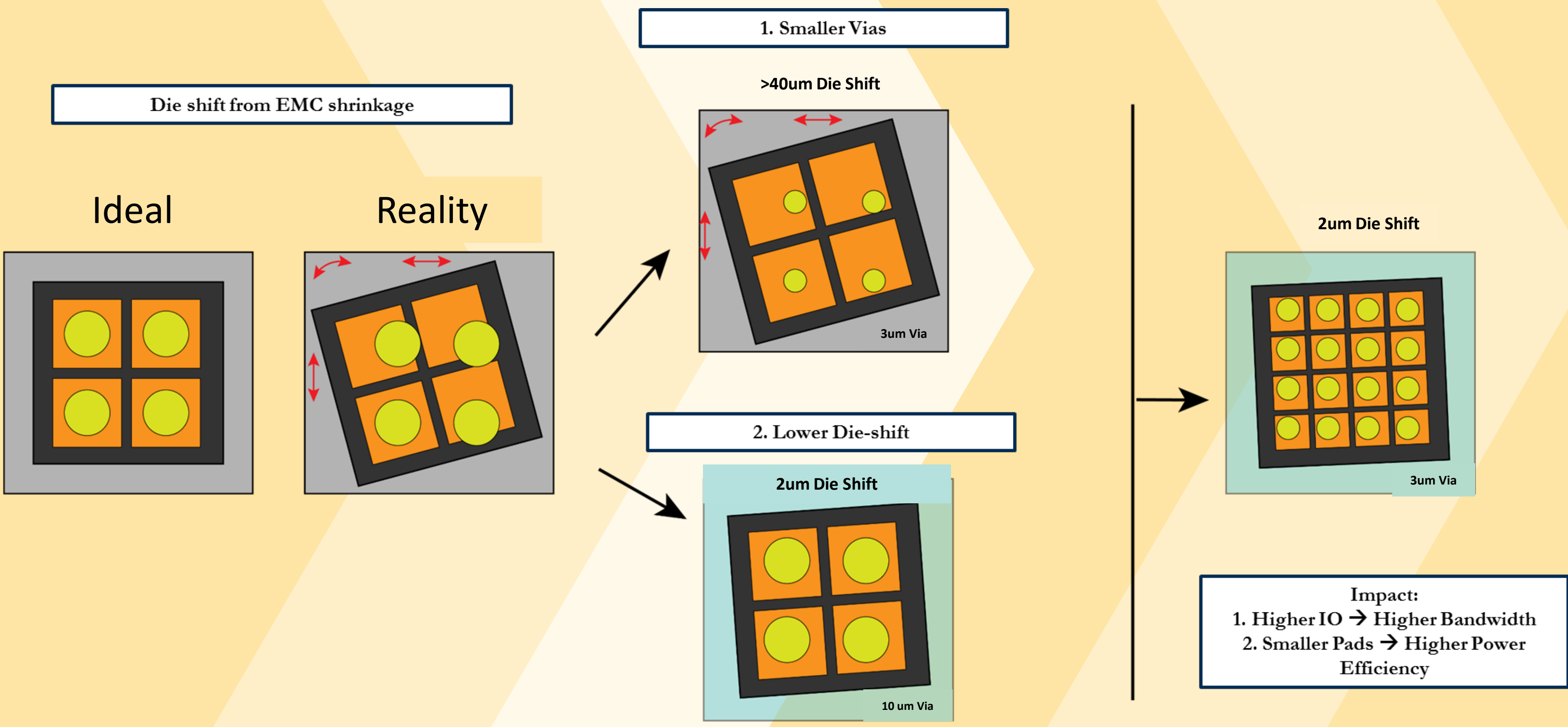


Research Highlights

	Research Task	Research Highlight
1. Design	a) Parasitic extraction to compare 2.5D, 3D chip-first and chip-last architectures	*Bandwidth* (Normalized Bandwidth: Si Interposer, 2.5D GPE, 3D GPE, 3D IC); *Power Efficiency* (Normalized Power Efficiency: Si Interposer, 2.5D GPE, 3D GPE, 3D IC)
2. Demo	a) Die-shift reduction	*<2um Die-shift using DAF*; *~5 um Surface planarity before fly cutting*; *2.5D GPE*
	b) Multi-die embedding	
	c) Reduce warpage to enable fine-pitch assembly on GPE	*2x warpage reduction from low stress bonding*; *Backside alignment patterns*; *3D GPE*
	d) Panel-scale lithography	

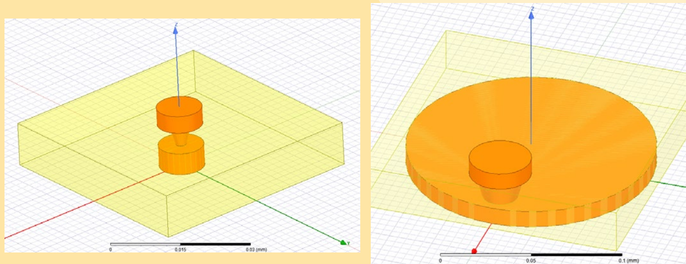
Recent Progress – Pitch Scaling in GPE

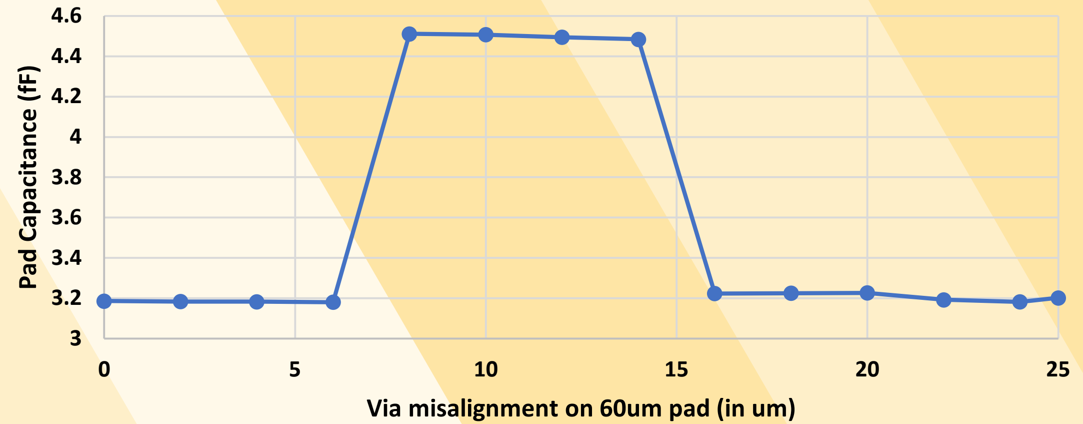
Challenges and Benefits of Pitch Scaling in GPE towards < 20 μm IO Pitch with 2 μm L/S Integration

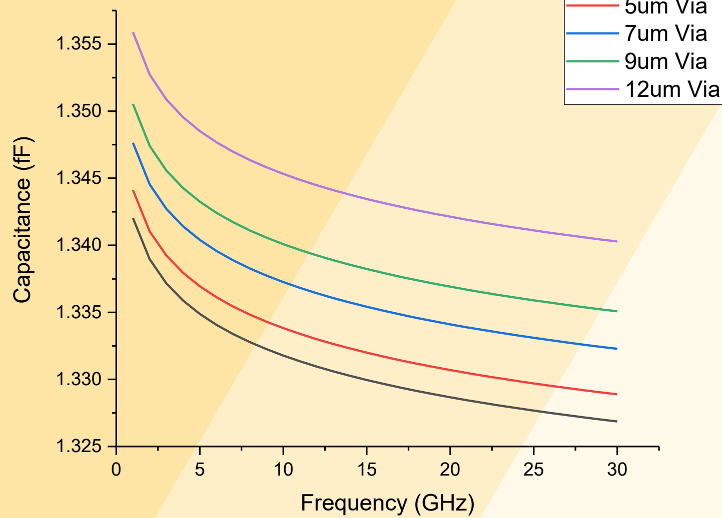


Impact of Via Size and Die-Shift on Capacitance

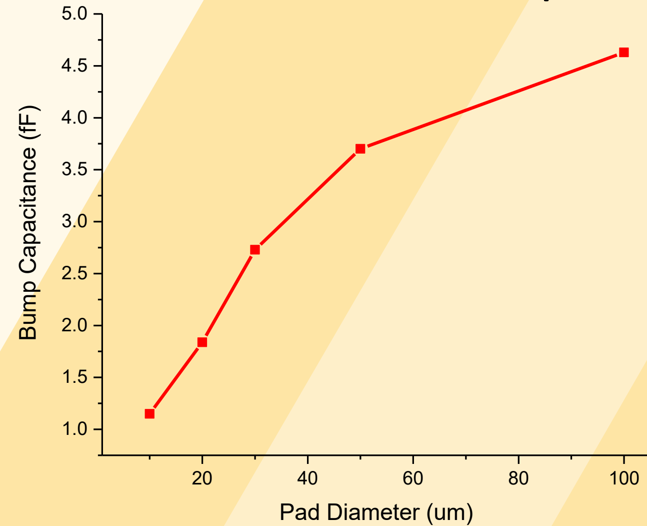
Parasitic Capacitance Extraction in HFSS





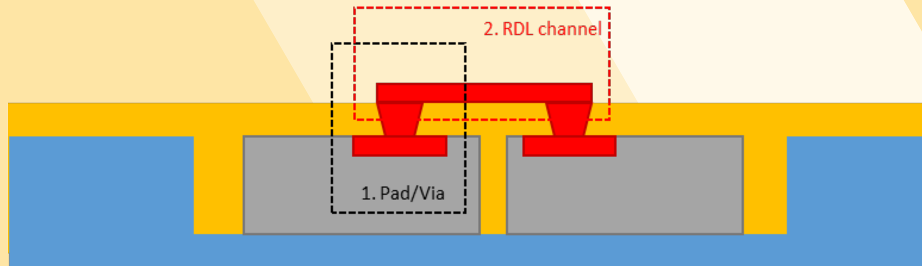


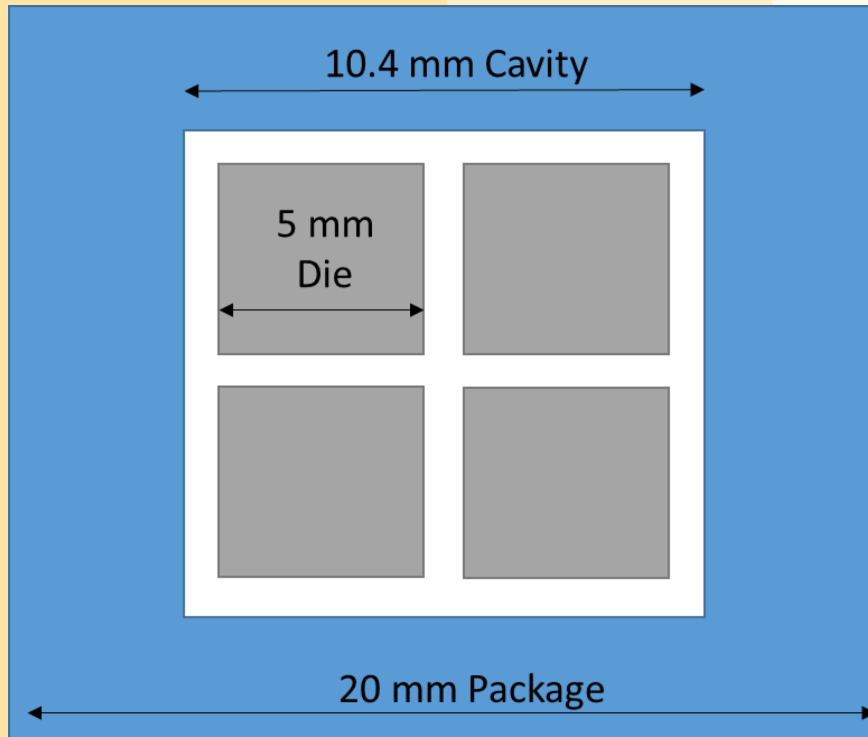
Improvement in Power-Efficiency is marginal



Up to 5X improvement in power-efficiency in scaling pad diameter from 100 to 10 um

High-density GPE TV Details



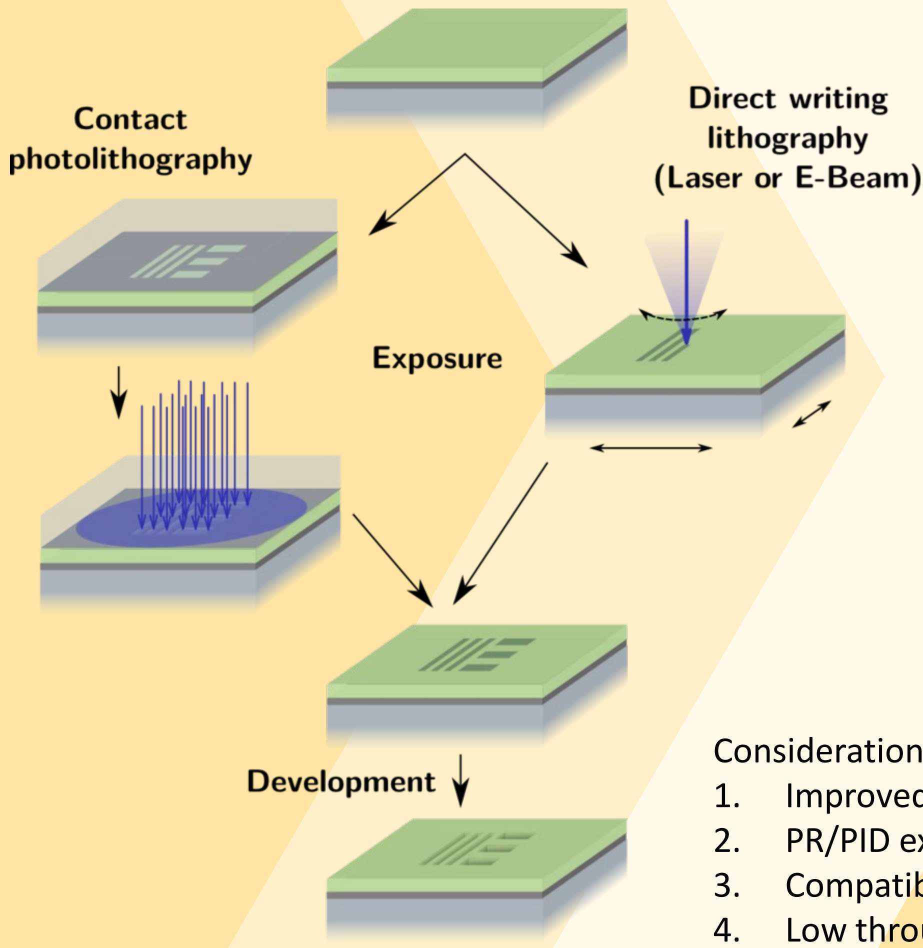


Die Size	5 x 5 x 0.3 mm
Cavity size	10.4 x 10.4 mm
Cavity Depth	310 µm
Substrate thickness	360 µm
Panel	100 x 100 mm

I/O Pitch	20, 15, 10, 7.5
Die to Die space	100, 50, 20
L/S	5, 4, 3, 2, 1
Chip-pkg via	7.5, 5, 3
Dielectric	5 µm

High-density GPE TV Fabrication

Contact vs Maskless Laser-writing Lithography



Heidelberg laser writer in IEN
Wavelength = 375 and 405 nm
CD = 1 μm

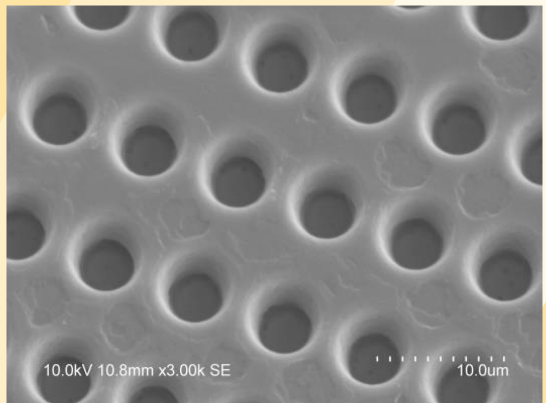
Considerations:

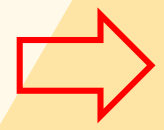
1. Improved local alignment to compensate for <u>manual</u> die-placement
2. PR/PID exposure conditions for 375 nm
3. Compatibility of substrate, alignment scheme with MLA
4. Low throughput process than contact/projection lithography

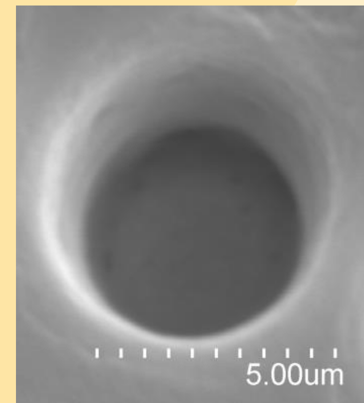
TV Fabrication- 1. Chip-to-PKG Microvia

Microvia formation on Maskless Aligner

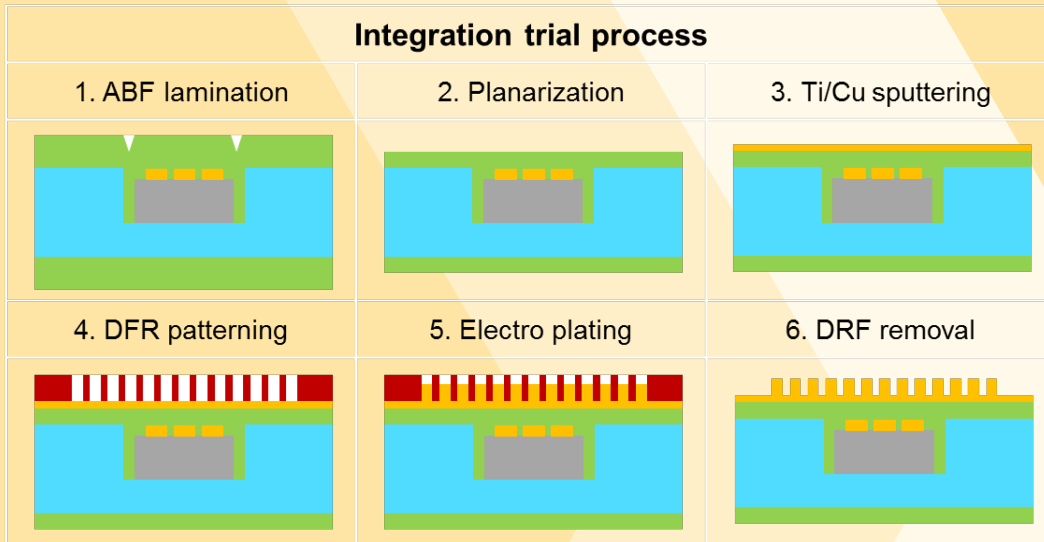
5 μm Via Diameter
In 5 μm Taiyo PID



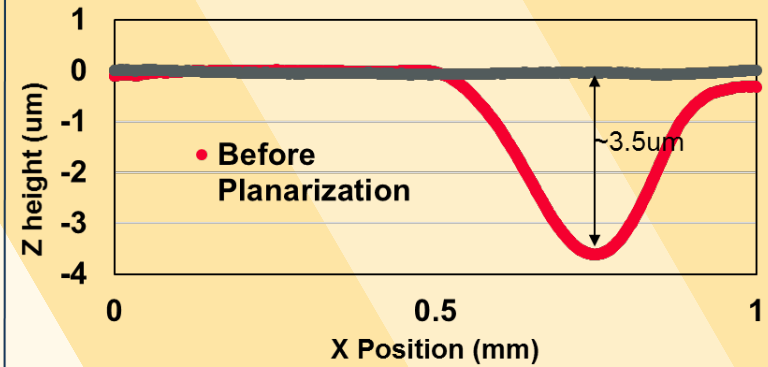


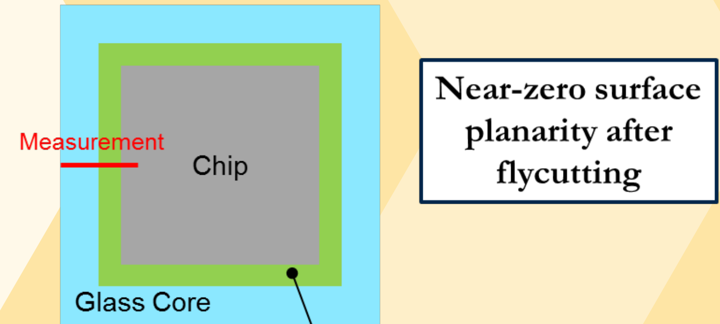


TV Fabrication- 2. RDL Channel

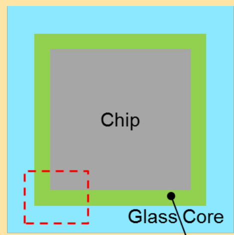


DFR : TOK 8 um
Exposure tool : Ushio UX-44101

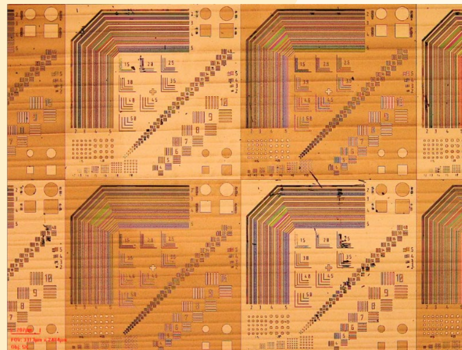


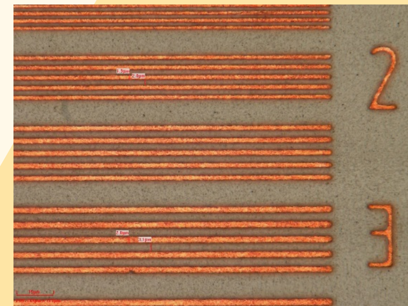


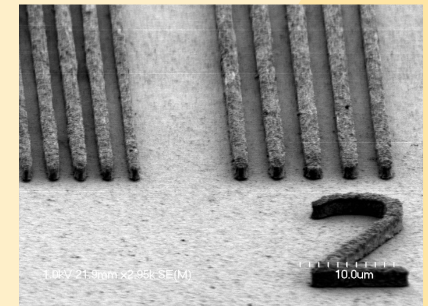
Near-zero surface planarity after flycutting



Glass Core : 250umt
ABF GXT61 : 30um on both side
Ti/Cu : 50/200nm







Summary

- Impact of via dimensions and pad scaling (die shift) on power efficiency (PE) is studied and it can be concluded that:
  - Misalignment from die-shift results in up to 25% variation in capacitance
  - Scaling pad diameter has more significant impact on PE than scaling via dimensions.
- Demo of pitch-scaling and multi-die integration on GPE:
  - Embedding Process: < 2 μm die-shift has been demonstrated before
  - Process for 3-5 μm Microvia integration for < 20 μm pitch chip-to-PKG interconnects on Maskless Aligner has been established
  - 2-5 μm lithography with 1-3 AR has been established on GPE substrates.
  - It is concluded that a planarization step will be required for < 10 μm L/S RDL in GPE

Timeline