

Direct Cu-Cu bonding in C2S applications using Cu-pillar with nanoporous-Cu caps

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Thank you to SRC for funding and guidance



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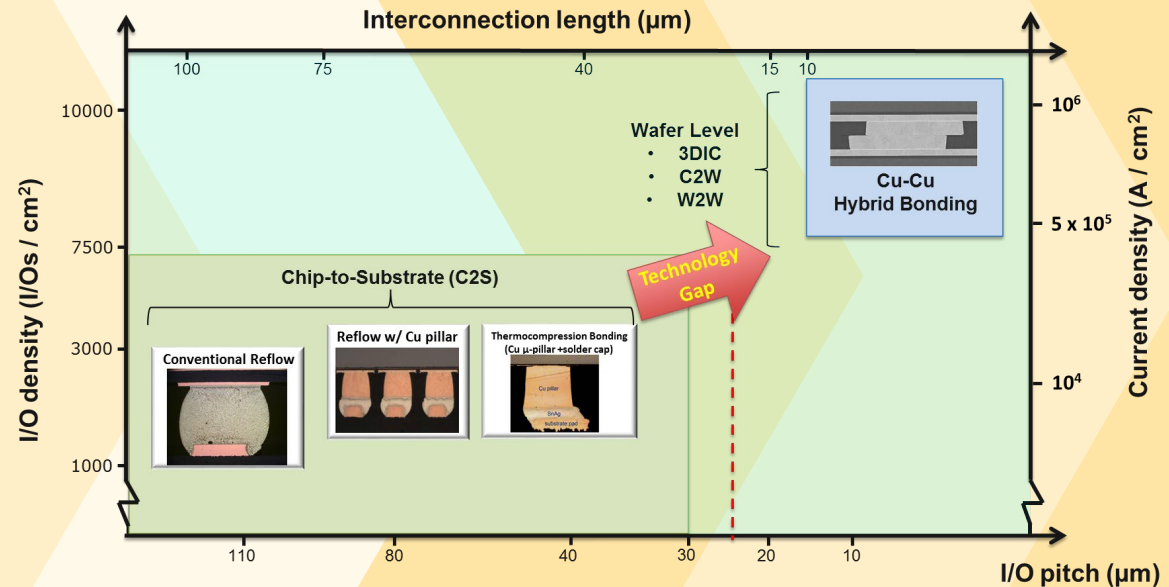
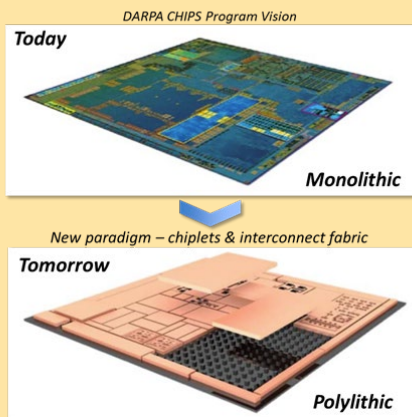
IBM

Samsung

- Goals & Objectives
- Prior Work
- Technical Approach
- Results & Key Accomplishments
- Comparison with Prior Art
- Summary
- Schedule

Design and demonstration of novel all-Cu interconnections with solder-like compliance before assembly and Cu-like performance and reliability after assembly, for C2S application

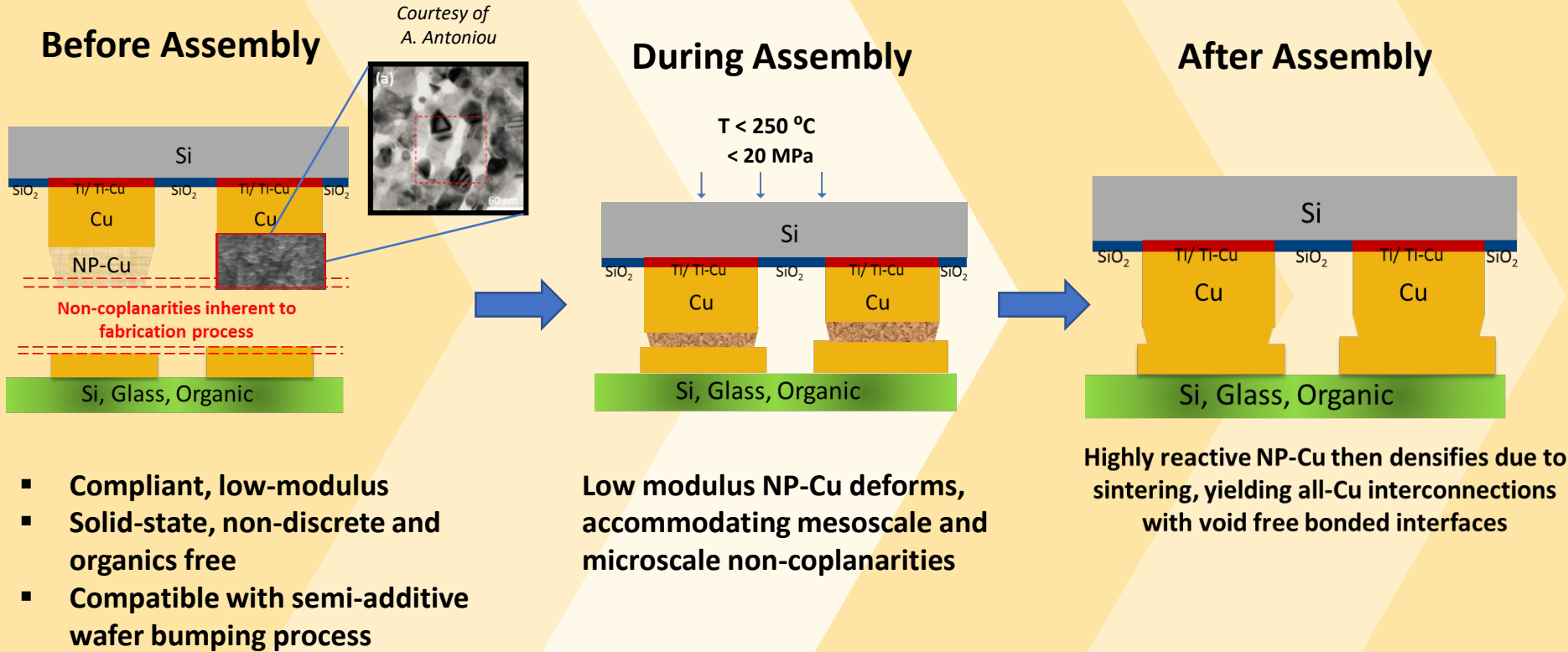
Example in HPC / AI:
The "Chiplet Revolution"
→ C2S pitches <20μm by 2030



- ❑ Solders are reaching their fundamental limits in **pitch scalability**, **power handling** capability and **fatigue resistance** – across applications (digital, analog, power, ...)
- ❑ **Direct Cu-Cu bonding** is predicted as the next interconnection node, but current technologies are not applicable at package level – the key bottleneck to developing a **universal** assembly solution: **non-coplanarities**

- ❑ Developed new process flow for seed layer etching that allows for the fabrication of daisy chain structures
- ❑ Stabilized electroplating bath chemistry to improve the composition uniformity of plated Cu-Zn structures
- ❑ Preliminary characterization of parts assembled using nanoporous-Cu caps as bonding interface

Introducing nanoporous-Cu (NP-Cu) as a replacement to solder caps to form all-Cu C2S interconnections:



4. Technical Approach

Comparison to solder technology

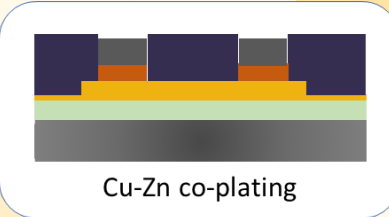
Wafer bumping

Solder caps fabrication

NP-Cu caps fabrication

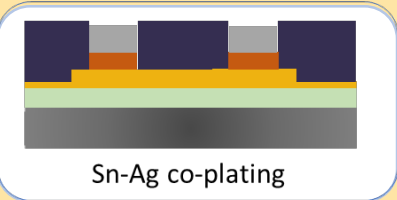


- Uniform composition
- Uniform plated thickness

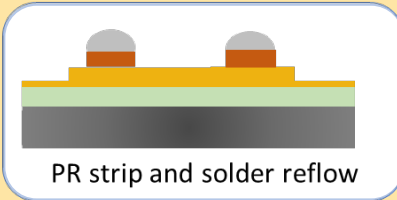


Cu-Zn co-plating

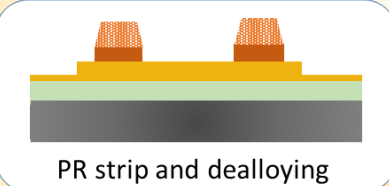
Maintaining compatibility with existing industry infrastructure is key to scaling to manufacturability



Sn-Ag co-plating



PR strip and solder reflow



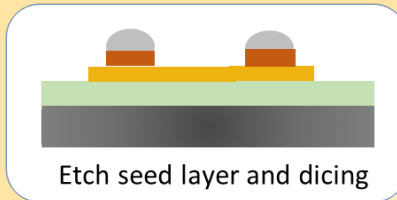
PR strip and dealloying

Proposed fabrication process is compatible with existing industry semi-additive processes, promising high precision and throughput

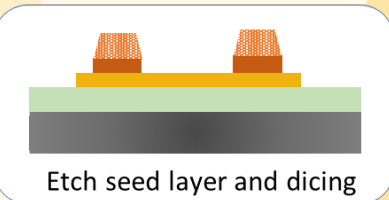
- Solder-like compliance

Assembly at <250°C

- Bulk-like properties after sintering (densification)



Etch seed layer and dicing

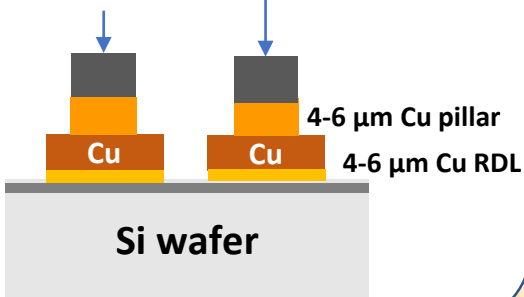


Etch seed layer and dicing

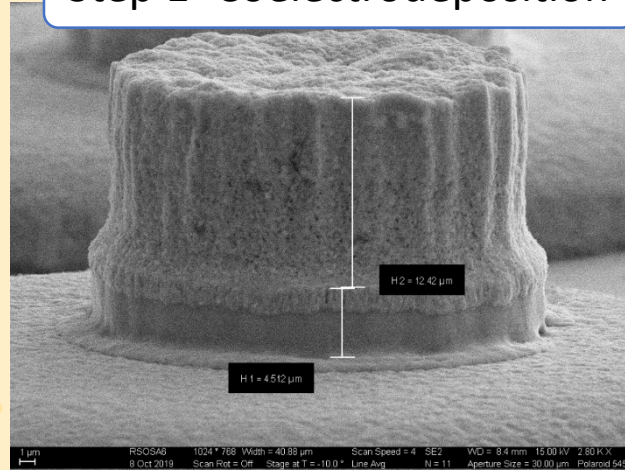
5.1 Understanding how to optimize the fabrication of a NP-Cu cap

Cu-Zn capped bump

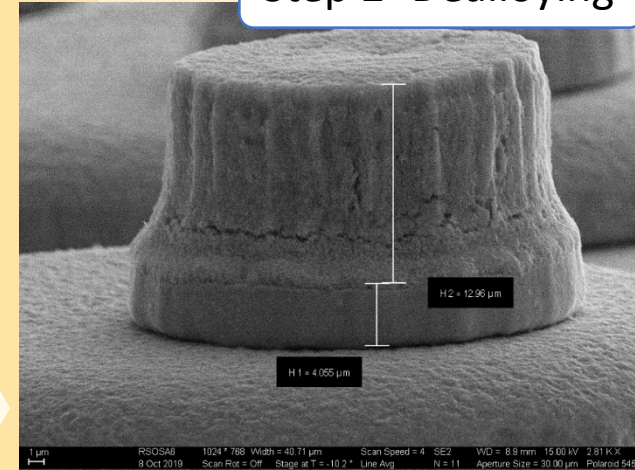
12-15 μm Cu-Zn



Step 1- Coelectrodeposition



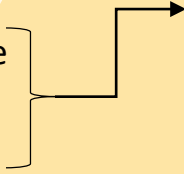
Step 2- Dealloying



- Properties of nanoporous metals are heavily dependent on fabrication
- Focus has been on determining how different process parameters influence the properties of the NP-Cu cap

Composition of the plating bath and plating potential primarily influence Cu-Zn composition, also:

- Plating rate
- WIP, WID, WIW uniformity
- Phases present in structure
- Grain structure
- Residual stresses



Dealloying controlled primarily by acid concentration and dealloying time but also on plated properties

- Modulus
- Residual Zn%
- Ligament morphology
- Cap shape
- Cracking

5.2 Effect of annealing on the properties of plated Cu-Zn

Cu-Zn on Bumps
Plated at -1.50 V for 45 min
~25:75 Cu:Zn initially

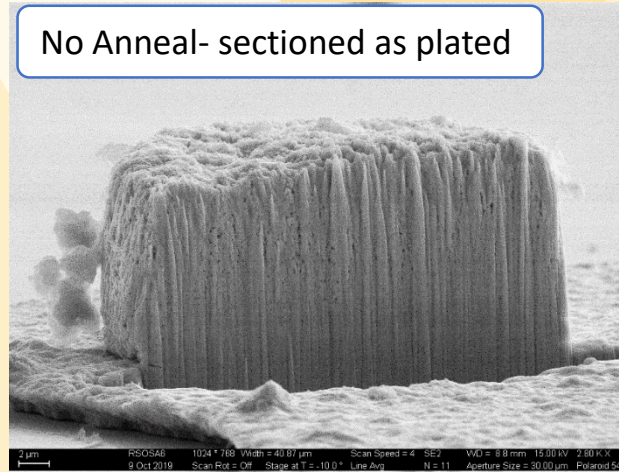
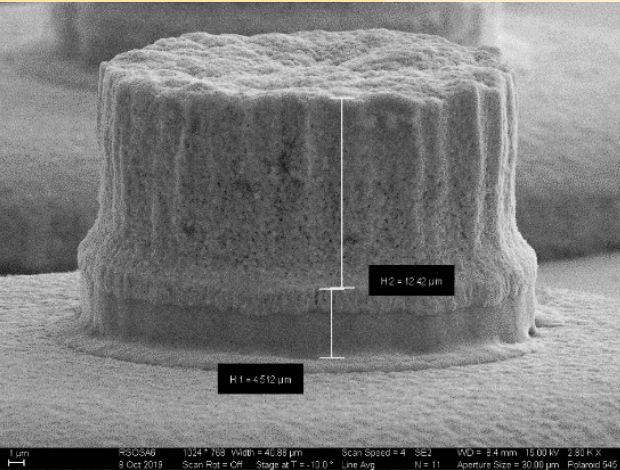
No Anneal- sectioned as plated

Key Insights:

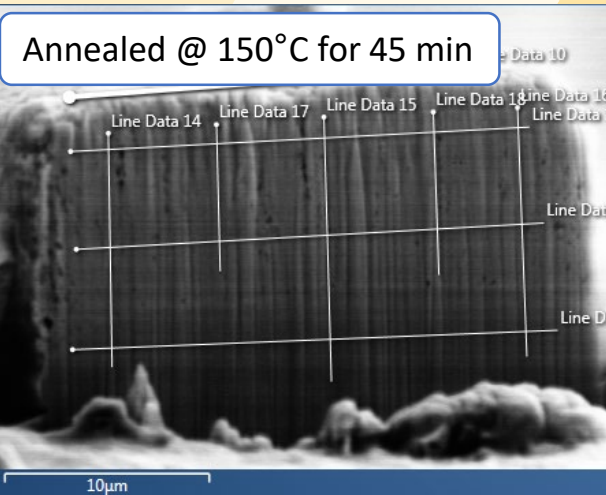
- Increase in Cu within Cu-Zn pillar-likely diffusion from underlying metallization
- More variation in composition throughout the Cu-Zn pillar- possibly from development of different phases

Need to be mindful of how comp. variance affects dealloying!

FIB X-Section Courtesy of Timothy Ibru



Average 23.36% Cu, $\sigma = .82\%$



Average 26.02 % Cu, $\sigma = 3.12\%$

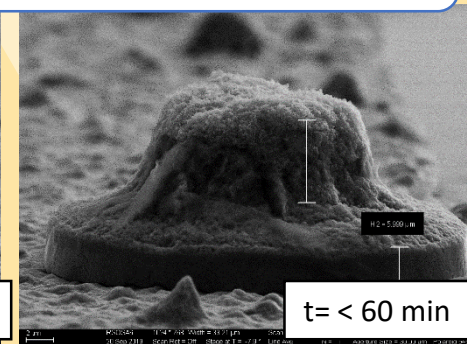
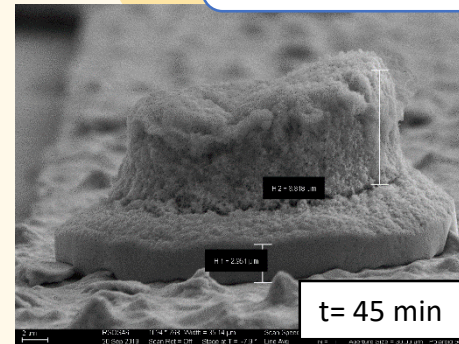
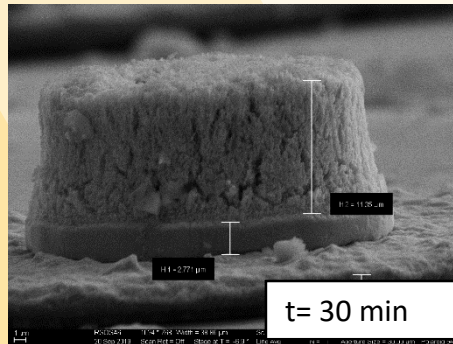
- Annealing shown to reduce tensile residual stresses induced during plating
- FIB milling and EDX line scans used to explore changes within the bump as a result of annealing

5.3 Effect of annealing on the dealloying process

Cu-Zn on Bumps
Plated at -1.50 V for 45 min
~25:75 Cu:Zn Initially
Dealloyed in 0.3 wt% HCl

No Anneal- dealloyed as plated

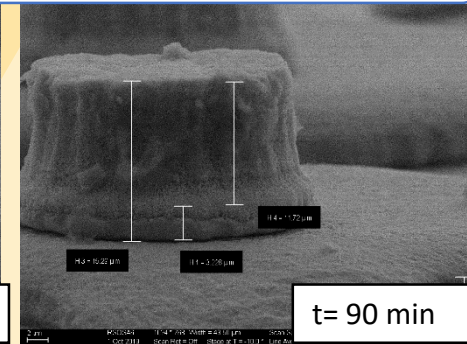
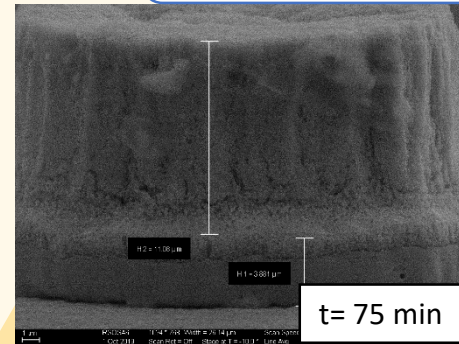
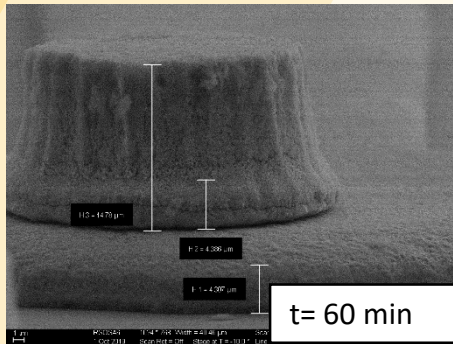
Residual Zn decreases rapidly, but at the expense of bump integrity



Annealed @ 180°C for 2 hrs

Dealloying rate slows considerably, but bump more stable

Same starting composition and structure...

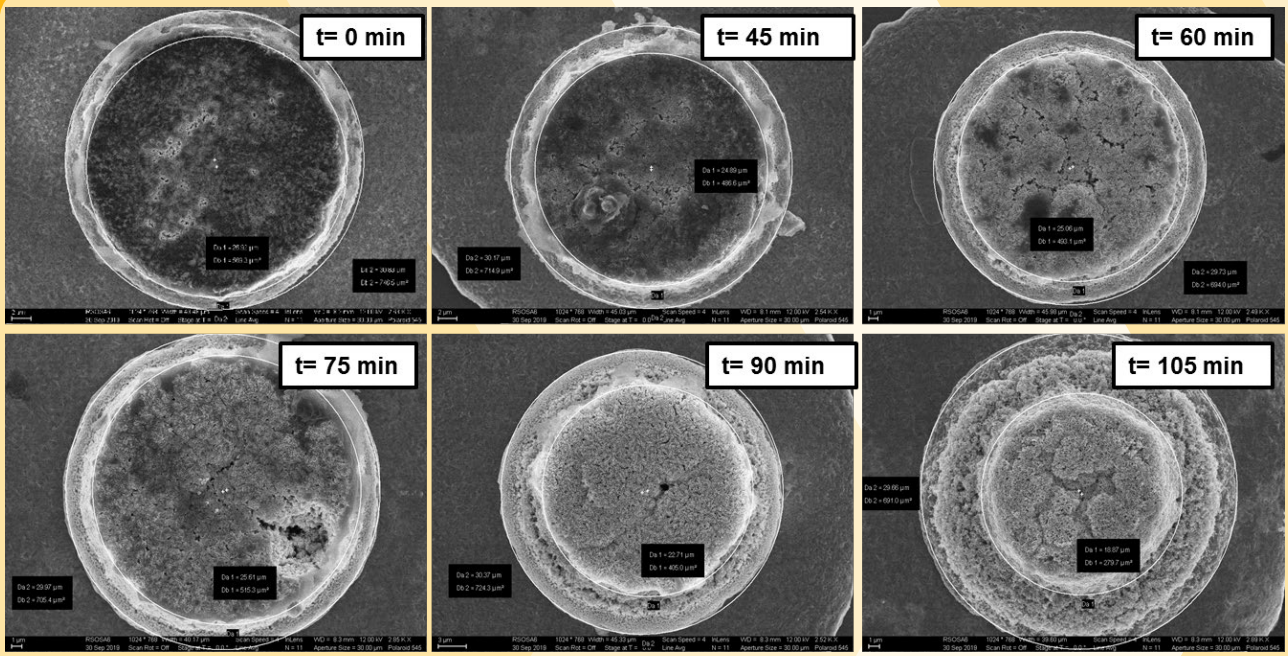


...different behavior influenced by processing

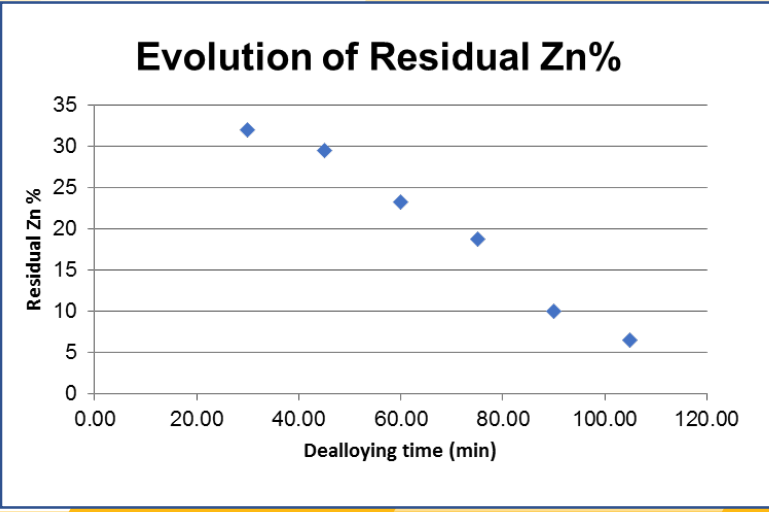
5.4 Effect of time on the dealloying process

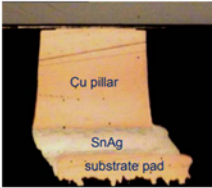
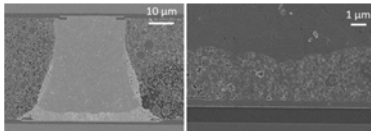
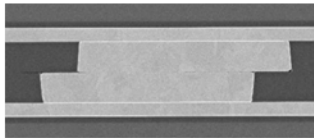
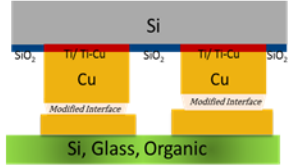
Cu-Zn on Bumps
Plated at -1.50 V for 45 min
~25:75 Cu:Zn Initially
Dealloyed in 0.3 wt% HCl

Change in **bump diameter** and increased **cracking** observed over time, as well as **coarsening** of NP-Cu- evaluating ways to reduce “delamination” and large cracks

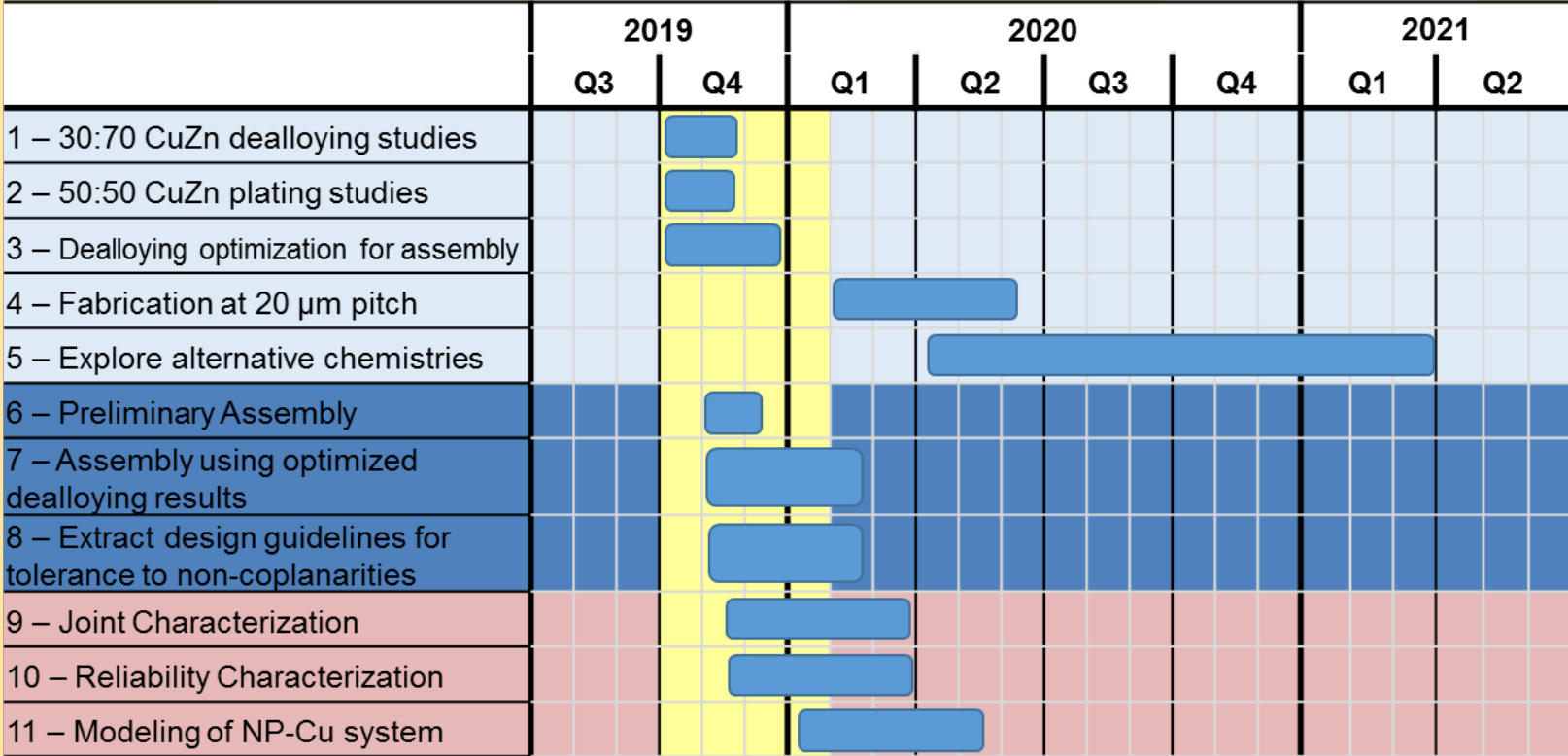


Dealloying kinetics need to be better understood- trivial to remove Zn at first, but difficult to leech remainder without compromising on bump shape and NP-Cu morphology



Parameters	State-of-the-art			Research objectives
	Lead-free solders (Cu μ -pillar TCB)	Nanoparticle Systems (IBM Zurich)	Direct Cu-Cu bonding (Xperi Hybrid)	
Package configuration				
	Universal	C2S	W2W	Universal
Pitch	Fine to large >35 μ m	Fine to large >35 μ m	Very fine <5 μ m	Very fine <20 μ m
Tolerance to non-coplanarities	High (>5 μ m)	High (>3 μ m)	Low (<<1 μ m)	High (>5 μ m)
Bonding parameters (Temp/pressure)	250°C 40 MPa	200°C 50.6 MPa	RT Oxide bond 200°C batch anneal	<250°C <20 MPa
Performance	Electromigration	<10 ⁴ A/cm ²	<10 ⁶ A/cm ²	10 ⁶ A/cm ²
	Thermomechanical Reliability	JEDEC standard JESD22-A104 thermal cycling at -55/125C, 1 cycle/h		

- ❑ Solving the problem of dealloying is non-trivial: yet to fully understand how the many input parameters contribute to the resultant structure of the NP-Cu
- ❑ Focus will be on identifying a preliminary candidate for full assembly characterization of system
- ❑ Exploring different regions of the phase diagram planned for future experiments (50:50 Cu:Zn seems promising based on preliminary results)
- ❑ Exploring different plating conditions and dealloying conditions to yield better NP-Cu



Light blue: Fabrication tasks
 Dark blue: Assembly tasks
 Light red: Reliability characterization
 Light Yellow: Current time window