Feasibility of integrated single-stage 48V to 1V conversion using GaN power devices

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Acknowledgements

Research Centers ….

Liaisons ….

1. Introduction

Conventional board net: 12V

- ❑ Board net at its power limit
- ❑ High wiring costs: >70 kg, >2.5 km

Introduction of 48V board net:

- ❑ Enable new high-power applications
- ❑ More power/better efficiency, CO_2 reduction

Conventional power distribution: 12V

- ❑ High current/wiring cost
- ❑ Up to 10 PSU close to server blades

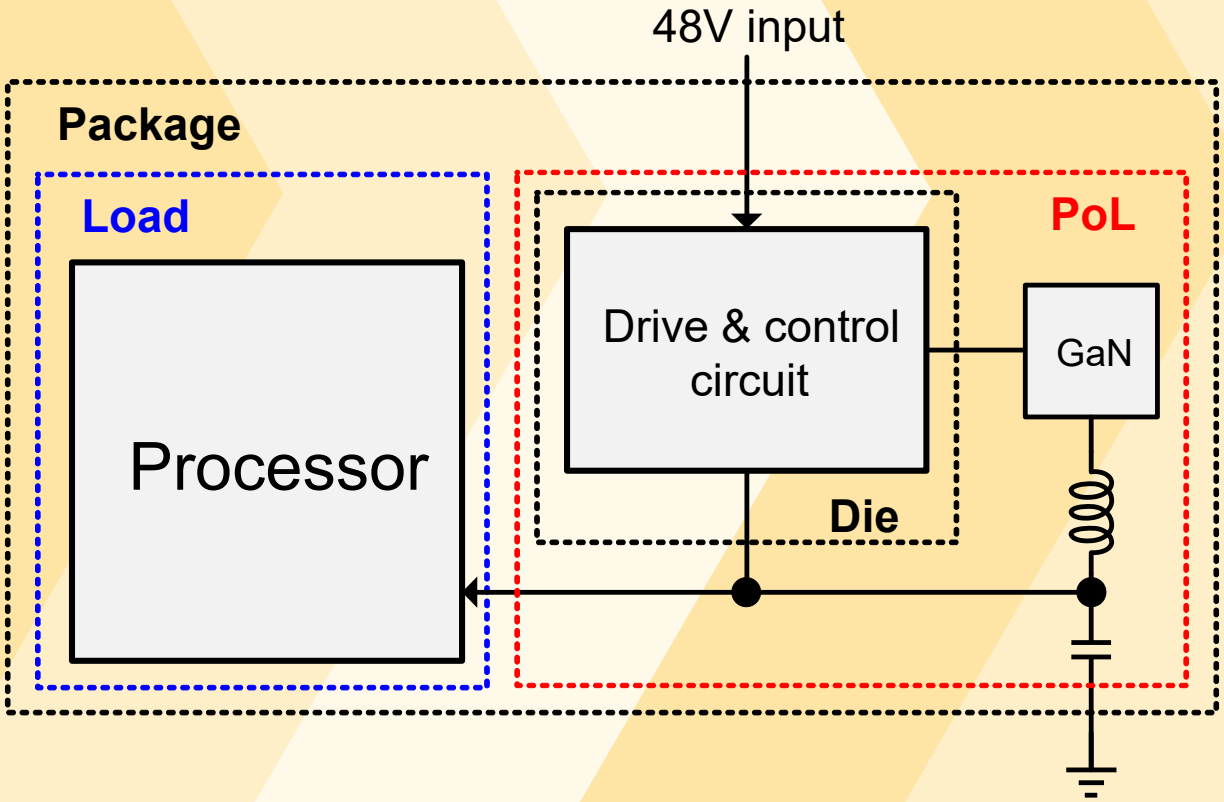
Introduction of 48V power distribution:

- ❑ Lower transmission loss
- ❑ 1 central PSU

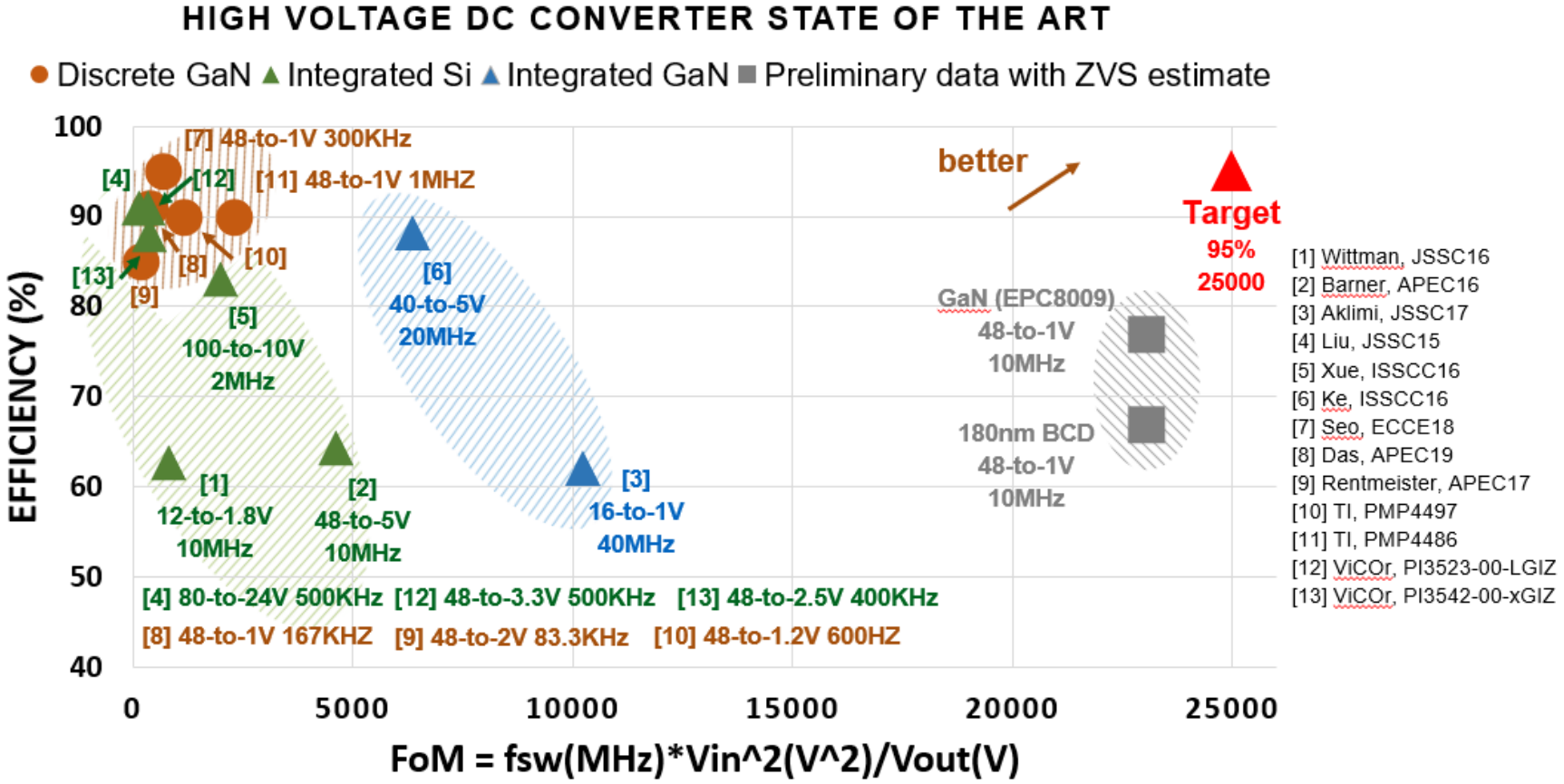
2. Target

A Integrated 48V to 1V single-stage DC-DC regulator for point-of-load:

- ❑ High efficiency (>90%), high output current (10A)
- ❑ Integrated with load chip in same package



3. State of the art



4. Topology

Linear regulator:

Cons:

- ❑ simple
- ❑ no switching noise
- ❑ low ripple

Pros:

- ❑ η = Vout/Vin

Switched capacitor:

Cons:

- ❑ Easy to integrate

Pros:

- ❑ Limited output current
- ❑ Complex control (more switches)

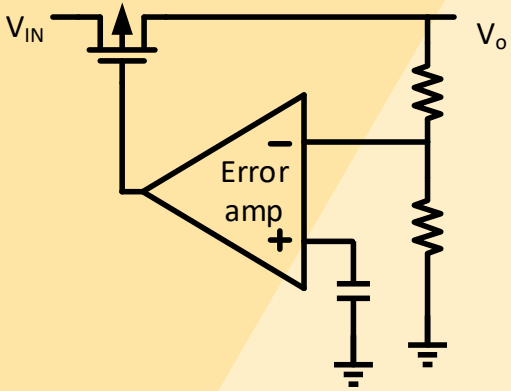
Switching regulators:

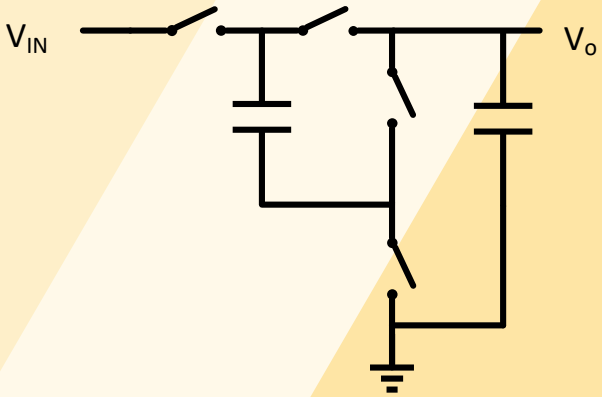
Cons:

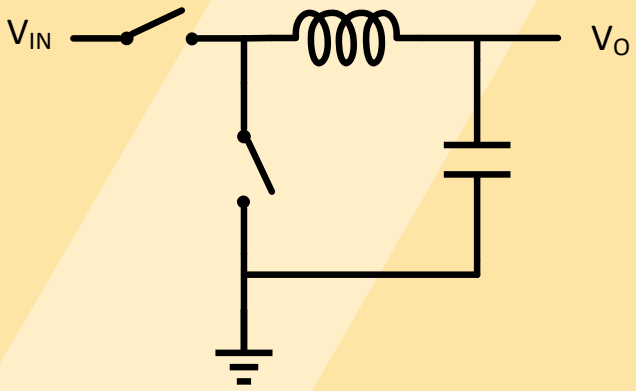
- ❑ High efficiency at high input voltage
- ❑ Passive scales with frequency

Pros:

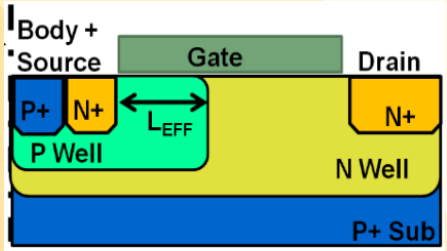
- ❑ Hard to integrate large passives
- ❑ High ripple
- ❑ Low efficiency at light load current

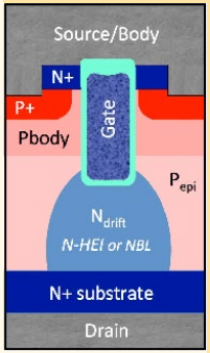


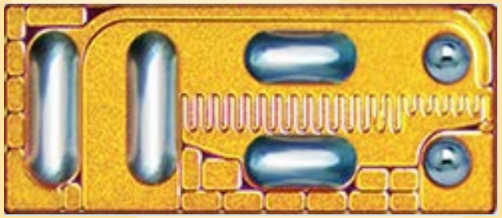




5. Silicon vs GaN





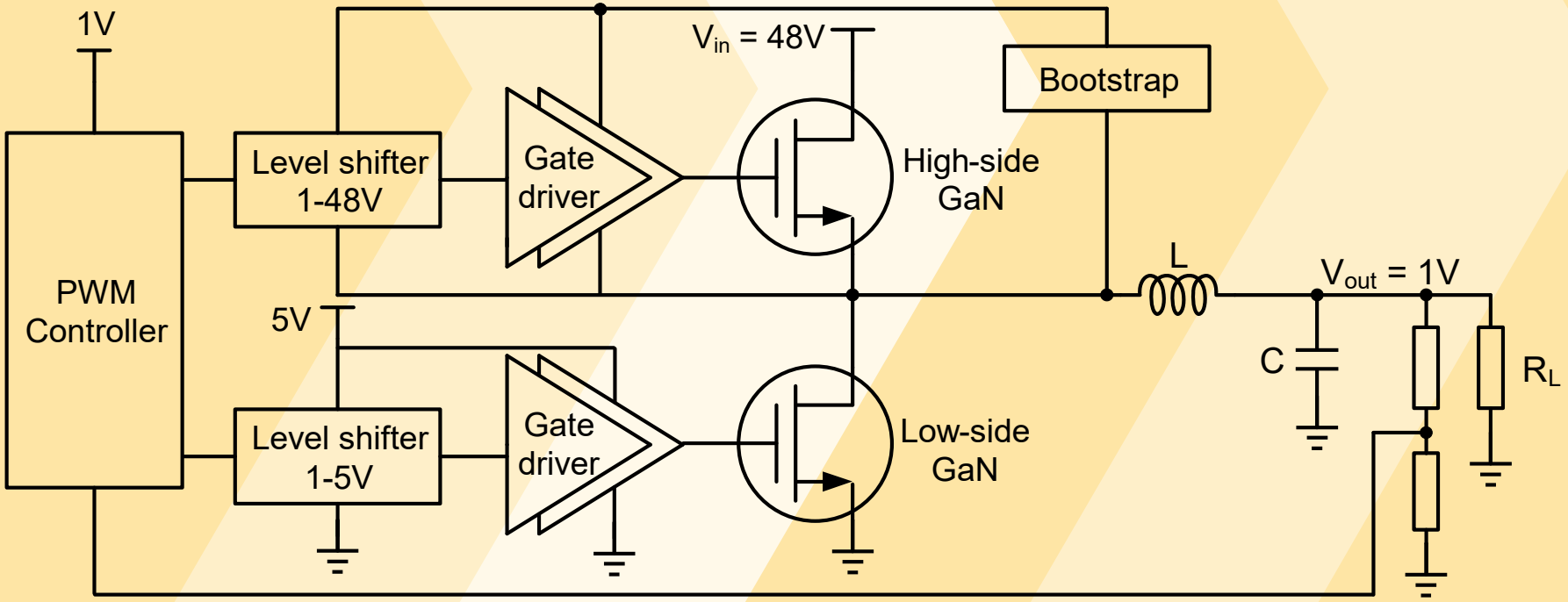


	Si – Lateral		Si – Vertical		GaN
Switch	Fully integrated		External		External
I_{out}	<5A		>5A		>5A
$Q_G \cdot R_{DSon}$	Low	2-5x	Medium	2-4x	High
$Q_{oss} \cdot R_{DSon}$	Low	10x	Medium	1.5x	High
$Area \cdot R_{DSon}$	Low	3X	Medium	1.5x	High
dV_{sw}/dt	<50V/ns				Up to 500V/ns

Comparison between silicon and GaN power devices

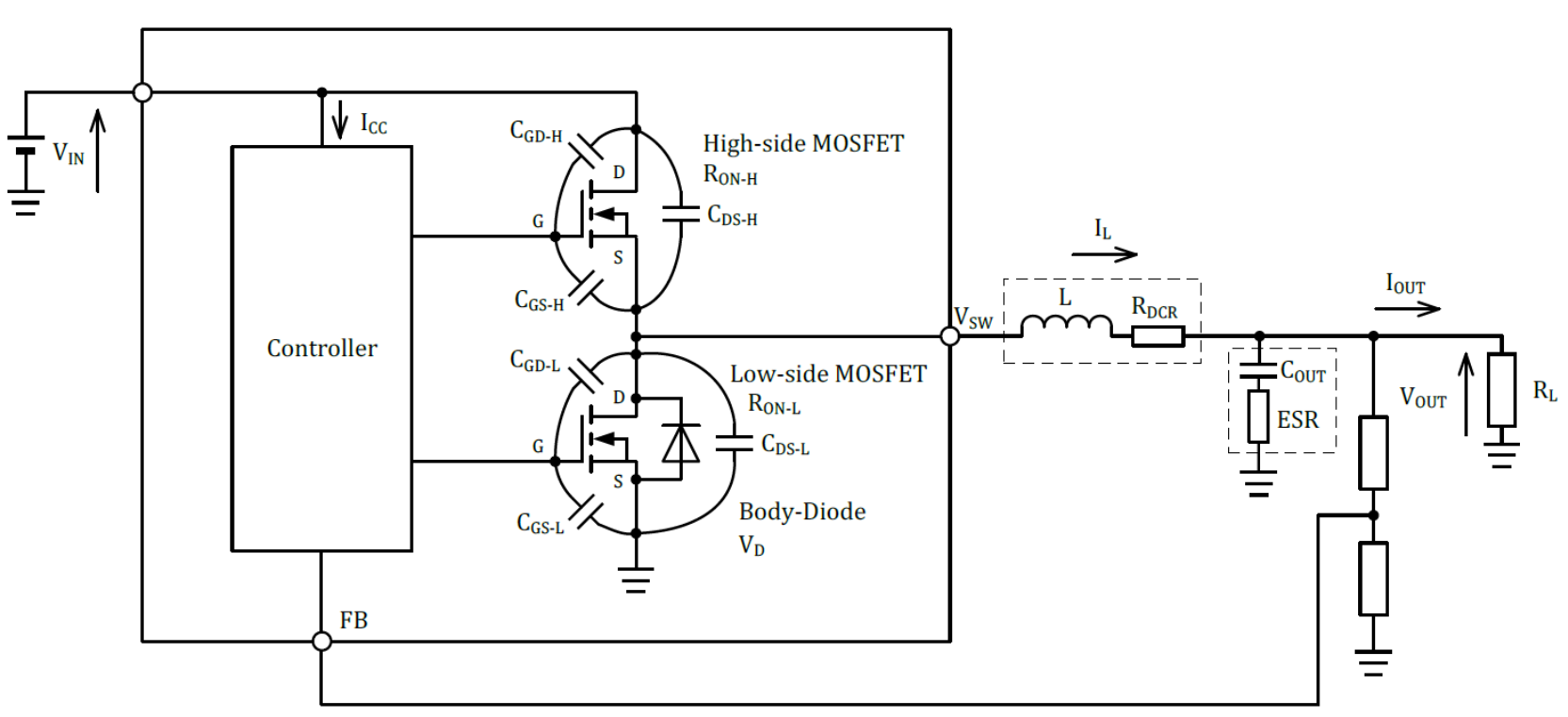
Synchronous buck converter with GaN power devices:

- ❑ Low voltage PWM controller: voltage regulate and dead time control
- ❑ Level shifter: signal voltage level changing
- ❑ Bootstrap circuit: high side GaN device drive
- ❑ Gate driver: provide enough drive strength for large GaN device



7. Loss analysis

7.1 Slide Subtitle

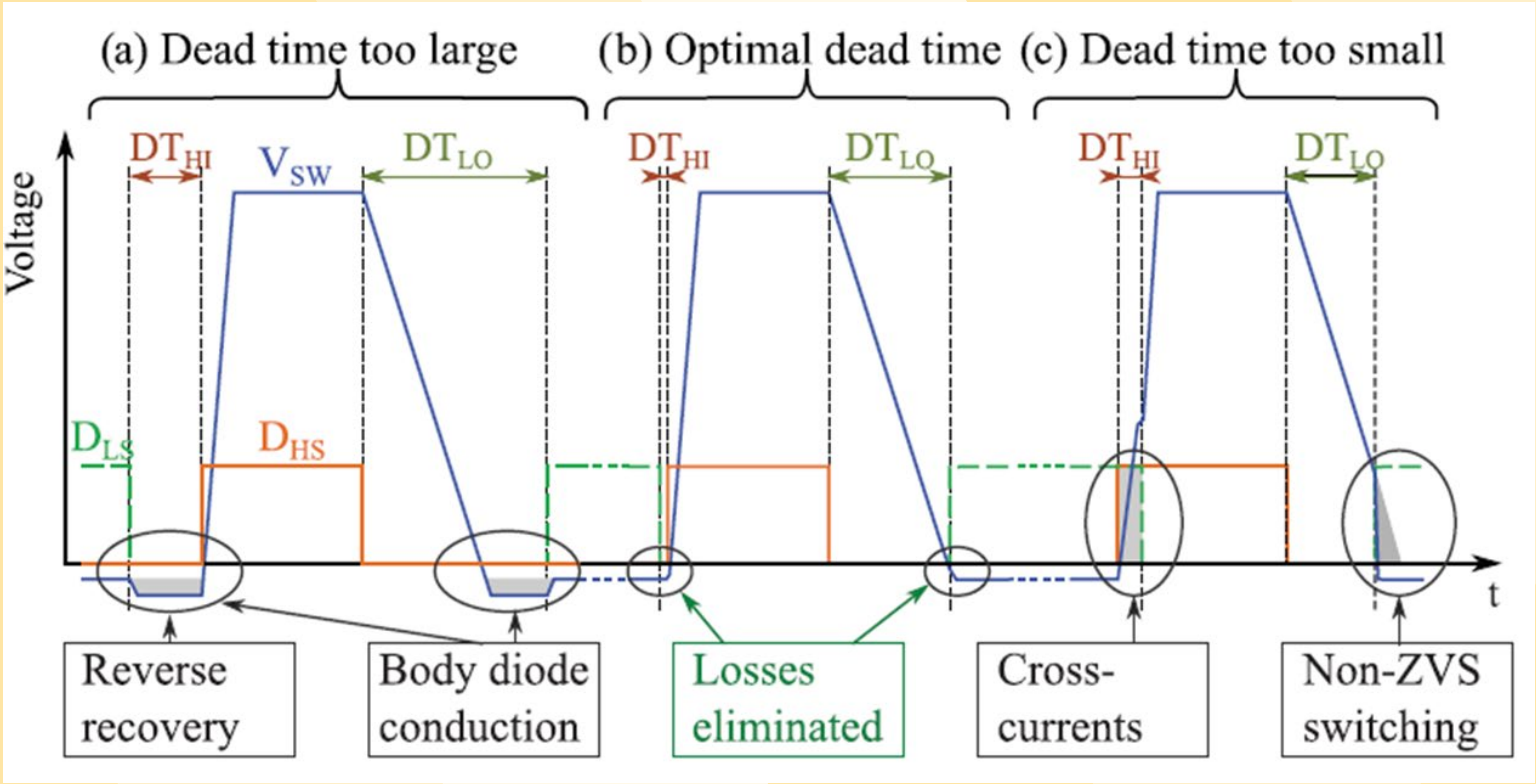


Main losses:

- ❑ Conduction loss
- ❑ Switching loss in MOSFET
- ❑ Reverse recovery loss of diode
- ❑ Dead time loss
- ❑ Output capacitor loss in MOSFET
- ❑ Gate charge loss
- ❑ Inductor conduction loss
- ❑ Capacitor loss

Dead time related losses:

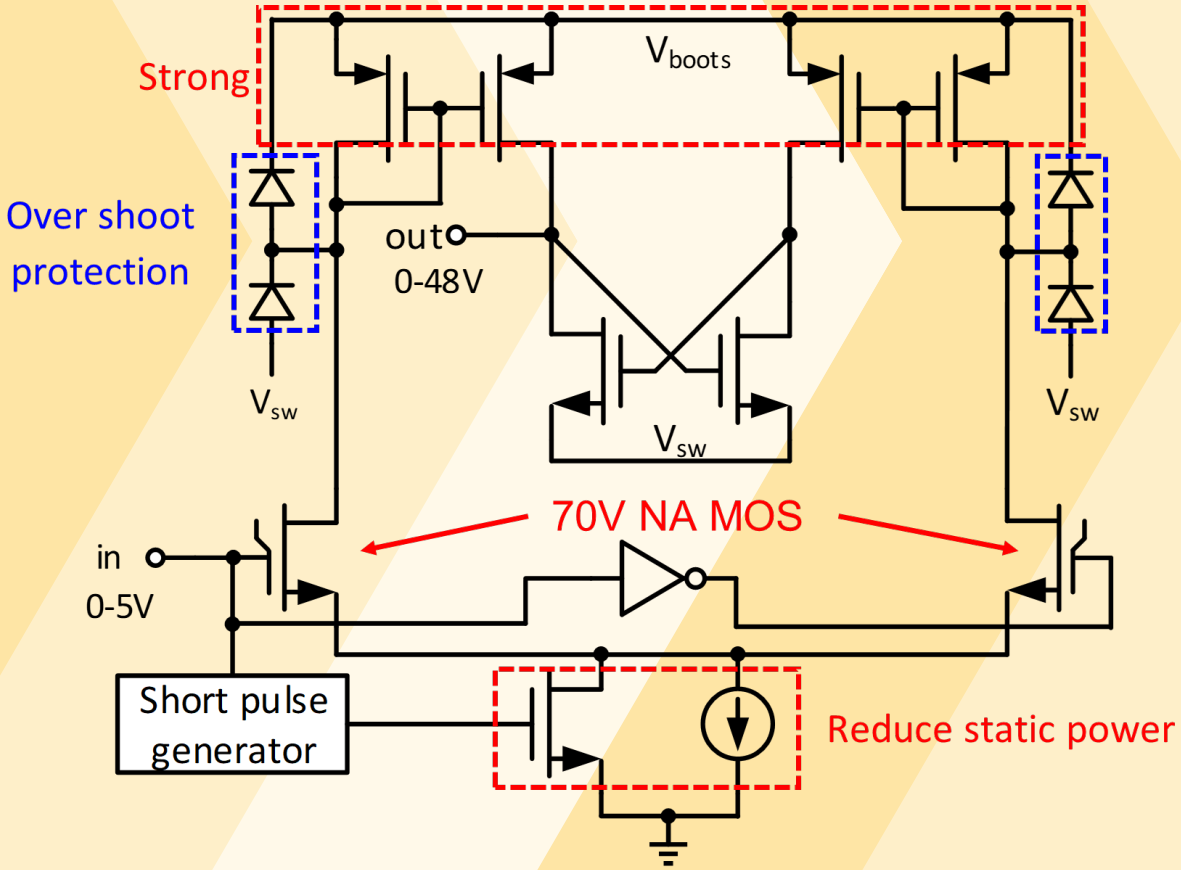
- ❑ Dead time too long: reverse recovery loss and body diode conduction loss
- ❑ Dead time too short: non zero-voltage switching (must avoid)
- ❑ Optimal dead time: loss eleminated



Dead time related losses [1]

Sub-nano delay high voltage level shifter:

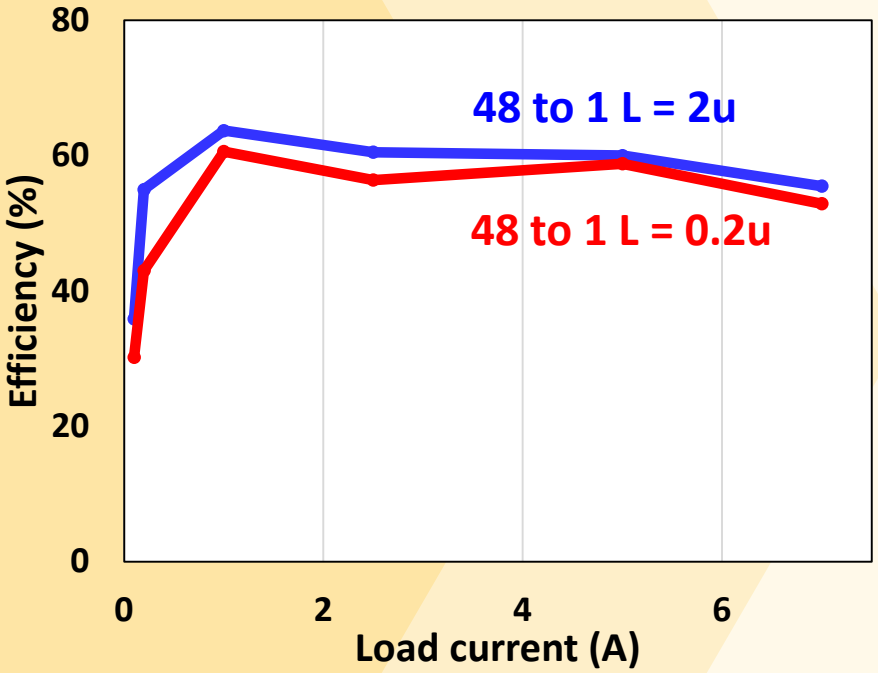
- ❑ High speed: dV/dt > 20V/ns
- ❑ Small delay: < 1ns
- ❑ Low static power



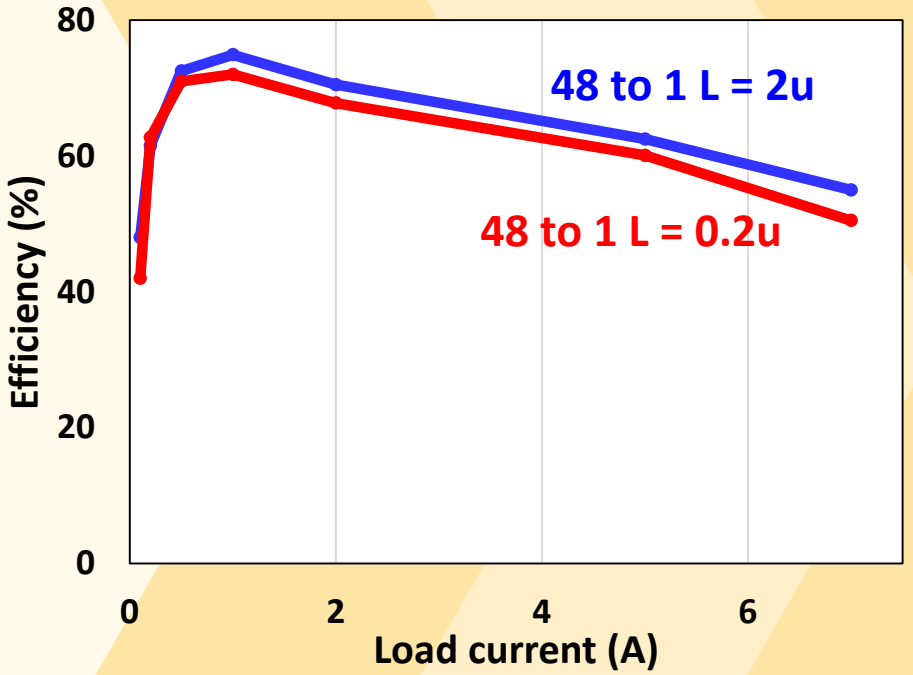
10. Results

10.1 efficiency

SPICE simulation results with GaN model and Verilog A



❑ With real ideal shifter

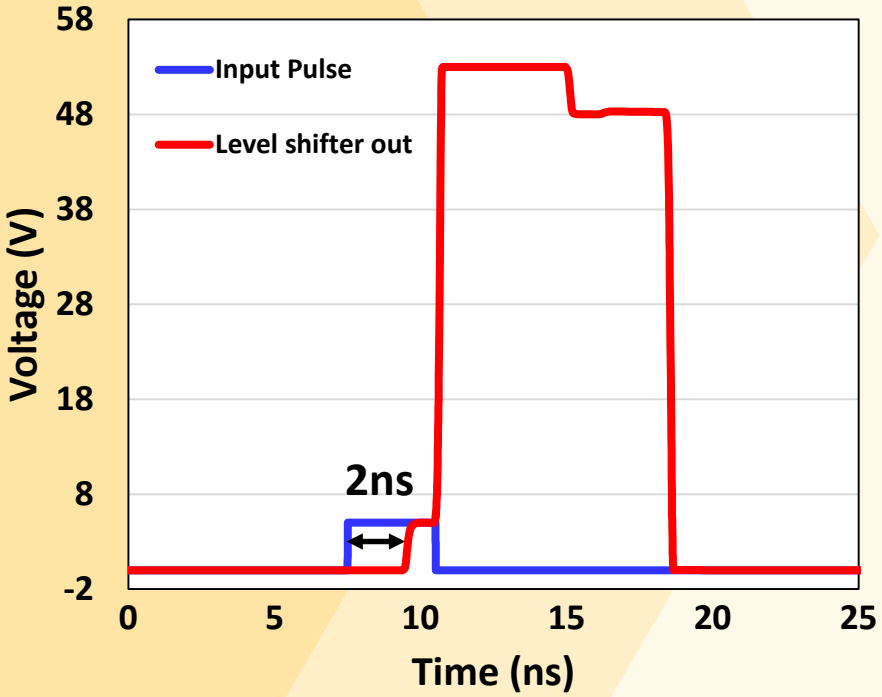


❑ With ideal level shifter

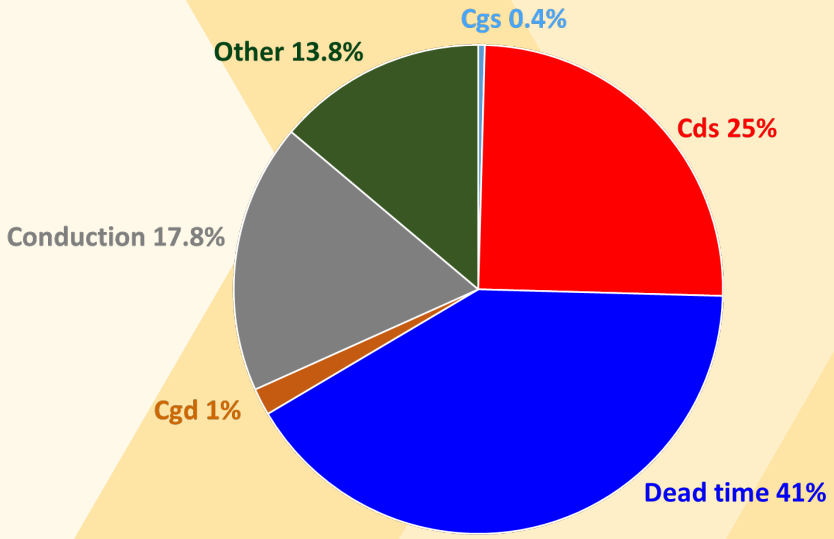
Level shifter delay is critical to dead time control

Simulation results of level shifter and loss breakdown

❑ Level shifter simulation



❑ Loss breakdown



❑ Dead time loss dominate

12. Conclusion

Conclusion:

- ❑ A feasibility study of single-stage 48V to 1V conversion
- ❑ Peak efficiency can achieve 75% with proper dead time control

Next step:

- ❑ New dead time control and current voltage sensing scheme
- ❑ High speed and high reliability level shifter

Reference:

- ❑ [1] Wittman, JSSC16
- ❑ [2] Barner, APEC16
- ❑ [3] Aklimi, JSSC17
- ❑ [4] Liu, JSSC15
- ❑ [5] Xue, ISSCC16
- ❑ [6] Ke, ISSCC16
- ❑ [7] Seo, ECCE18
- ❑ [8] Das, APEC19
- ❑ [9] Rentmeister, APEC17
- ❑ [10] TI, PMP4497
- ❑ [11] TI, PMP4486
- ❑ [12] ViCOr, PI3523-00-LGIZ
- ❑ [13] ViCOr, PI3542-00-xGIZ