Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse

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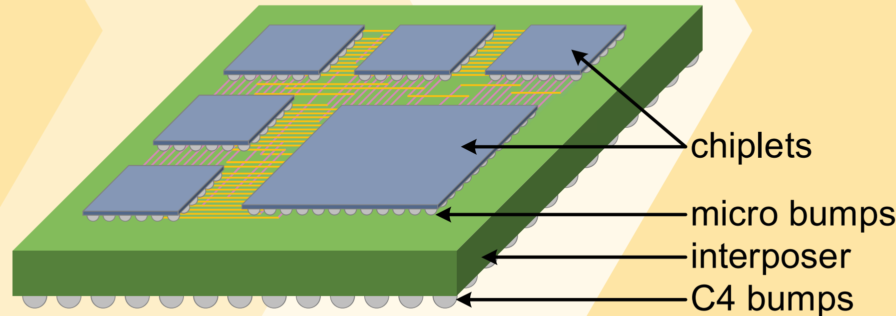
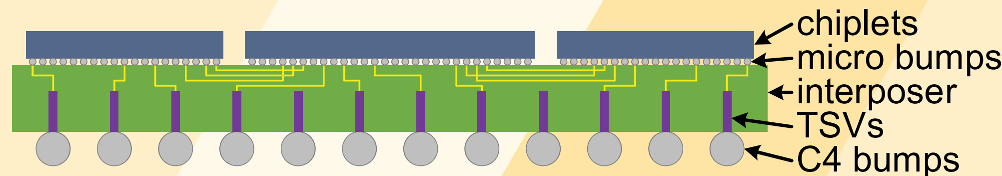
1. 2.5D Chiplet Integration with an Interposer

1.1 Chiplet Integration with an Interposer

- **Block-level heterogeneous integration**
- **Chiplet: independently designed IP**
  - **with most suitable technology node**
- **Simply reuse off-the-shelf chiplets**
- **Reduce design time and complexity**



(a) Interposer-based 2.5D IC

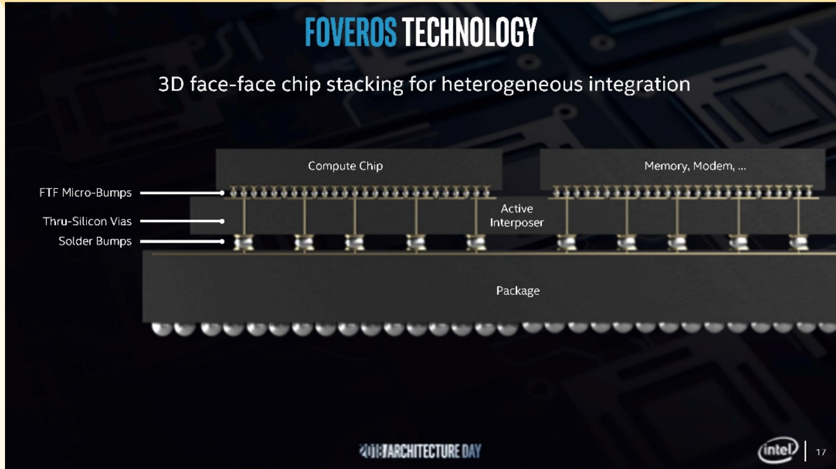


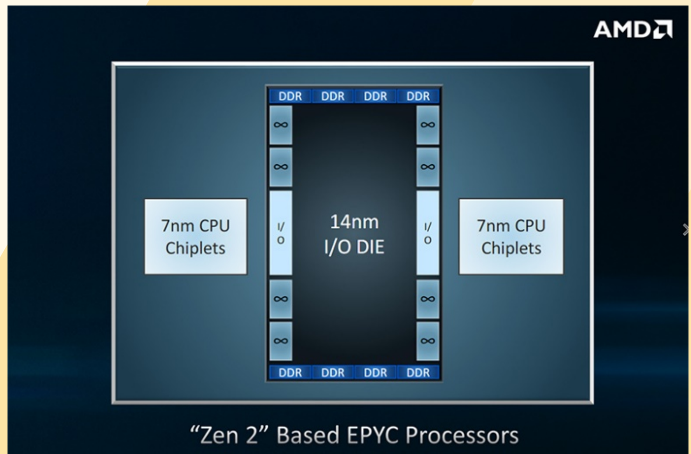
(b) Cross-section view of 2.5D IC

1. 2.5D Chiplet Integration with an Interposer

1.2 Comparison between Traditional Designs

	2D IC Design	2.5D Chiplet Integration	PCB IC Integration
Design time	Worst	Medium	Best
Performance	Best	Medium	Worst
Area	Best	Medium	Worst
Heterogeneity	Worst	Best	Best





Right1: Intel's FOVEROS product
Right2: AMD's 7 nm Zen 2 based EPYC processors

2. Contributions of This Work

- **We propose:**
  - **RISC-V based 64-core architecture as a benchmark design**
  - **A vertically-integrated EDA flow for 2.5D IC design**
  - **A new protocol, Hybrid-Link, for 2.5D chiplet communication**

- **We build a monolithic 2D IC and an interposer-based 2.5D IC**
  - **Technology node: commercial 28 nm and 130 nm**

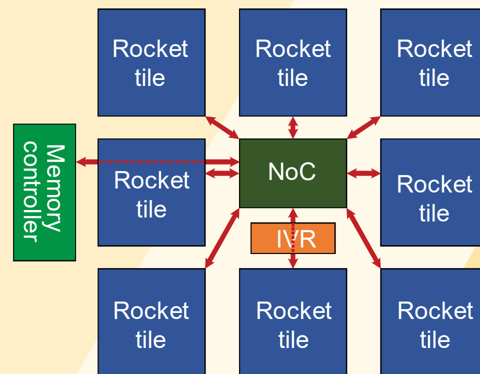
- **We analyze the power-performance-area overhead of 2.5D IC design**

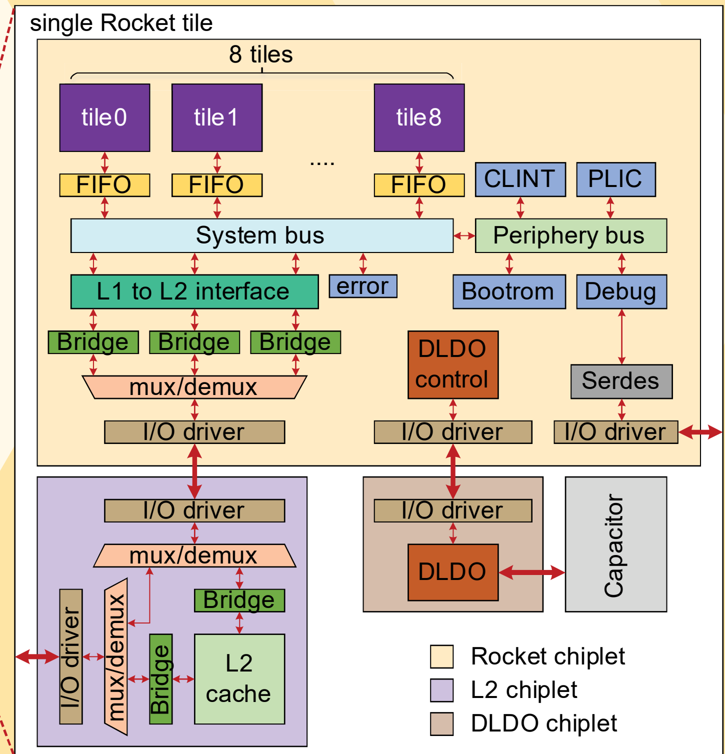
3. ROCKET-64

RISC-V-based 64-core Architecture

- 64 RISC-V cores [1] (5-stage in-order)
  - 2MB L1 & 8MB L2 cache
- Centralized Network-on-chip (NoC) arbiter[2]
- 4-channel memory controller
- Integrated voltage regulator & digital low-dropout regulator

The architecture of ROCKET-64 ►





[1] K. Asanovic et al., The Rocket Chip Generator, Technical Report UCB/EECS-2016-17, 2016
[2] Opensmart: Single-cycle multi-hop NoC generator in BSV and chisel

4. Hybrid-Link Protocol

A New Protocol for Chiplet Communication

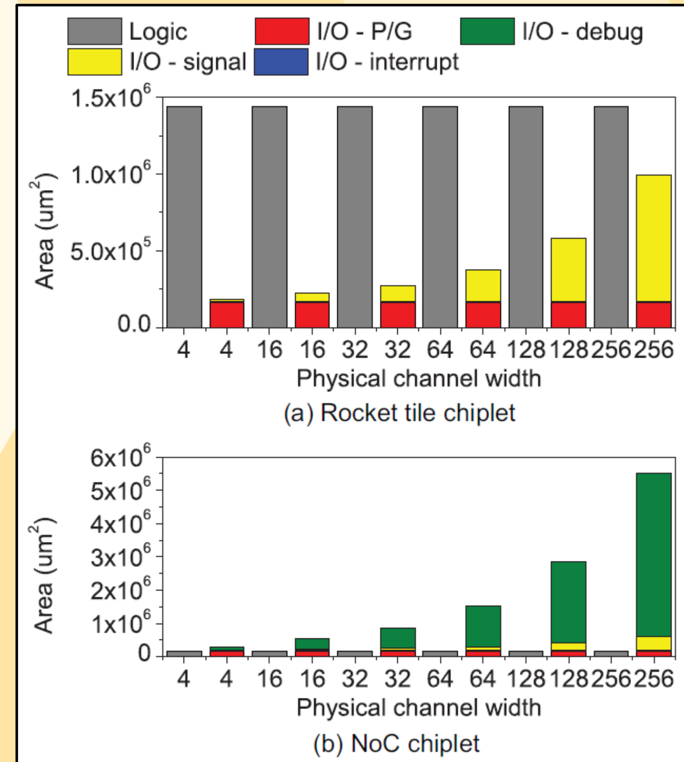
- **Default flit width: 40 bits**
  - **Lightweight mode: simple point-to-point connections**
  - **Extended mode: more complex transactions (e.g., coherence transactions from CPU to memory)**

Flit Stream (40 bit wide)	Protocol mode	CMD
	Lightweight	Read Req
	Extended	Read Req
	Lightweight	Write Req(4B)
	Extended	Write Req(4B)
	Lightweight	Read Resp(4B)
	Extended	Read Resp(4B)

Flit0 (Header) Flit 1 Flit 2

Lightweight /Extended [1b], Valid [1b], CMD [3b], Length [3b], Addr [32b], Data [32b], TID [6b], DID [6b], RSVD

▲ **Flit representation of Hybrid-Link**

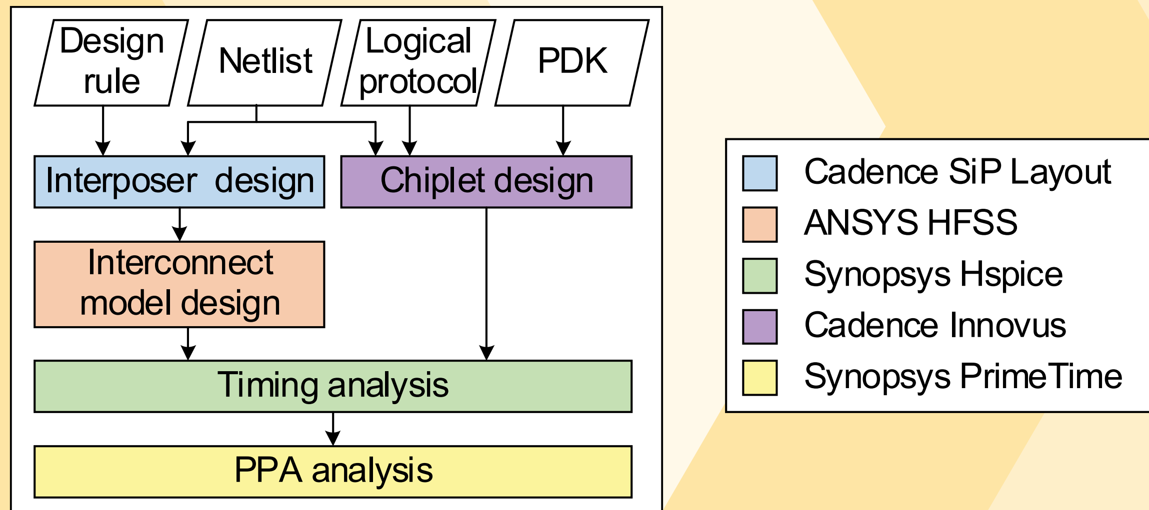


▲ **The size of chiplet vs. I/O counts**

5. A Vertically-integrated EDA Flow

5.1 Overall Flow

- Chip-to-package co-design and analysis flow
  - Using commercial tools
    - For design: Cadence SiP Layout, Cadence Innovus, ANSYS HFSS
    - For analysis: Synopsys PrimeTime, Synopsys Hspice



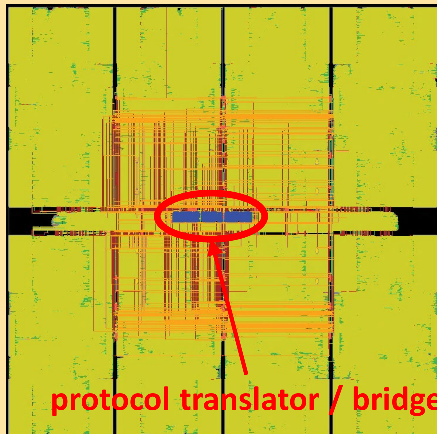
▲ A vertically-integrated EDA flow

5. A Vertically-integrated EDA Flow

5.2 Chiplet Design (commercial 28 nm/130 nm PDK)

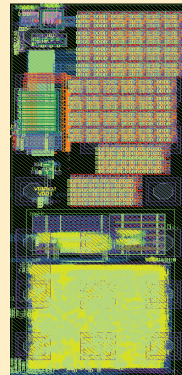
- Regular bump assignment
  - P/G bumps at periphery and signal bumps in the center
- Area I/O placement
  - I/O drivers as macro cells
- Chiplet design results (GDS layouts)

28 nm



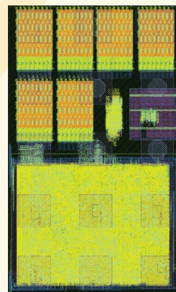
Rocket chiplet

130 nm



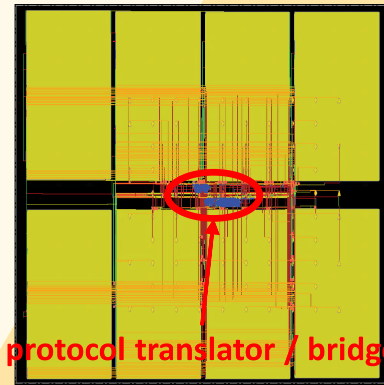
IVR chiplet

130 nm



DLDO chiplet

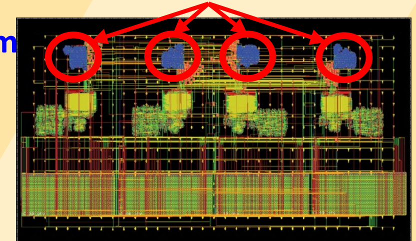
28 nm



L2 chiplet

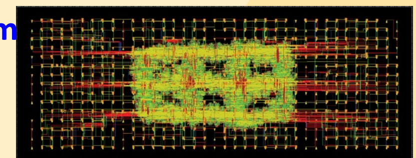
protocol translator / bridge

28 nm



Memory controller chiplet

28 nm



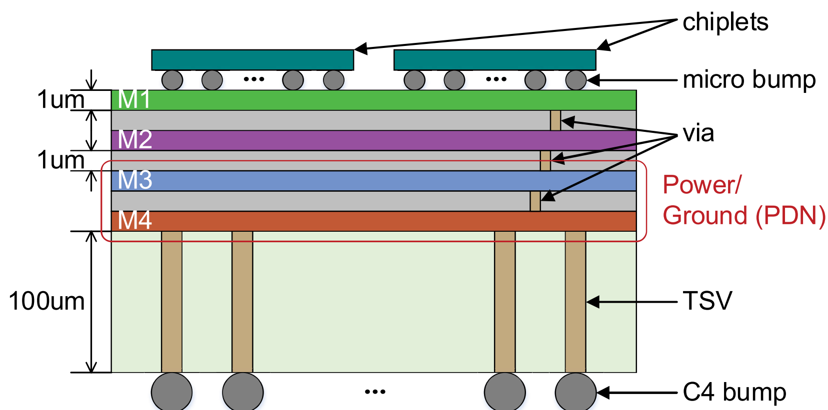
NoC chiplet

5. A Vertically-integrated EDA Flow

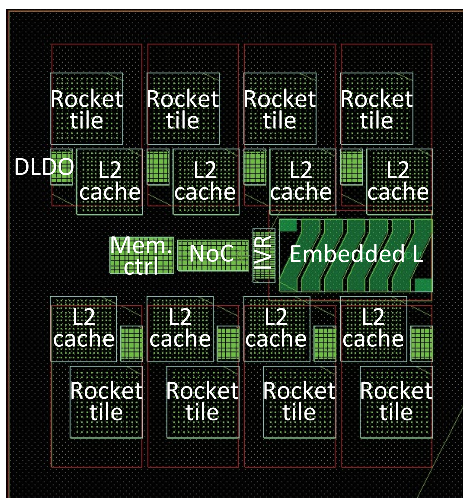
5.3 Silicon Interposer Design

1. Interposer technology file import
- based on TSMC CoWoS® [1]

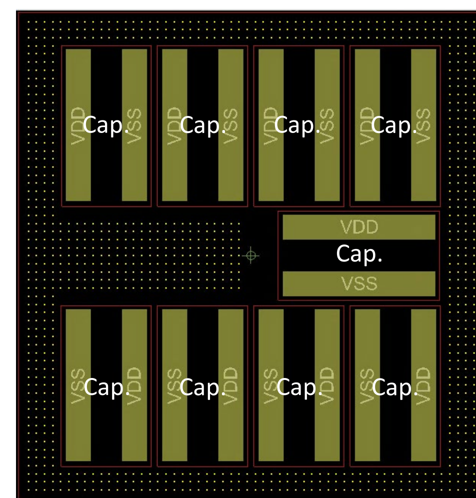
65nm Silicon Interposer Design Rules	
Metal layer #	4
Metal/dielectric thickness	1 μm/1 μm
Min. line width/spacing	0.4 μm/0.4 μm
TSV size/depth	10 μm/100 μm
Die-to-die spacing	100 μm
Micro/C4 bump pitch	40 μm/180 μm
PDN width/spacing	40 μm/90 μm



2. Chiplet placement
- 27 chiplets (6 types), 10 passives



(a) top side



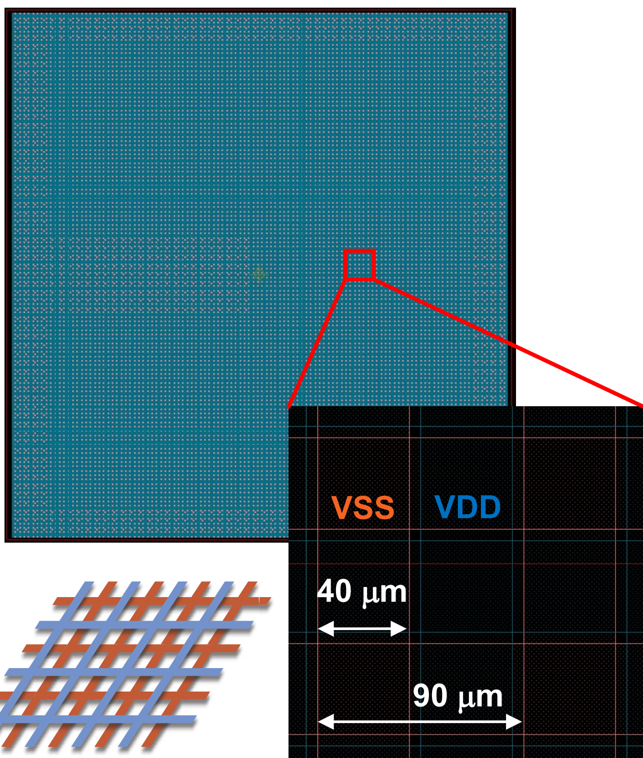
(b) bottom side

[1] R. Chaware et al., Assembly and reliability challenges in 3D integration of 28nm FPGA die on a large high density 65nm passive Interposer, ECTC, 2012

5. A Vertically-integrated EDA Flow

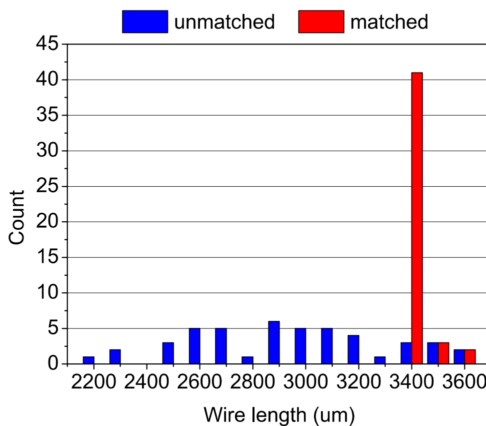
5.3 Silicon Interposer Design (continued)

3. Power distribution network placement - mesh type PDN



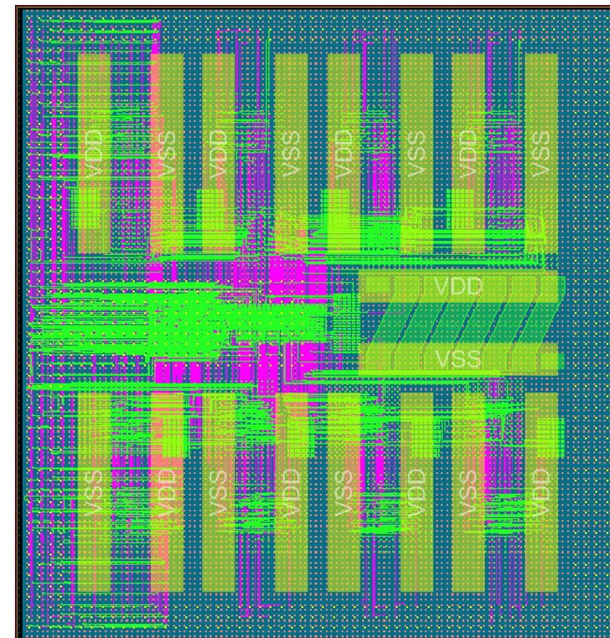
4. Interposer routing - Automatic Router (Manhattan routing)

- Match Group (data skew issue)



Silicon Interposer Routing Results	
Routed net #	1,441
Min. wire length	780 µm
Avg. wire length	3,781.9 µm
Max. wire length	7,020 µm
PDN DC resistance	20.1 mΩ
Footprint	111.65 mm^2

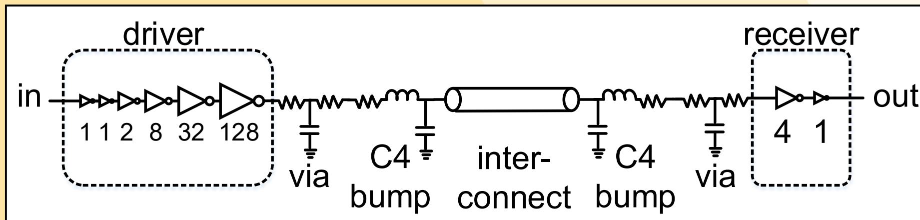
- Interposer GDS layout



5. A Vertically-integrated EDA Flow

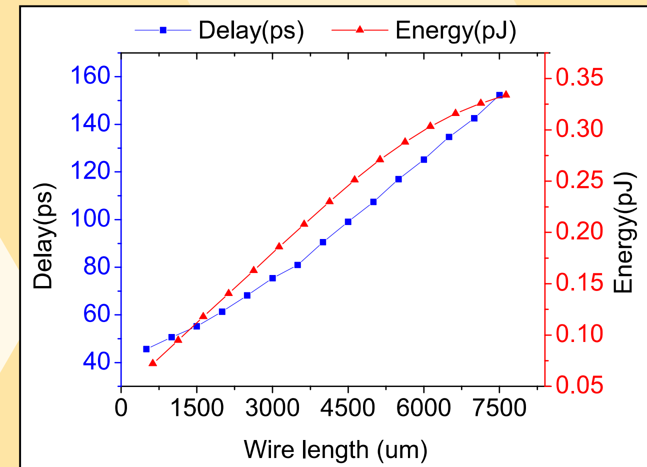
5.4 Timing/Power Analysis

- I/O driver design
  - Digital inverter with full-swing signal
  - Impedance matching to eliminate reflections
    - Final driver size: × 128 / Z_{out} = 47.4 Ω



▲ Timing simulation testbench

HSPICE simulation



Worst case propagation delay = 152.3 ps

Maximum power consumption = 0.33 mW

- Power calculation
  - To reflect various wirelength in silicon interposer.

$$P_{2.5D} = P_{CORE} + P_{I/O}$$

$P_{2.5D}$: total power of 2.5D design

P_{CORE} : the power of chiplet core

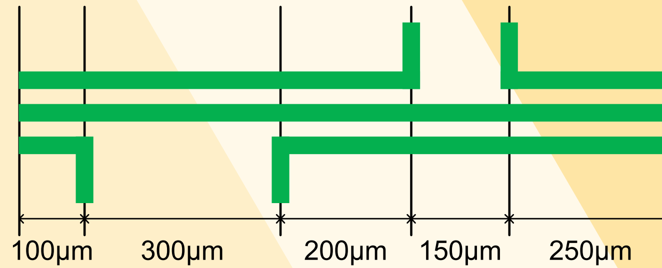
$P_{I/O}$: the power of I/O drivers

5. A Vertically-integrated EDA Flow

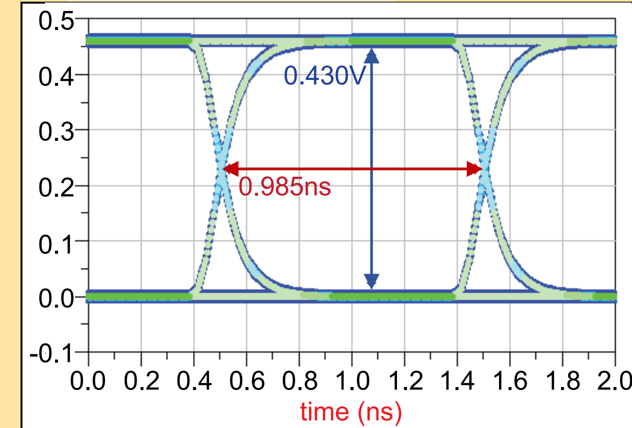
5.5 Signal/Power Integrity

- **Signal integrity on a complex interconnect channel**

Signal Integrity setup	
Data rate	1 Gbps
I/O driver impedance	50 Ω (ideal case)
Chiplet pad parasitic	2 pF

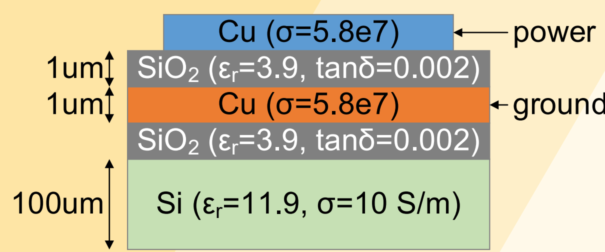


▲ Complex channel model

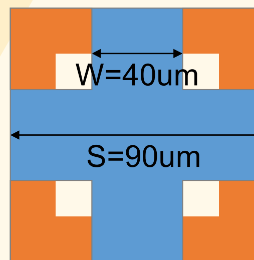


▲ Eye diagram

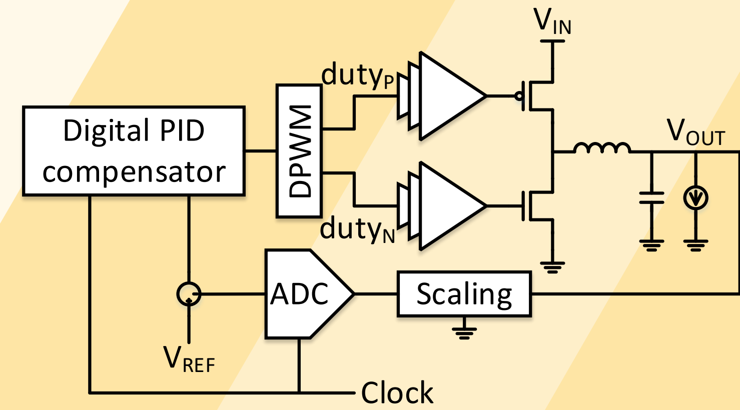
- **PDN model and IVR model for power integrity**
  - **PDN DC resistance: 20.1 mΩ**
  - **Power delivery efficiency: 89.7%**



(a) cross-ection view



(b) PDN unit cell



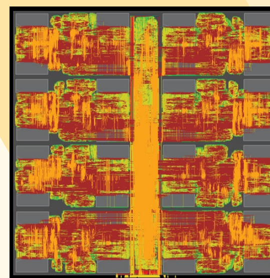
IVR block diagram

6. Monolithic 2D vs. Interposer-based 2.5D

PPA Analysis Result Comparison

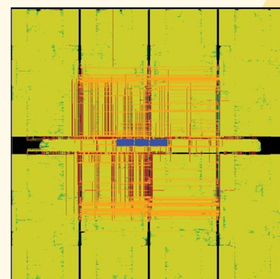
- The overhead of interposer-based 2.5D
  - 2.5x area
  - 1.008x total power
  - 17.0x average wire length

	2D Design	2.5D Design
Target Freq. (GHz)	1.0	1.0
Min. wirelength (µm)	0.3	780
Avg. wirelength (µm)	222.4	3,781.9 (17.00x)
Max. wirelength (µm)	1,435.1	7,020 (4.89x)
Cell #	7,887,365	7,979,736 (1.01x)
Total power (W)	8.948	9.023 (1.008x)
Logic power (W)	8.948	8.703 (0.97x)
I/O power (W)	-	0.320
Area (mm^2)	53.14	111.65 (2.5x)
Footprint (mm x mm)	7.29 x 7.29	10.30 x 10.84

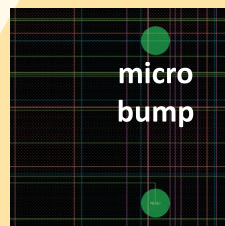


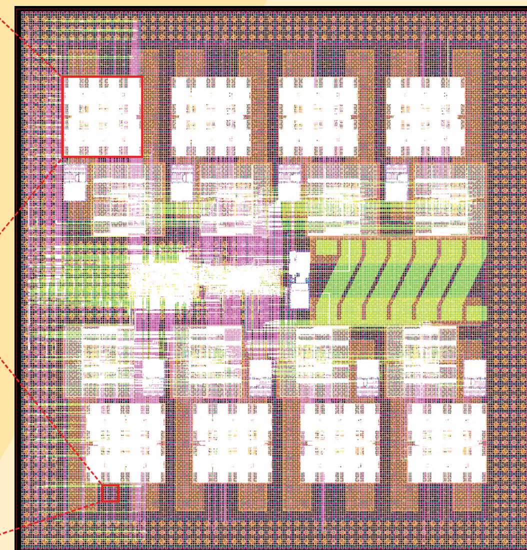
Rocket tile

(a) Monolithic 2D design



Rocket tile chiplet





(b) Interposer-based 2.5D design

7. Conclusion

- Our vertically-integrated EDA flow
  - Covers and fully automates the whole design phase of architecture, circuit and package
- ROCKET-64: RISC-V based 64-core architecture
  - 2.5D overhead: 2.5x area, 1.008x power, and 17.0x average wire length increment
- Hybrid-Link: a new standard protocol for 2.5D integration
  - Enables low number of chiplet I/Os with the full functions
- Our work, for the first time, serves as a full set of quantified comparison results of the 2.5D and 2D designs
  - enables the SoC designer to have an objective criteria of evaluating interposer-based design