RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs

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1. Introduction

- Monolithic 3D (M3D) IC: Maximize 3D IC benefits
  - Massive inter-tier connections: Inter-layer via (ILV)

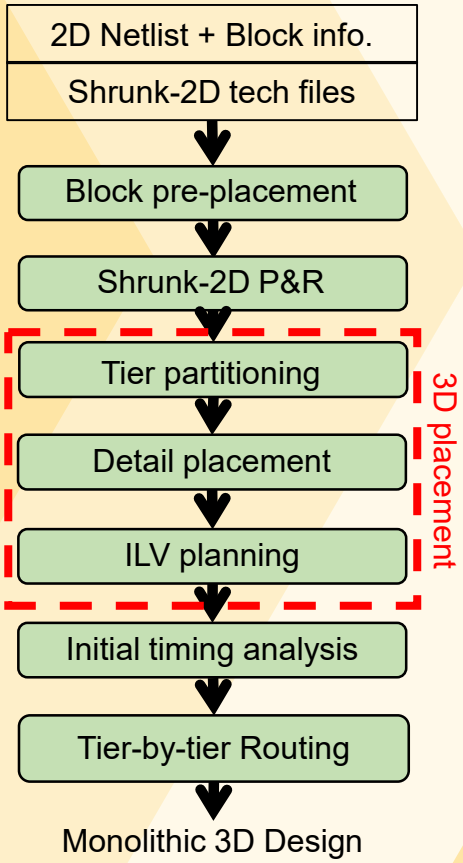
- Issues on M3D IC
  - Lack of EDA tools for M3D IC
  - ILV: Vulnerable to defects (shorts, opens, SAFs, …)
  - Resistive RAM (ReRAM): No automated methods

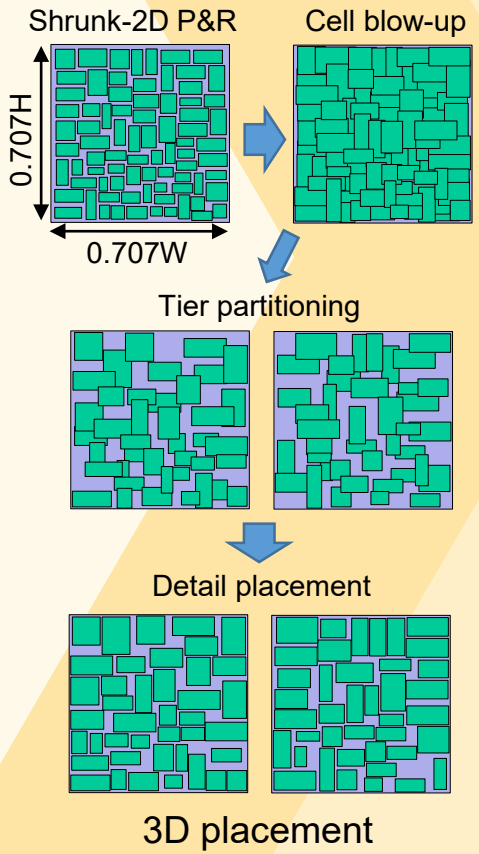
- This work proposes…
  - RTL-to-GDS design flow for M3D IC
  - Design-for-Test (DfT) method for ILV faults
  - ReRAM module generator

2. Monolithic 3D IC Design Flow

- RTL-to-GDS design flow is proposed
- 2D CAD tools are utilized

→ Guarantee commercial quality

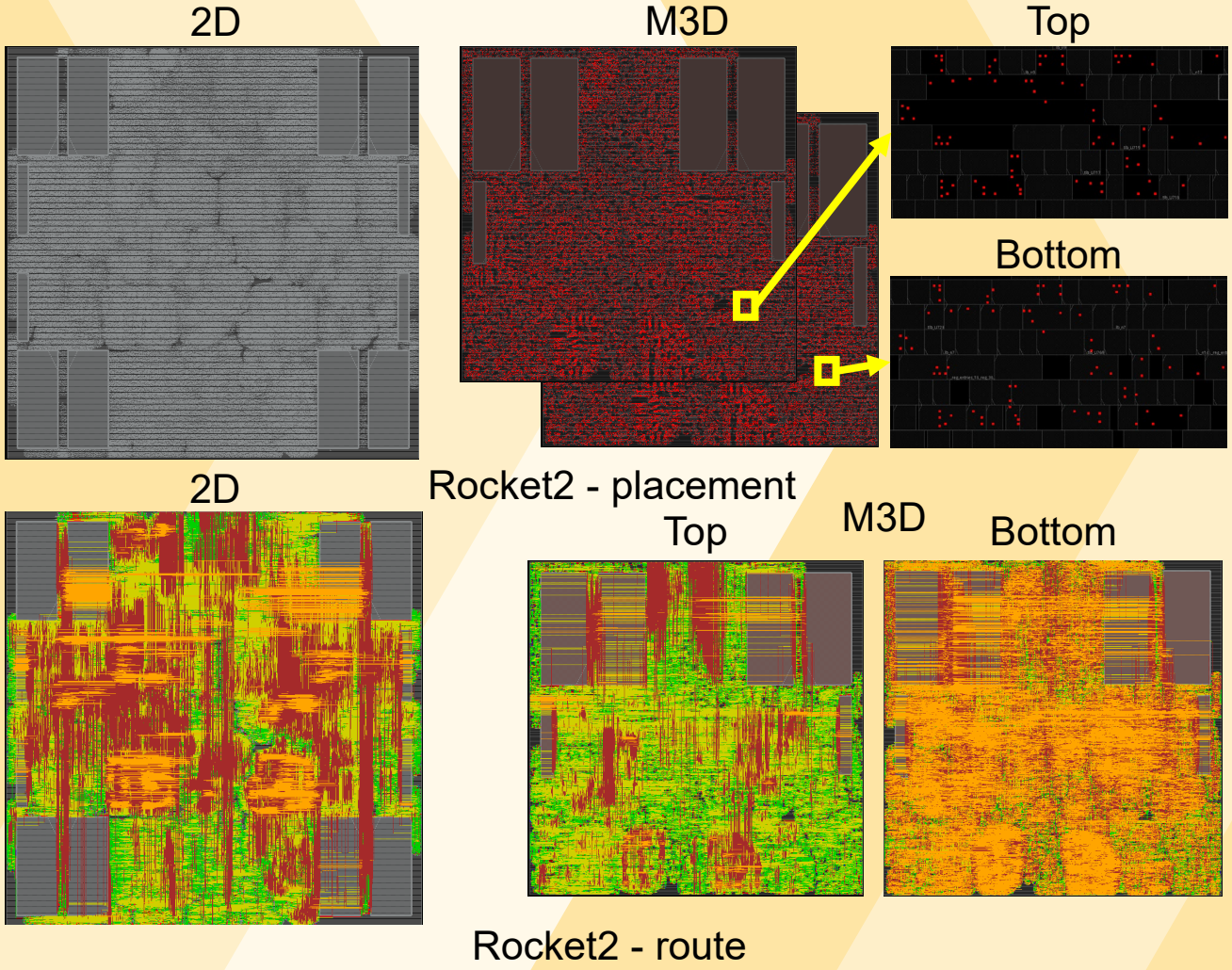




2. Monolithic 3D IC Design Flow

- Layout example: 2D & M3D – Rocket2

→ M3D: Nano-scaled ILVs are included



2. Monolithic 3D IC Design Flow

- TABLE: 2D vs. M3D – PPA comparison

→ Less power (-4%), Less area (-50%)

→ Comparable WNS: < 10% of clock period

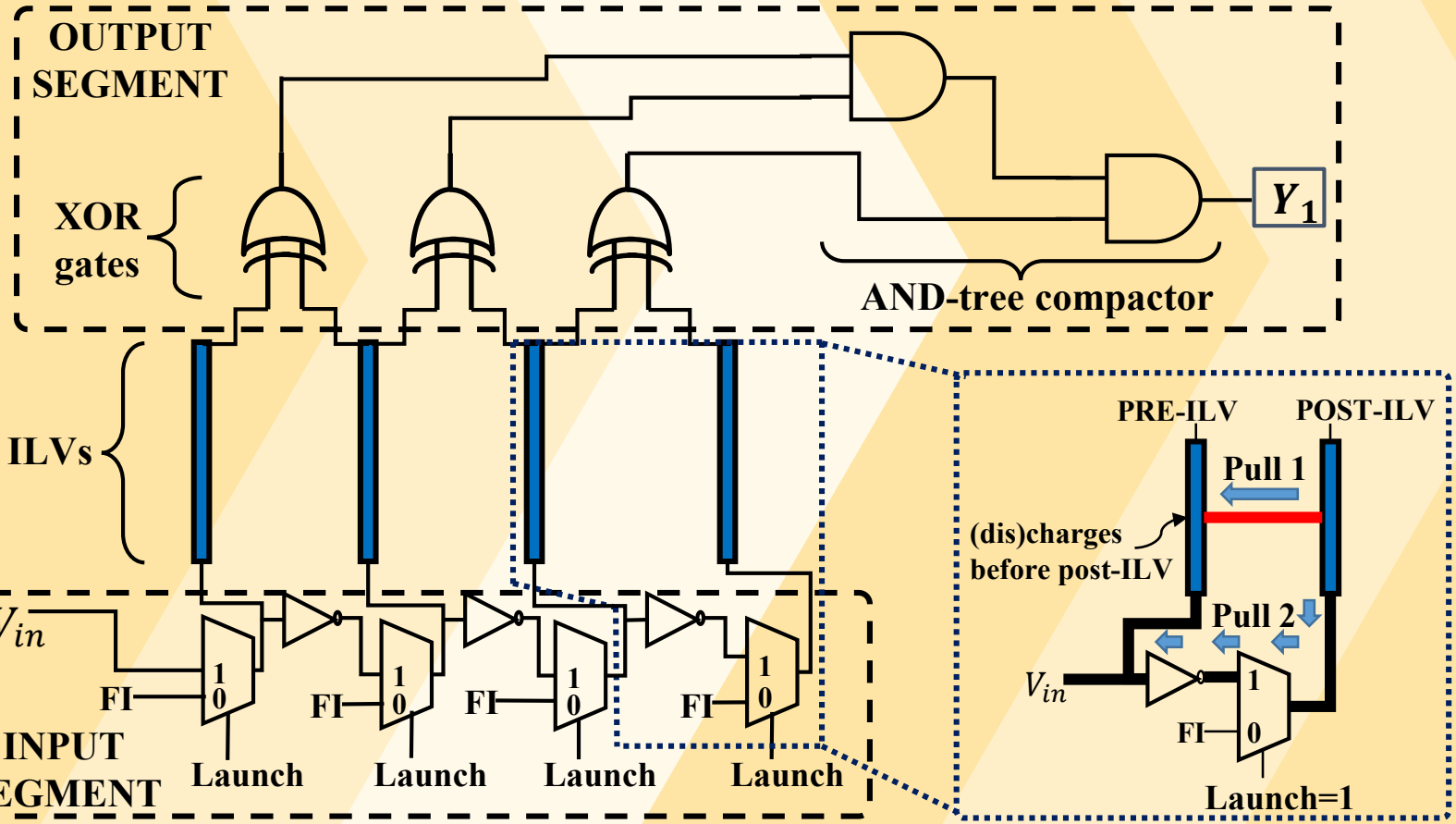
	Rocket2, 800MHz			AVC-Nova, 730MHz			AES-128, 3.44GHz		
	2D	M3D	Δ(%)	2D	M3D	Δ(%)	2D	M3D	Δ(%)
Footprint (mm^2)	0.746	0.373	-50.01	0.286	0.142	-50.21	0.210	0.105	-50.2
Std. cell count	279983	278622	-0.49	132725	132299	-0.32	109878	109634	-0.22
Std. cell area (mm^2)	0.363	0.362	-0.30	0.190	0.189	-0.79	0.124	0.121	-2.71
Wirelength (mm)	4712.46	4045.65	**-14.15**	2336.97	1954.92	**-16.35**	1494.13	1196.88	**-19.89**
ILV count	0	111395		0	56989		0	44782	
Total Pwr. (mW)	371.90	366.25	**-1.52**	122.50	120.31	**-1.79**	269.59	258.96	**-3.95**
Net Switching Pwr. (mW)	82.70	78.00	-5.68	23.55	22.32	-5.20	67.65	61.57	-8.99
Cell Internal Pwr. (mW)	224.84	224.26	-0.26	63.46	63.20	-0.41	174.66	171.86	-1.60
Leakage Pwr. (mW)	64.36	63.99	-0.58	35.50	34.79	-1.99	27.29	25.52	-6.48
Worst Neg. Slack(ps)	-54.27	-49.47		-60.48	-135.57		-14.88	-26.87	

3. Design-for-Test Solutions for M3D IC

- Built-in-self-test (BIST) architecture

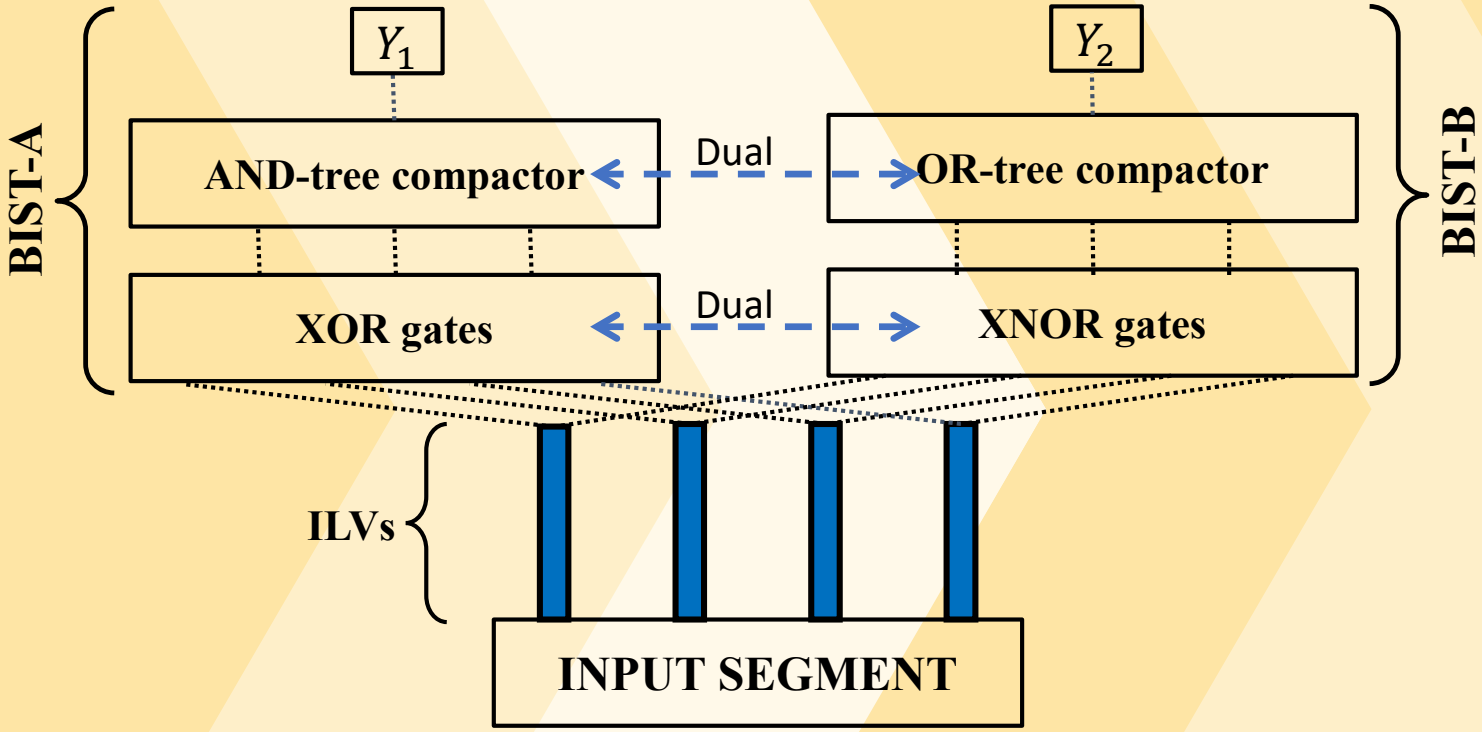
→ Test shorts, opens, and stuck-at-faults (SAFs)

→ Less power/area overhead



3. Design-for-Test Solutions for M3D IC

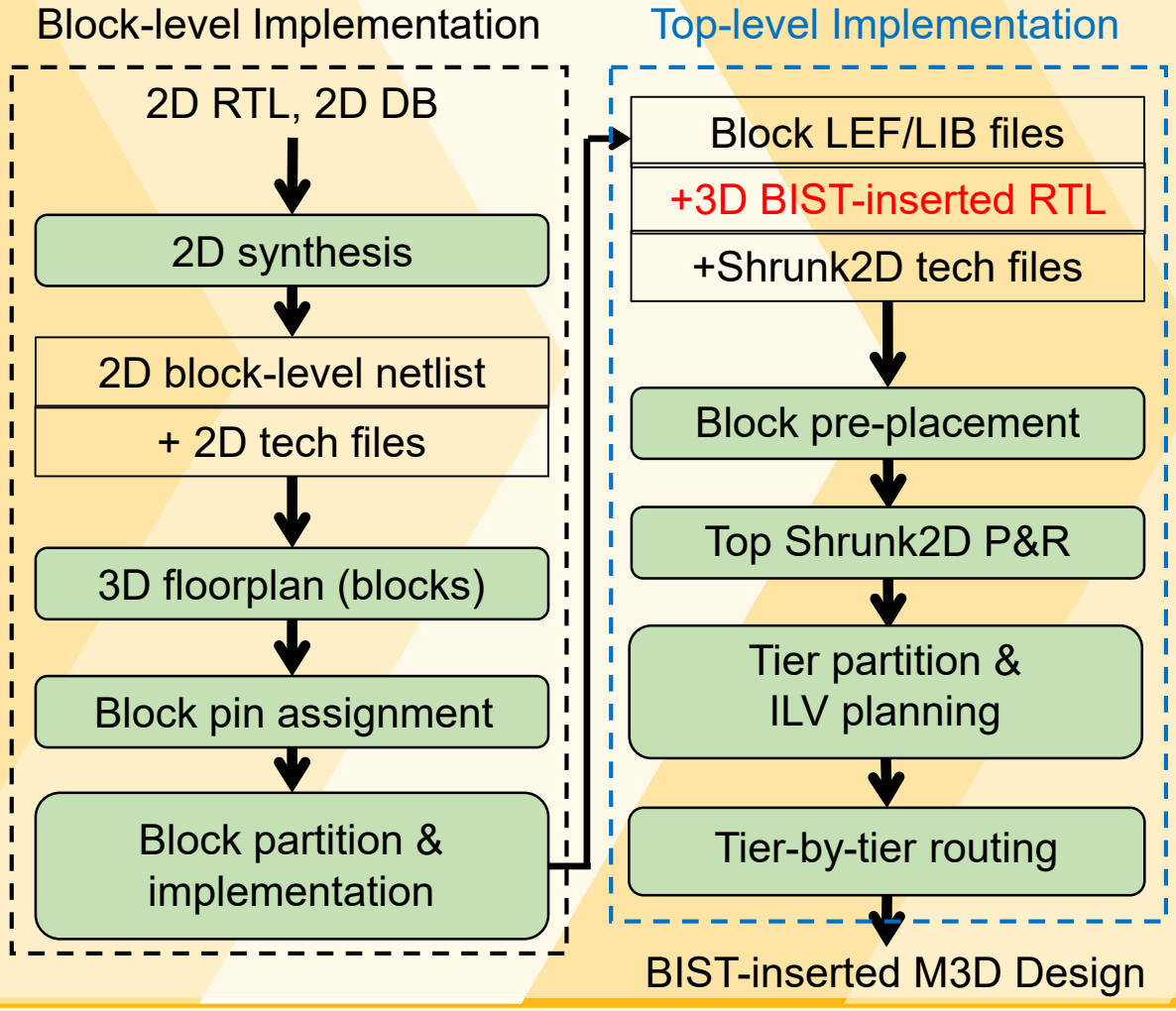
- Dual-BIST structure: minimize masking probability



3. Design-for-Test Solutions for M3D IC

- BIST-inserted M3D IC Design flow

→ Merge BIST architecture into M3D IC design flow



3. Design-for-Test Solutions for M3D IC

- TABLE: Overhead of BIST architecture

→ Area (1~2%), Power (2~8%)

Circuit	Metric	N-BI	BI	Overhead (%)
Rocket2	Cell area (μm^2)	382037.6	389785.6	2.03
	Power (mW)	227.3607	232.5544	2.28
AVC-Nova	Cell area (μm^2)	196841.5	199038.7	1.12
	Power (mW)	87.46587	90.79729	3.81
AES-128 (I)	Cell area (μm^2)	132049.9	134771.2	2.06
	Power (mW)	178.5411	194.3433	8.85
AES-128 (II)	Cell area (μm^2)	103632.4	106324	2.6
	Power (mW)	110.96	119.42	7.63

- TABLE: Area reduction of dual-BIST architecture

→ -32~38% w.r.t. original BIST

Benchmark	Baseline DfT (μm^2)	Dual-BIST (μm^2)	Reduction (%)
Rocket2	12288	7748	36.9
AVC-Nova	3246.1	2197.2	32.3
AES-128 (I)	4352	2721.3	37.5
AES-128 (II)	4362.2	2691.6	38.3

4. ReRAM Module Generator

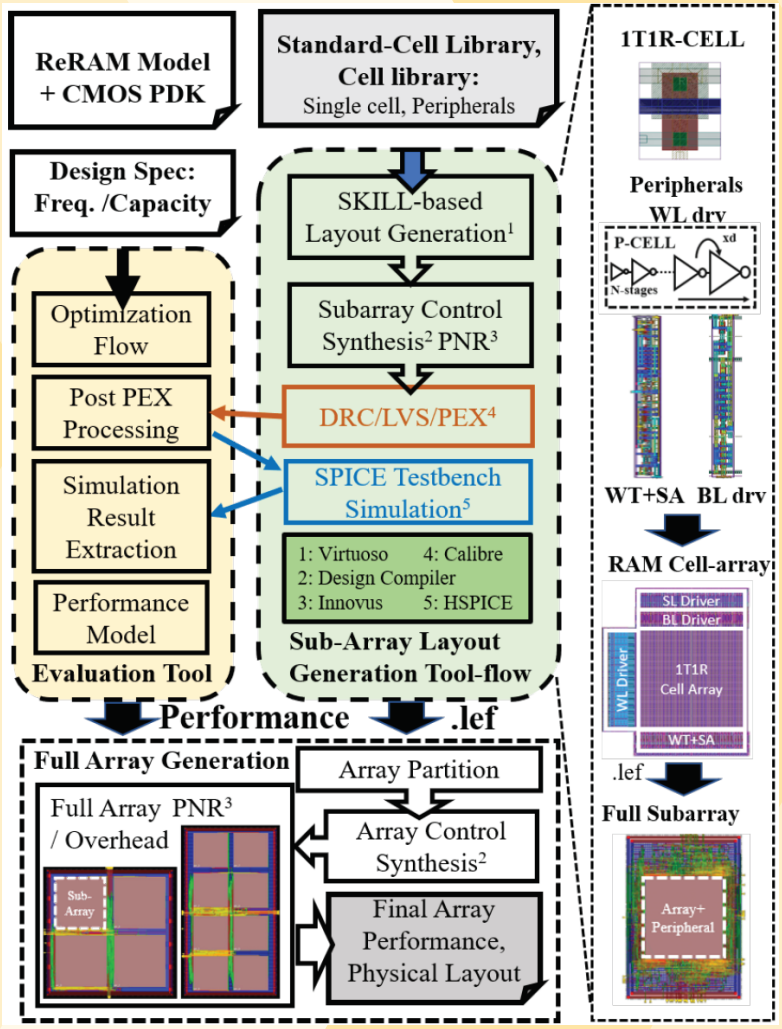
- ReRAM: On-chip non-volatile memory (NVM)
- Previous works
  - ReRAM device technology & custom macro design
  - ReRAM architecture analysis tool

→ Lack of EDA methods and tools for ReRAM sub-array & large macro design

4. ReRAM Module Generator

- ReRAM module generator: Top view

→ Sub-array design → Large macro → DSE



4. ReRAM Module Generator

- TABLE: Designs from ReRAM module generator

→ 1T1R ReRAM cells, 65nm CMOS technology

Sub-Array	Total Capacity 8kB			
	Area (mm^2)	R.E*(pJ)	W.E.*(pJ)	Top.E.**(pJ)
64x64	0.605	22.10	36.44	19.13
128x128	0.279	11.25	38.40	5.30
256x256	0.125	13.19	65.91	1.31
	Total Capacity 32kB			
64x64	2.421	64.14	78.48	61.17
128x128	1.073	30.08	57.24	24.14
256x256	0.530	19.01	71.73	7.13

References

Heechun Park, Kyungwook Chang, Bon Woong Ku, Jinwoo Kim, Edward Lee, Daehyun Kim, Arjun Chaudhuri, Sanmitra Banerjee, Saibal Mukhopadhyay, Krishnendu Chakrabarty, and **Sung Kyu Lim**, "RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs," in *ACM/IEEE Design Automation Conference (DAC)*, 2019

Acknowledgements

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