Inductor & Power-Stage Co-Design for 48V to 1V Integrated Voltage Regulators (HV-IVR)

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Outline

1. Motivation and Objectives

2. Figure of Merit (FoM)

3. Technical Approach

   • Challenges

   • Power Stage

   • Inductor and Comparison to Prior-Art

   • Co-Design Requirements

4. Results & Key Accomplishments

   • Proposed Inductor Structure

   • Fabrication Process

5. Summary and Schedule

Motivation

- Power Distribution Networks (PDN) in data centers and servers have multiple down-conversion stages from the AC grid to the SoC load.
- Many power loss sources in the PDN chain from 48V backplane to 1V System-on-Chip.
- System efficiencies can be as low as 70%

$\eta = 95\%$
48V to 12V VRM

$\eta = 93\%$
12V to 1.7V VRM

1.7V to 1.0V IVR

SoC

PDN Losses

$\eta = 92\%$
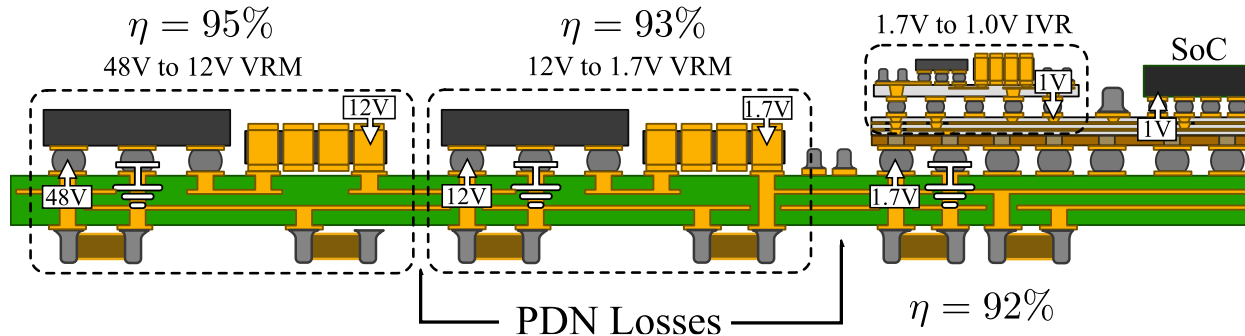
Objective

- Design and demonstrate a 48V to 1V IVR with GaN FETs and embedded inductors.
- Efficiency greater than 90% (Power stage: 95% and Inductor: 95%)
- 1V output voltage, 2.5A output current per phase
- 10 MHz switching frequency to allows passives components miniaturization

48V to 1.0V
Integrate Voltage
Regulator

C_{in} NGaN NGaN C_{out}
Power Stage
Copper Layers
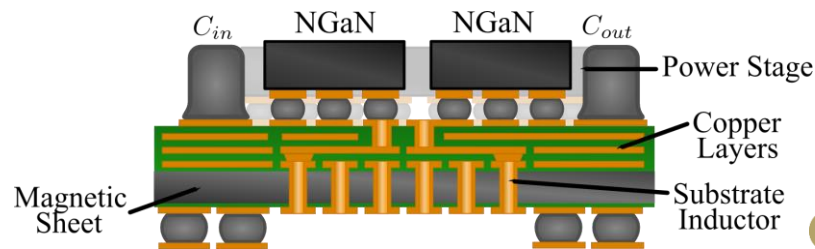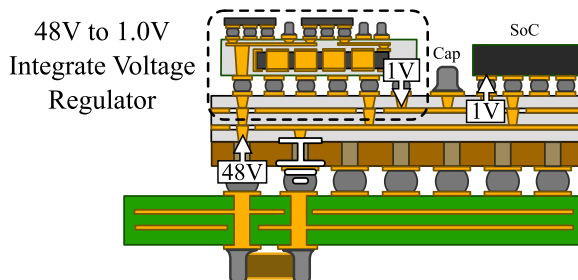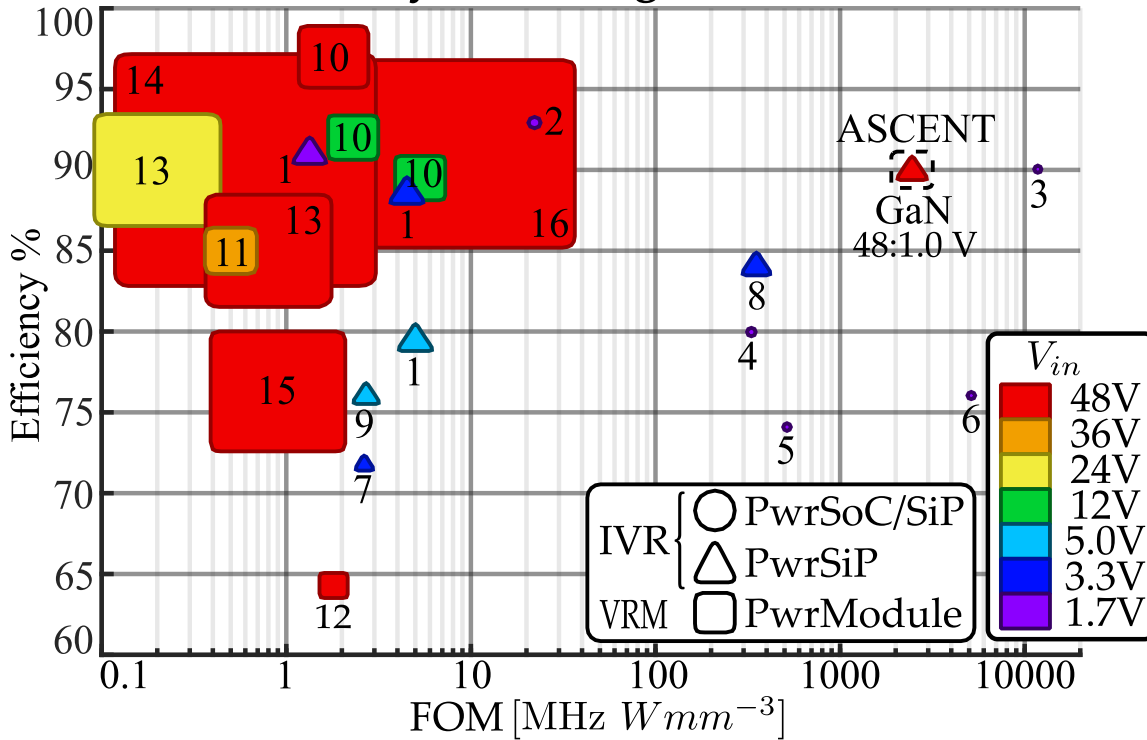Magnetic Sheet
Substrate Inductor

Figure of Merit (FoM)

Efficiency versus Figure of Merit 1

- The color represent the Input voltage.

- The shape represent the type of integration.

- And the size represent the relative solution volume.

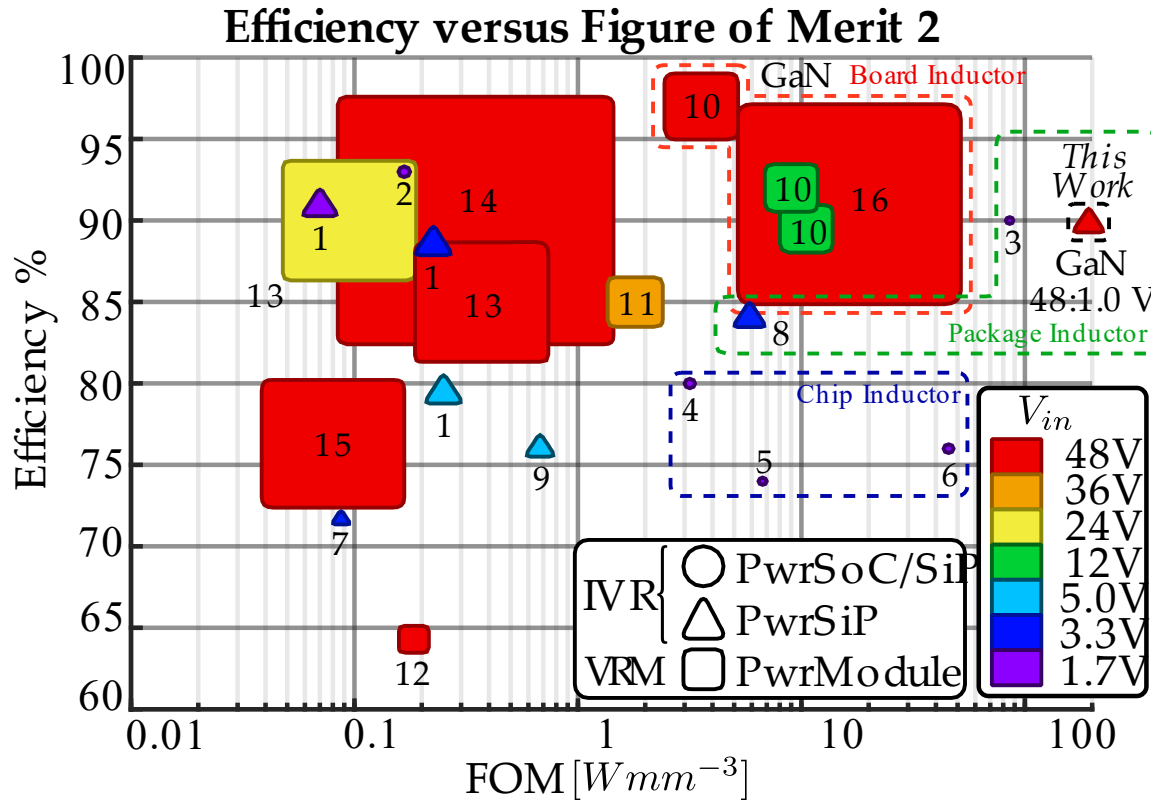- The frequency in the FOM makes it difficult (unfair) the comparison.

[1] 1.7:1.1 V   [3] 1.7:1.1 V   [7] 3.0:1.5 V   [11] 36:5.0 V   [14] 48:5.0 V
    3.0:1.0 V   [4] 1.8:1.2 V   [8] 3.3:1.0 V   [12] 48:5.0 V   [15] 48:5.0 V
    5.0:1.0 V   [5] 1.8:1.1 V   [9] 5.0:1.2 V   [13] 24:5.0 V   [16] 48:1.0 V
[2] 1.7:1.1 V   [6] 2.4:1.0 V   [10] 12:1.0 V   48:5.0 V
                        48:12 V

$$FOM1 = f_{sw} \cdot \frac{V_{in}}{V_{out}} \cdot V_{in} \cdot \frac{I_{out}}{volume}$$

Figure of Merit (FoM)

Efficiency versus Figure of Merit 2

[2] TSMC
[3,6,8] Intel **(140MHz)**
[4,5] Ferric **(100MHz)**
[9] Enpirion
[10] EPC Co. **(GaN, <1MHz)**
[11] Microchip
[16] TI **(GaN, <1Mhz)**

[1]	1.7:1.1 V	[3]	1.7:1.1 V	[7]	3.0:1.5 V	[11]	36:5.0 V	[14]	48:5.0 V
	3.0:1.0 V	[4]	1.8:1.2 V	[8]	3.3:1.0 V	[12]	48:5.0 V	[15]	48:5.0 V
	5.0:1.0 V	[5]	1.8:1.1 V	[9]	5.0:1.2 V	[13]	24:5.0 V	[16]	48:1.0 V
[2]	1.7:1.1 V	[6]	2.4:1.0 V	[10]	12:1.0 V		48:5.0 V		
					48:12 V				

$$FOM2 = \frac{V_{in}}{V_{out}} \cdot V_{in} \cdot \frac{I_{out}}{volume} = \frac{48}{1} \cdot 48 \cdot \frac{2.5}{5 \times 4 \times 1.5} = 192 \, \frac{W}{mm^3}$$

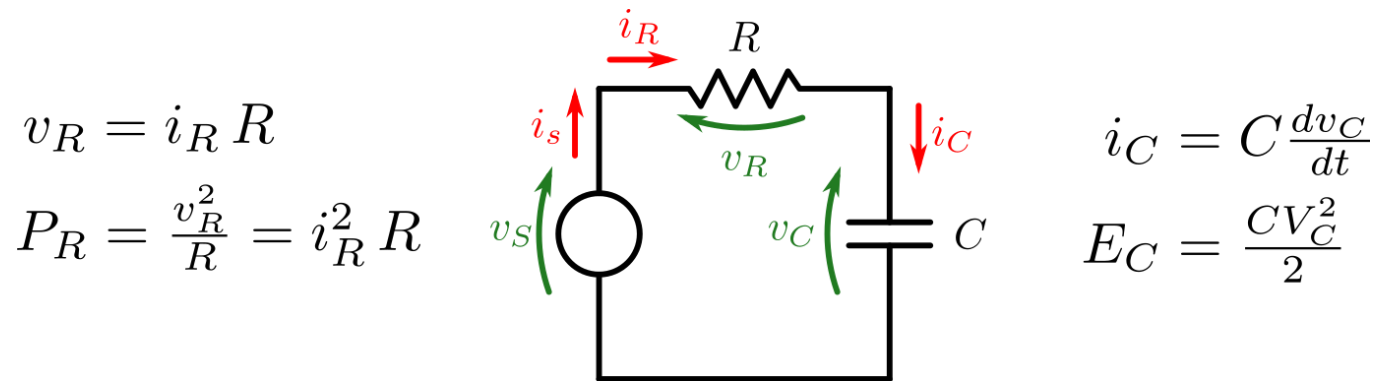# Challenges – An Intuitive Power Loss Analysis
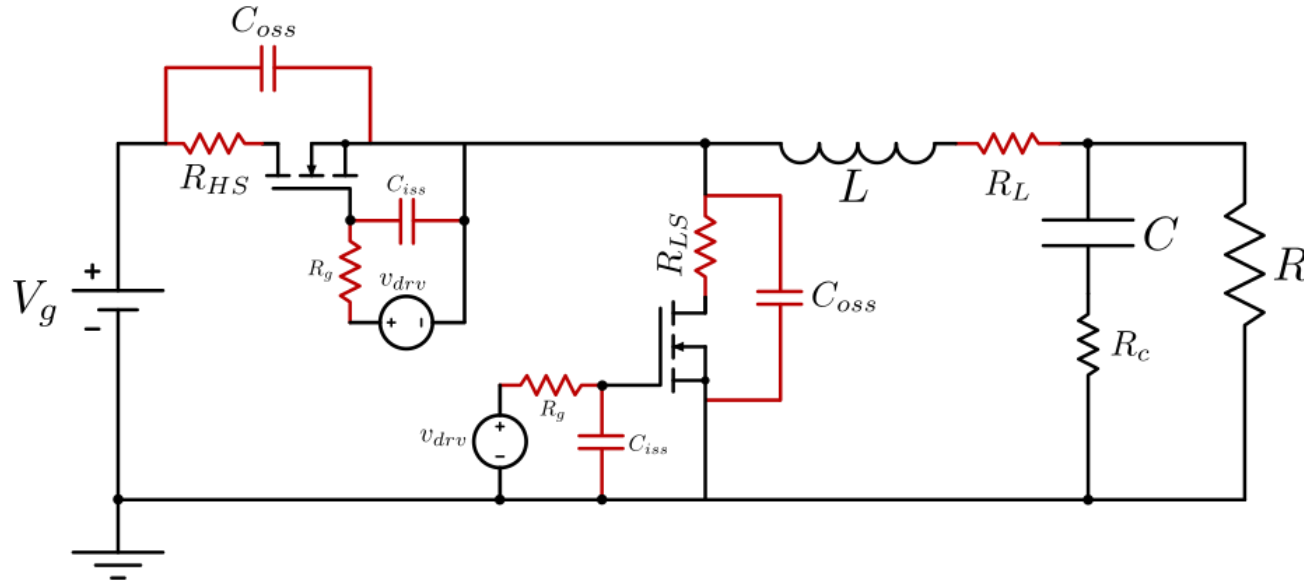
The simplest hard-switched buck converter

Elements in red burn power, reducing the efficiency

Challenges – An Intuitive Power Loss Analysis

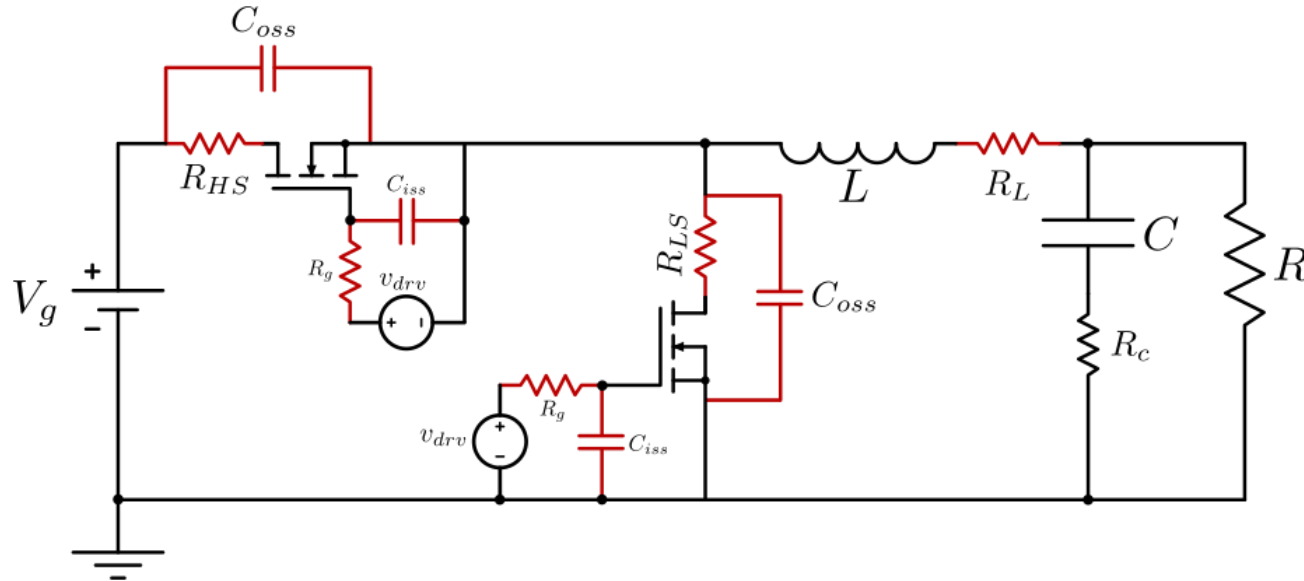Let consider the simple RC network, where C is charge by a generic source.

$$v_R = i_R\, R$$

$$P_R = \frac{v_R^2}{R} = i_R^2\, R$$

$$i_C = C\frac{dv_C}{dt}$$

$$E_C = \frac{CV_C^2}{2}$$

We want to find $v_s(t)$ or $i_s(t)$ that maximize and minimize the power loss in R.

$$\min(P_R) \;\Rightarrow\; i_S \equiv const. \;\Rightarrow\; P_R = I_{RMS(R)}^2 R$$

$$\max(P_R) \;\Rightarrow\; v_S \equiv const. \;\Rightarrow\; E_R = \frac{CV_C^2}{2}$$

Challenges – **An Intuitive Power Loss Analysis**

- Every time the HS switch is turn on, $\frac{C_{oss}V_g^2}{2}$ energy is lost
- Every time a switch is turn on and off, $C_{iss}V_{drv}^2$ energy is lost

Every switching period

- Duty cycle $D = \frac{1}{48} = 0.021$ means at 10 MHz an on-time of 2.1ns.
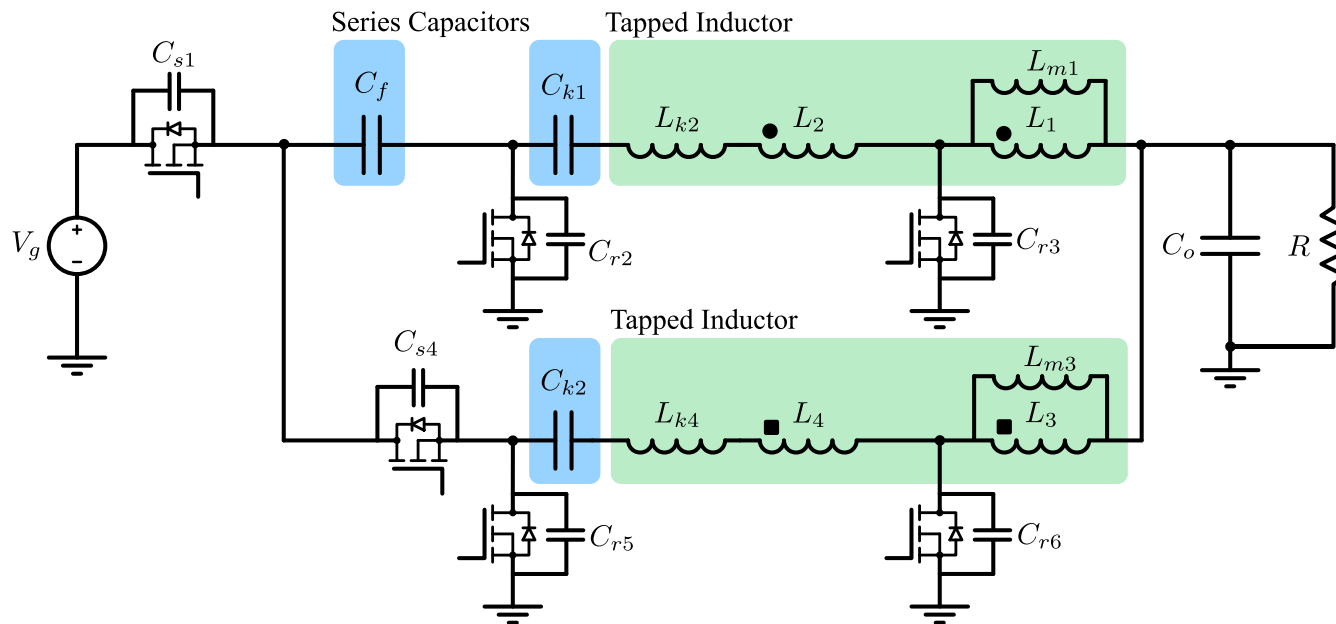- State of the Art GaN driver has minimum on-time between 5ns to 10ns.

With V_g = 12V
$P_{oss} \sim 350$ mW
$P_G \sim 130$ mW

1. **Reduce P$_{oss}$**
2. **Reduce P$_g$**
3. **Increase duty cycle**

Power Stage [1]

- Inductances L_k act as current source that can charge/discharge the output capacitance.

- The switch capacitor and tapped inductor extend the duty cycle.

- We have two more transistors that add gate charge losses and series resistance.

- Ck1 and Ck2 also adds series resistance.

[1] K. I. Hwu, et. Al., "An Expandable Two-Phase Interleaved Ultrahigh Step-Down Converter With Automatic Current Balance," 2017
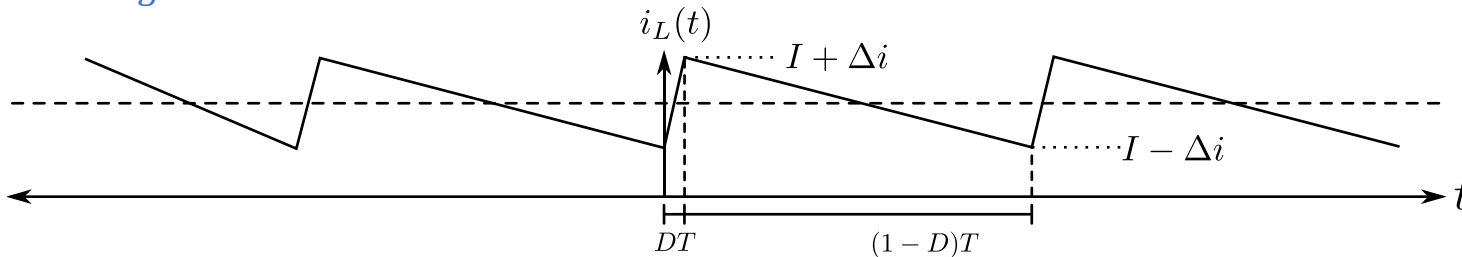
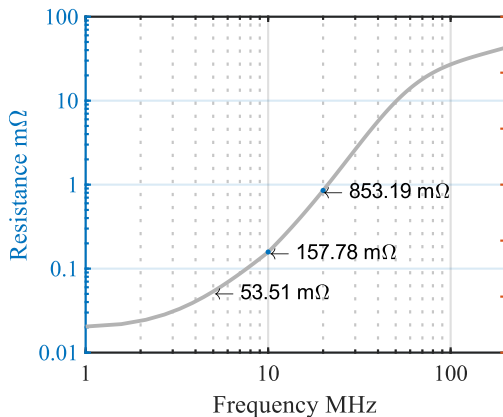# Challenges – An Intuitive Power Loss Analysis
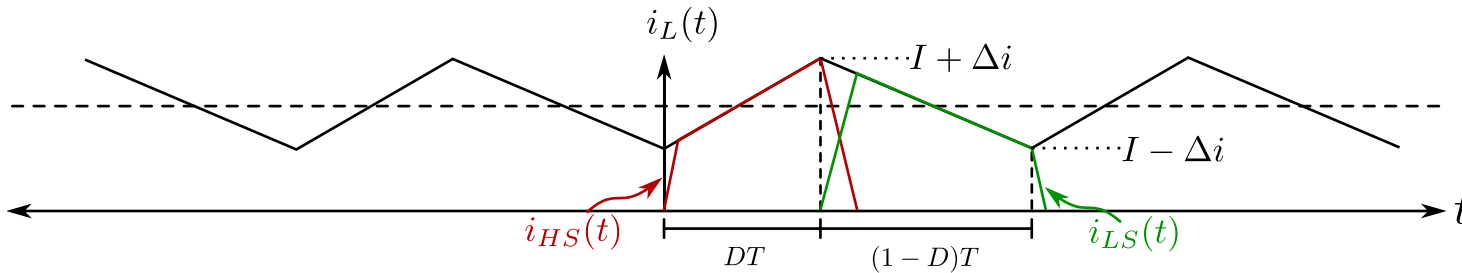
Generalized inductor current ripple

$$D = \frac{V_{out} + I(R_L + R_{LS})}{V_g - I(R_{HS} - R_{LS})} \approx 2.2\%$$

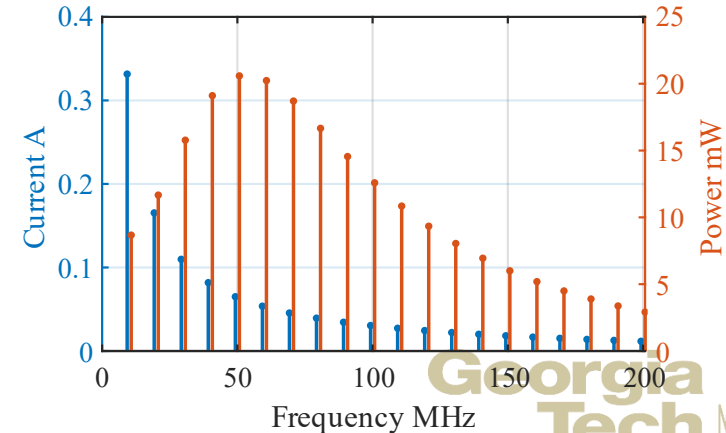But in a 48V to 1V converter the duty cycle is only D = 2.2%

The current ripple look like a ramp
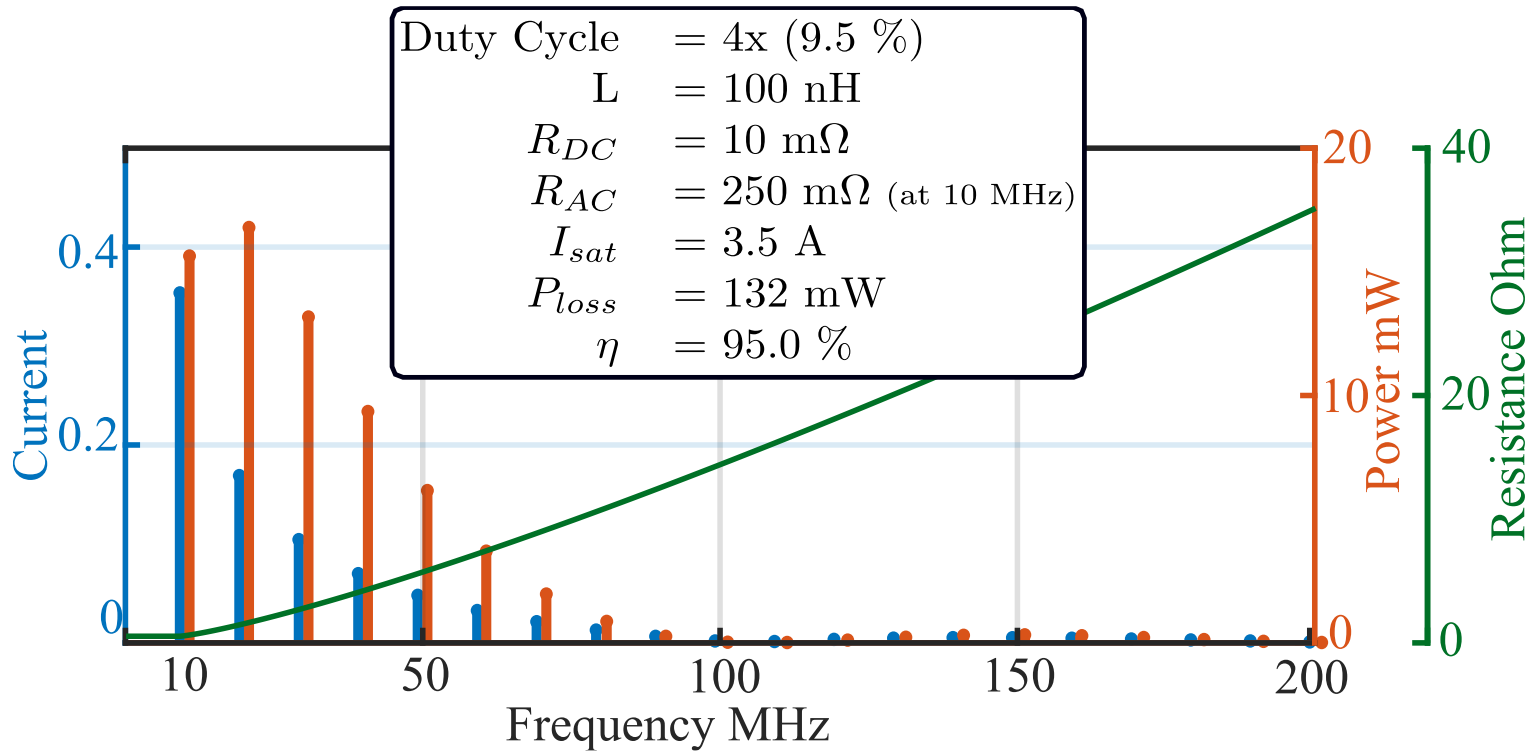

Each current harmonic contribute to the power loss

At 10MHz we can expect harmonic up to 1/2.2ns = 208 MHz

853.19 mΩ

157.78 mΩ

53.51 mΩ

Challenges – Inductor

New
Work

The previous analysis allows us to determine the minimum inductor parameters to achieve 95% of inductor efficiency

$$
\begin{aligned}
\text{Duty Cycle} &= 4\text{x} \ (9.5\ \%) \\
L &= 100\ \text{nH} \\
R_{DC} &= 10\ \text{m}\Omega \\
R_{AC} &= 250\ \text{m}\Omega \ \text{(at 10 MHz)} \\
I_{sat} &= 3.5\ \text{A} \\
P_{loss} &= 132\ \text{mW} \\
\eta &= 95.0\ \%
\end{aligned}
$$

Intel IVR Package Inductor [1]:   140Mhz, L=3.17nH, R_{DC}=12mΩ, R_{AC}=102.1mΩ,   2.5A
Ferric IVR Chip Inductor [2]:   100Mhz, L=10nH, R_{DC}=112mΩ, R_{AC}=348mΩ,   0.75A

[1] William J. Lambert, *et.al.*, Intel FIVR, TCPMT 2016
[2] Ferric Technology, APEC 2017

Power Stage and Inductor Co-design

New Work

Targets
- Efficiency > 90%
  - Inductor efficiency > 95%
  - Power stage efficiency > 95%
- V_{in} = 48, V_{out} = 1V
- I_{out} = 2.5A
- F_{sw} = 10 MHz

Power Stage
- Duty cycle
- Conduction losses
- Switching losses
- ZVS or soft-switching

Inductor
- Duty cycle
- Embedded structure
- Conduction losses (R_{DC})
- AC losses (R_{AC})
- Saturation current

Inductor and Power Stage Co-Design

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Proposed Inductor

To enable next generation IVR, we need an inductor than can

- Match the power stage duty cycle
- Be used as single inductor
- Be used as coupled or tapped inductor
- Be embedded in the package substrate
- Be compatible with multi-phase converters
- Have ultra-low losses
- Have high inductance density
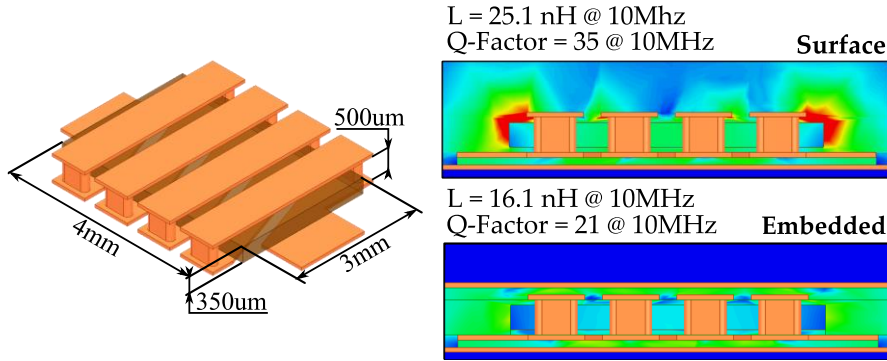- Have close magnetic path
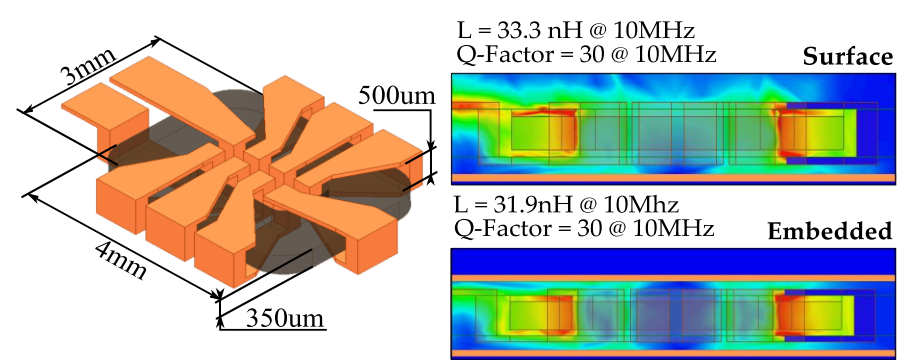
Proposed Inductor Structure

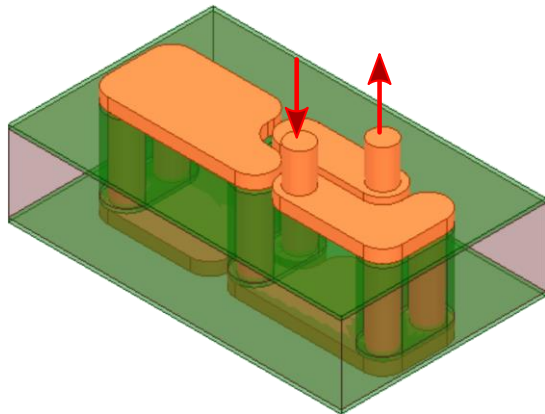Invention Disclosure GTRC ID#8341 submitted on 11/05/2019

New Work

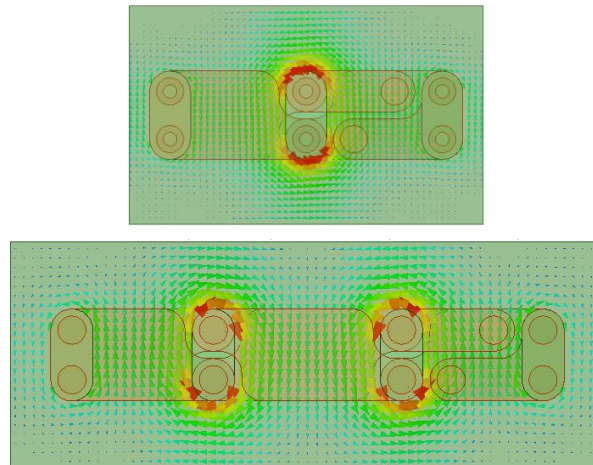**Open magnetic loop inductors can lose more than 35% of inductance when are embedded [5]**

L = 25.1 nH @ 10Mhz
Q-Factor = 35 @ 10MHz
Surface

500um

4mm

3mm

350um

L = 16.1 nH @ 10MHz
Q-Factor = 21 @ 10MHz
Embedded

Closed magnetic inductors are almost not affected by near conduction planes [5]

3mm

4mm

350um

500um

L = 33.3 nH @ 10MHz
Q-Factor = 30 @ 10MHz
Surface

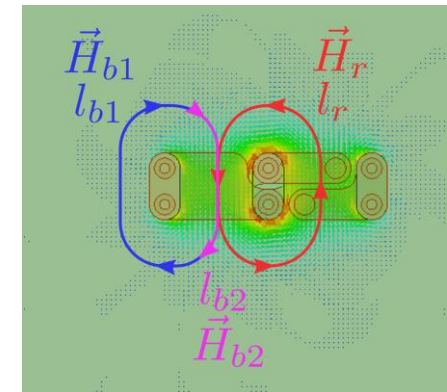L = 31.9nH @ 10Mhz
Q-Factor = 30 @ 10MHz
Embedded

A via is the simplest structure that has a close magnetic path.

The inductor cell present a toroidal field distribution.

It also has an enclose field distribution, confined to the cell.

$\vec{H}_{b1}$
l_{b1}

$\vec{H}_r$
l_r

l_{b2}
$\vec{H}_{b2}$

$$H_{b1} \approx 0$$

$$H_{b2} \approx H_r$$

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[5] Claudio Alvarez, *et.al.*, "Open and Closed Loop Inductors for High-Efficiency System-on-Package Integrated Voltage Regulators", ECTC 2019
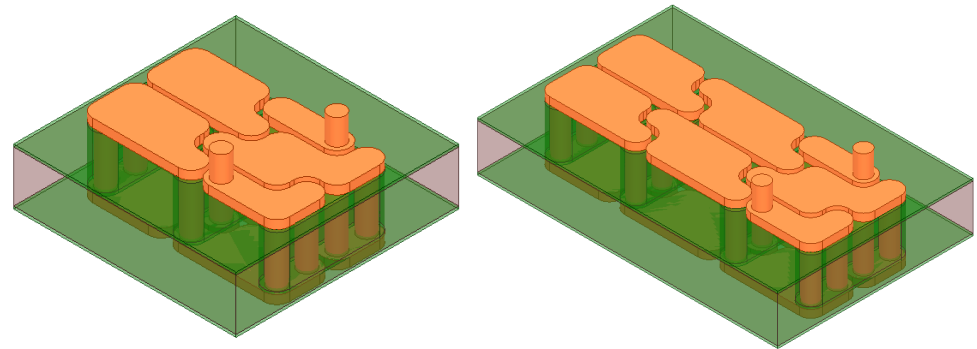
Proposed Inductor Structure

Invention Disclosure GTRC ID#8341
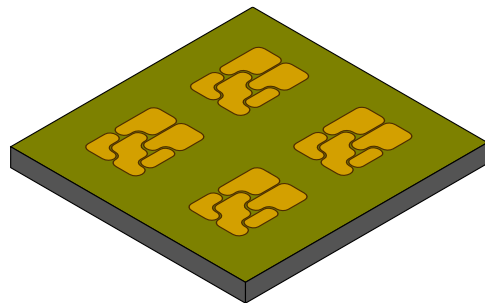submitted on 11/05/2019

New Work

Increase the self inductance
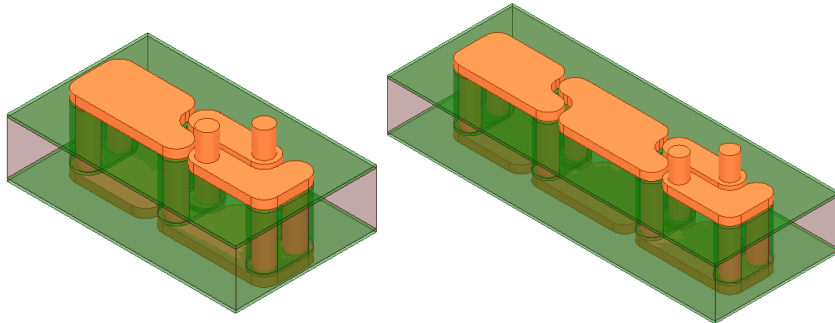
Increase both the self and mutual inductance

Several inductors can be built on the same magnetic sheet substrate.

Tap inductors can be easily obtained with coupling ratio greater than 0.90
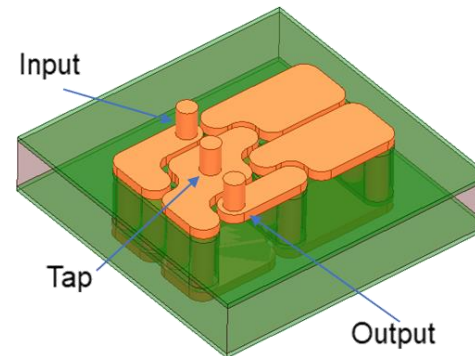
Proposed Inductor Structure

Invention Disclosure GTRC ID#8341
submitted on 11/05/2019

New
Work

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PACKAGING RESEARCH CENTER

SRC
JUMP

Required Magnetic Material
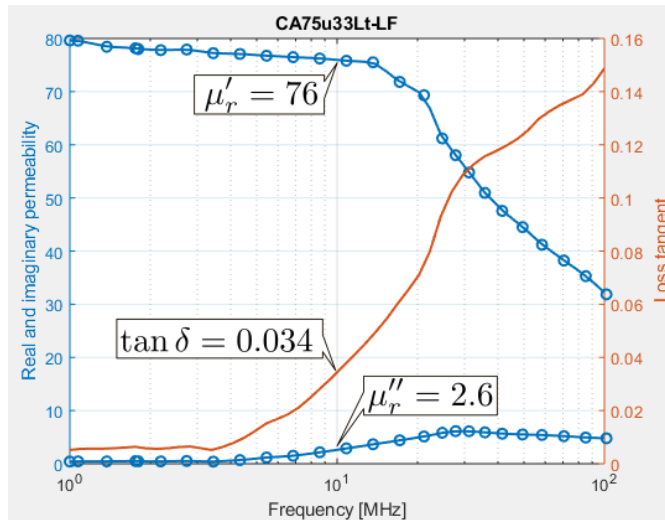
1.8 x 2.3 x 0.5 mm
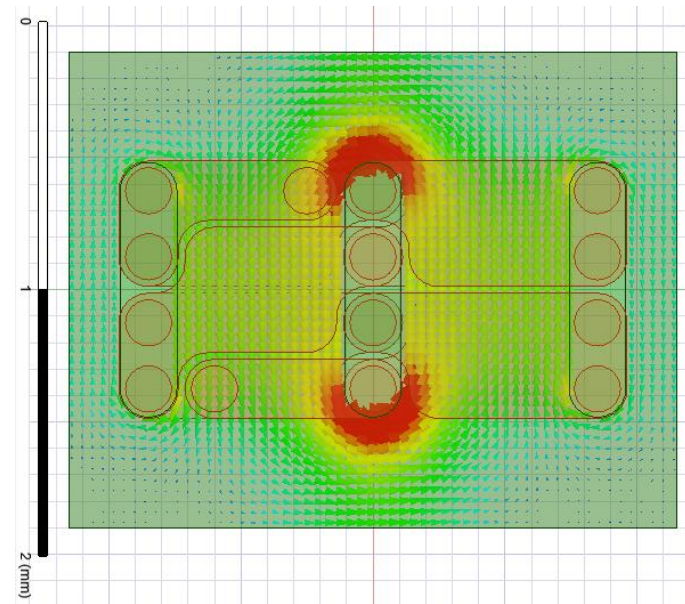
I_{DC} [A]	2.5
L [nH]	117
L_{den} [nH/mm^3]	53
R_{DC} [mΩ]	9.3
R_{AC} [mΩ]	297

Duty cycle [%]	9.5
Output power [mW]	2500
DC Losses [mW]	58.1
AC Losses [mW]	39.3
Inductor Efficiency [%]	96%

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Fabrication Process

New Work

The process is divided in four major steps
1. Mechanical laser drilling *(steps 1 to 4)*
2. Electroless seed copper layer *(step 5)*
3. Lithography *(steps 6 to 8)*
4. Copper electroplating *(steps 9 and 10)*

The entire process is handled in the Packaging Research Center (PRC) at Georgia Tech.

1. Magnetic sheet substrate
300 um

2. Laser drill slot with a fempto-laser

3. Laminate the polymer and fill the slots.

4. Laser drill the vias in slots

5. Deposit an electroless layer of copper

6. Laminate a negative photoresist

7. Place a positive mask and expose to UV light

8. Remove the photoresist that was not exposed.

9. Electroplate with thick copper

10. Etch out the photoresist and seed copper

Schedule

- Toroidal single inductor is already designed
- Fabrication is in process of optimization
- A single inductor based 4-phases buck is in design step
- A Journal paper will be prepared with the analysis results so far

- Next step will be preparing a measurement setup to measure the inductor under DC current bias and with triangular current waveform.
- Next iteration will be the design of a tapped inductor based converter

	2019		2020				2021	
	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
3 – 3D Inductor Design								
3 – 3D Inductor Fabrication								
4 – Inductor Process Optimization								
5 – IVR Dielet Process Dev./Opt.								
6 – IVR Dielet Layout								
7 – Power Stage Design								
8 – Power Stage Model								
10 – PWM and Test Vehicle Layout								
11 – IVR and Board Manufacture								
12 – Measurements								
13 – Meas. To Design Correlation								

done — 3 – 3D Inductor Design
progress — 3 – 3D Inductor Fabrication
progress — 4 – Inductor Process Optimization
progress — 7 – Power Stage Design
progress — 8 – Power Stage Model

Light blue: Inductor design
Dark blue: System design
Light Yellow: Current time window

1st   2nd   Iteration
- Electrical Design
- Packaging Design
- Internship period

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end.

Thanks.