Package-Integrated, Low-ESR, High-Density Capacitors for IVR

Faculty:
- Dr. Himani Sharma
- Prof. M. Swaminathan

Students:
- Grant Spurney
- Mercy Daniel-Aguebor

Industry: Panasonic
- Senshu Takahiro
- Cheng Ping Lin
- Naoki Watanabe

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- ❑ Prior Work
- ❑ Technical Approach
- ❑ Results & Key Accomplishments
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- ❑ Schedule
- ❑ Summary

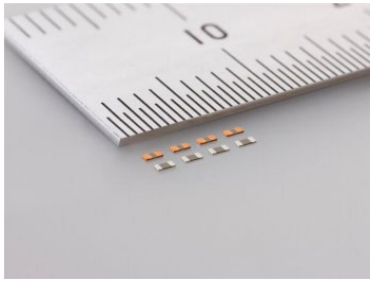
Goals and Objectives

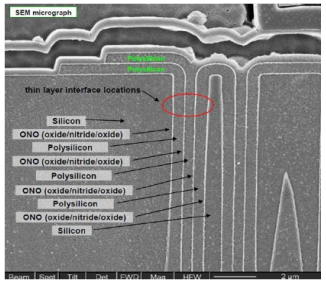
- Demonstrate thin-film tantalum capacitors on silicon with >0.1 µF/mm^2 for 3 V and >20 nF/mm^2 for 48V applications at 10 MHz switching and high current handling

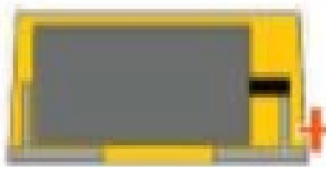
- Specific Objectives & Targets:

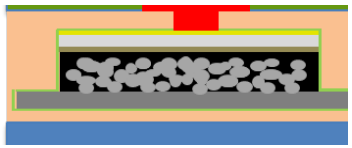
Parameter		Objective	Challenges	Tasks
Capacitance Density at 10 MHz and 100 µm thickness	5 V	**>0.1 µF/mm^2**	Retain high volumetric density and low ESR for high current handling with small form-factor	Substrate-compatible fabrication using high-surface area, printed Ta nanoelectrodes
	48 V	**>20 nF/mm^2**		
ESR and Frequency Stability		**1-10 MHz ESR <50 milliohm**		
3D Package Integration		• **~100 µm interconnects** • **0% added area**	Capacitor compatibility with via formation and build-up processes	Integration directly on silicon using scalable foil transfer
Reliability at High Operating Temperature		**125 ° C**	Conducting polymers are susceptible to thermally induced moisture absorption and oxidation	Develop barrier-material strategy to limit moisture infiltration and pass reliability tests

Prior Art



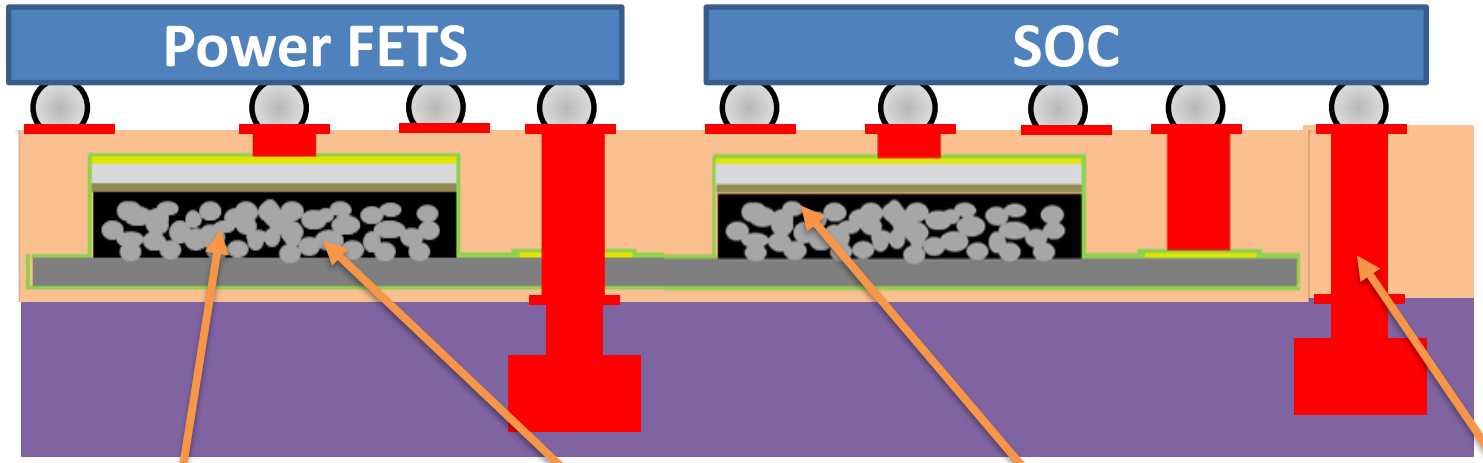






	Murata Thin MLCC	IPDiA Silicon Trench	AVX Ta Chip	GT Ta Thin-film
Volumetric Density	5 µF/mm^3	2 µF/mm^3	10 µF/mm^3	>10 µF/mm^3
Thickness	100 µm	100 µm	600 µm	100 µm
Freq. Stability	10-50 MHz	>100 MHz	300 kHz	1-10 MHz
ESR	~15-50 mΩ	200 mΩ	500 mΩ	~50 mΩ
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	105° C	125° C

Technical Approach



Printed Tantalum Nanoparticles Anode

- High-surface area at thin form-factor
- Scalable to any design need
- Improved frequency stability

Nanoscale Ta_2O_5 Dielectric

- Paraelectric for DC bias and temperature stability
- Amorphous for low leakage current

Conformal Conducting Polymer Cathode

- Low-resistivity and thick coating for low ESR
- Self-healing for low leakage current

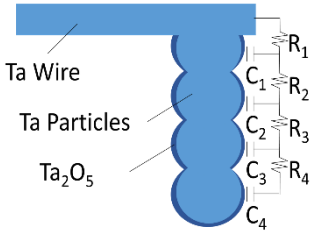
Foil-transfer integration

- Thin-film lamination
- Ultra-short copper interconnections for reduced impedance
- Low-cost, panel-scale, 3D approach

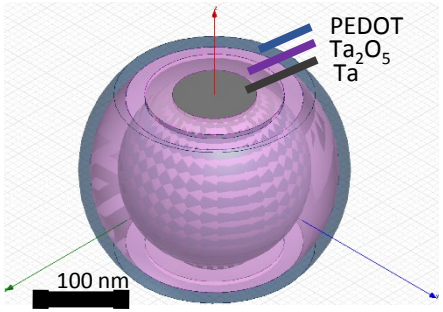
Research Tasks

Task 1: Capacitor Design

Design electrode microstructure for high-density, improved impedance characteristics, and frequency stability



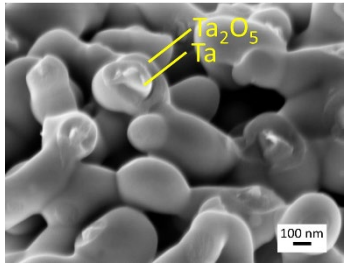
Ta capacitor equivalent circuit



Simplified FEM model of capacitor nanoparticle

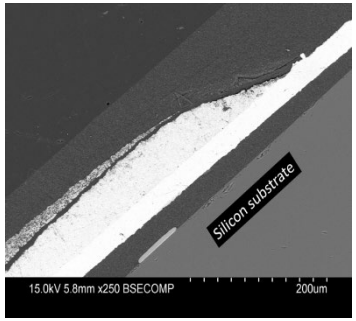
Task 2: Capacitor Fabrication & Integration

Develop process for capacitor materials formation



Sintered and anodized Ta-Ta_2O_5 nanoparticles

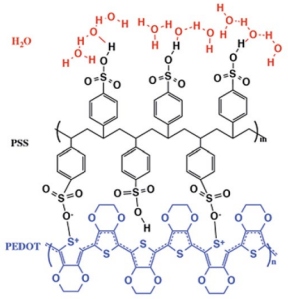
Demonstrate performance of embedded capacitors meeting design objectives



Embedded Ta thin-film capacitor

Task 3: Capacitor Reliability Evaluation

Develop material system strategy to limit diffusion of moisture into capacitor structure at high temperatures



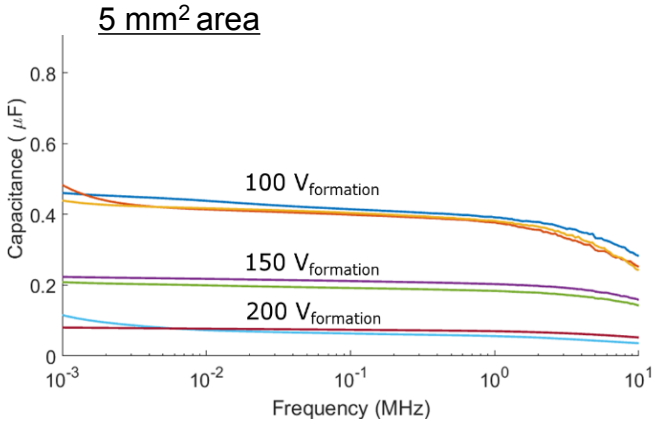
Moisture absorption in PEDOT:PSS cathode material

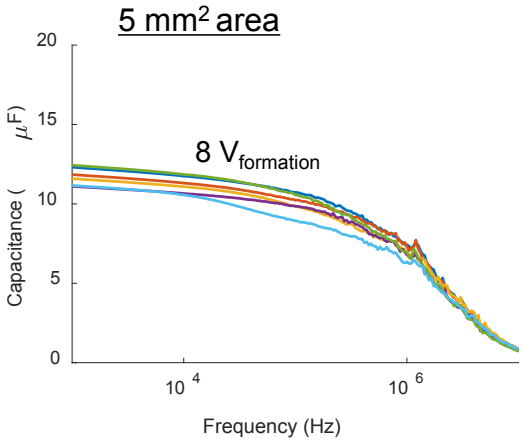
Demonstrate reliability of the capacitors using accelerated stress testing

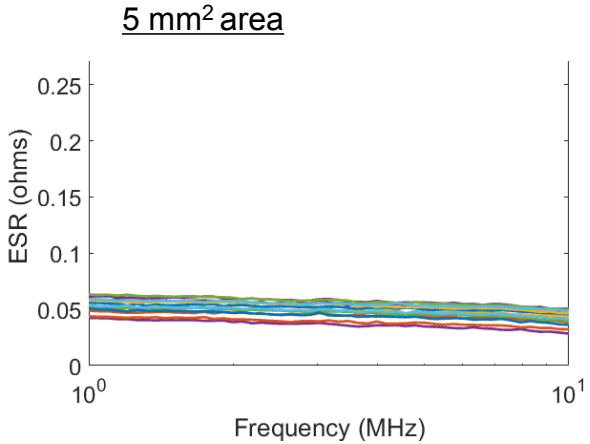
HAST chamber

Prior Work

- Capacitors fabricated and tested meeting designs objectives:

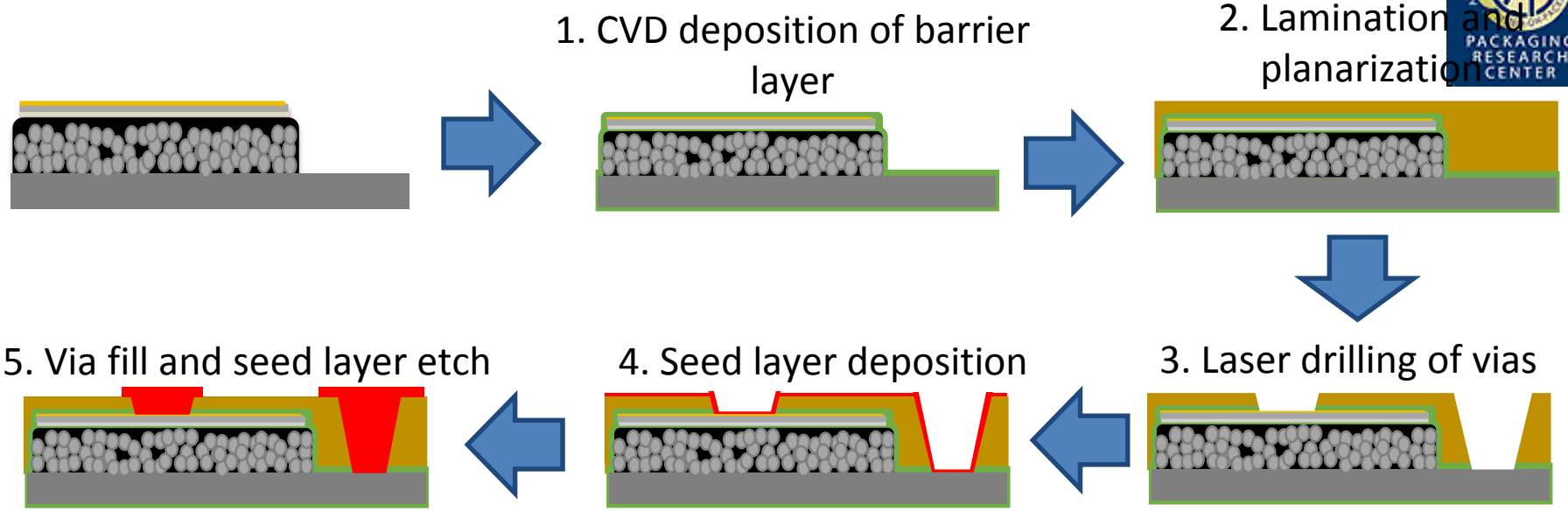


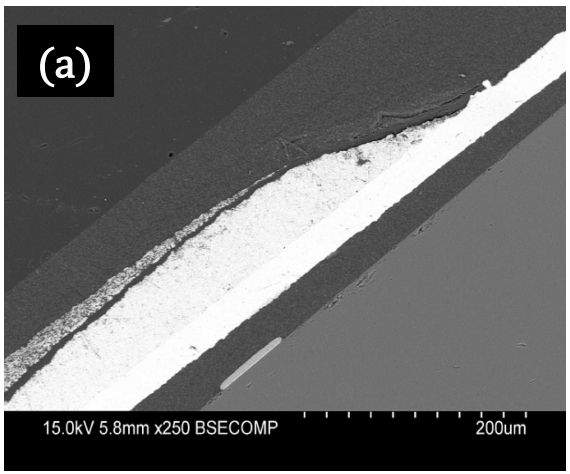


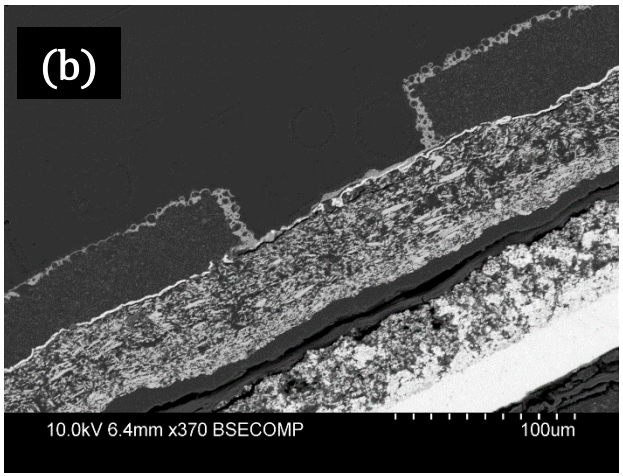


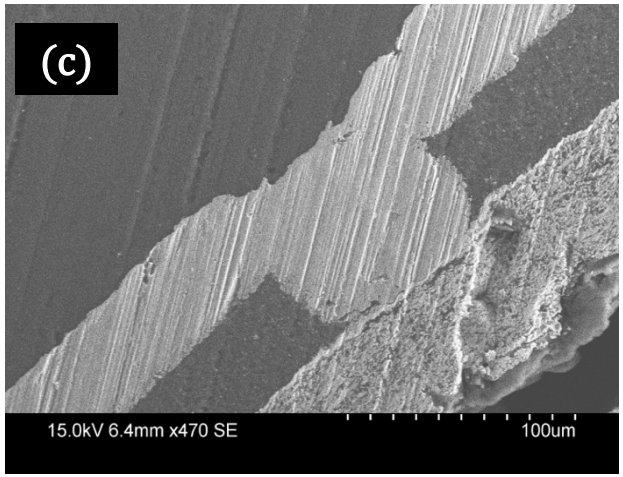
- Foil-transfer lamination process optimized for successful capacitor integration on organic, silicon, or glass substrate
- Preliminary reliability testing results showed use of thin-film diffusion barriers improve high-temperature lifetime of capacitors

Integration Process Overview



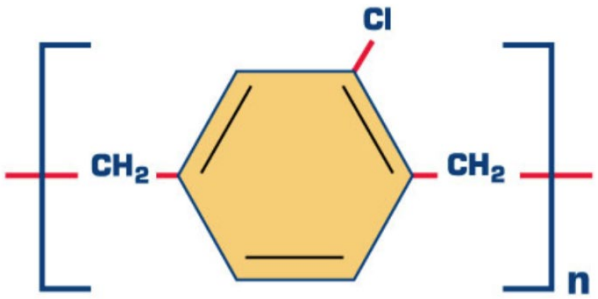




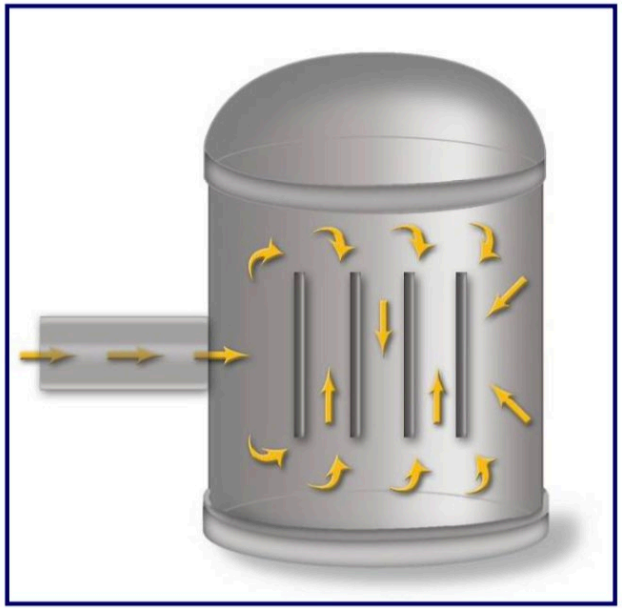


(a) Thin-film Ta capacitor laminated and planarized on silicon (b) Thin-film capacitor after laser drilling of via and electroless copper deposition (c) Partially filled copper via contacting Au/silver paste cathode layers

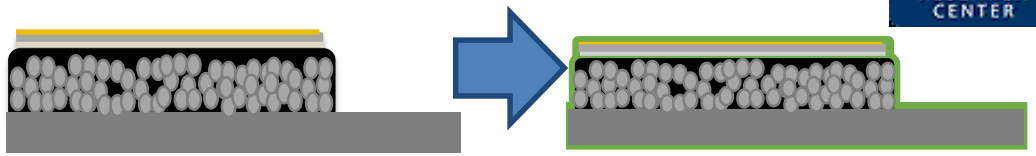
Barrier Layer Deposition of Parylene C using CVD



Linear structure & aromatically stabilized Cl in Parylene C structure → High crystallinity



*Low-temperature CVD **of Parylene***
→ Good conformality and strong adhesion

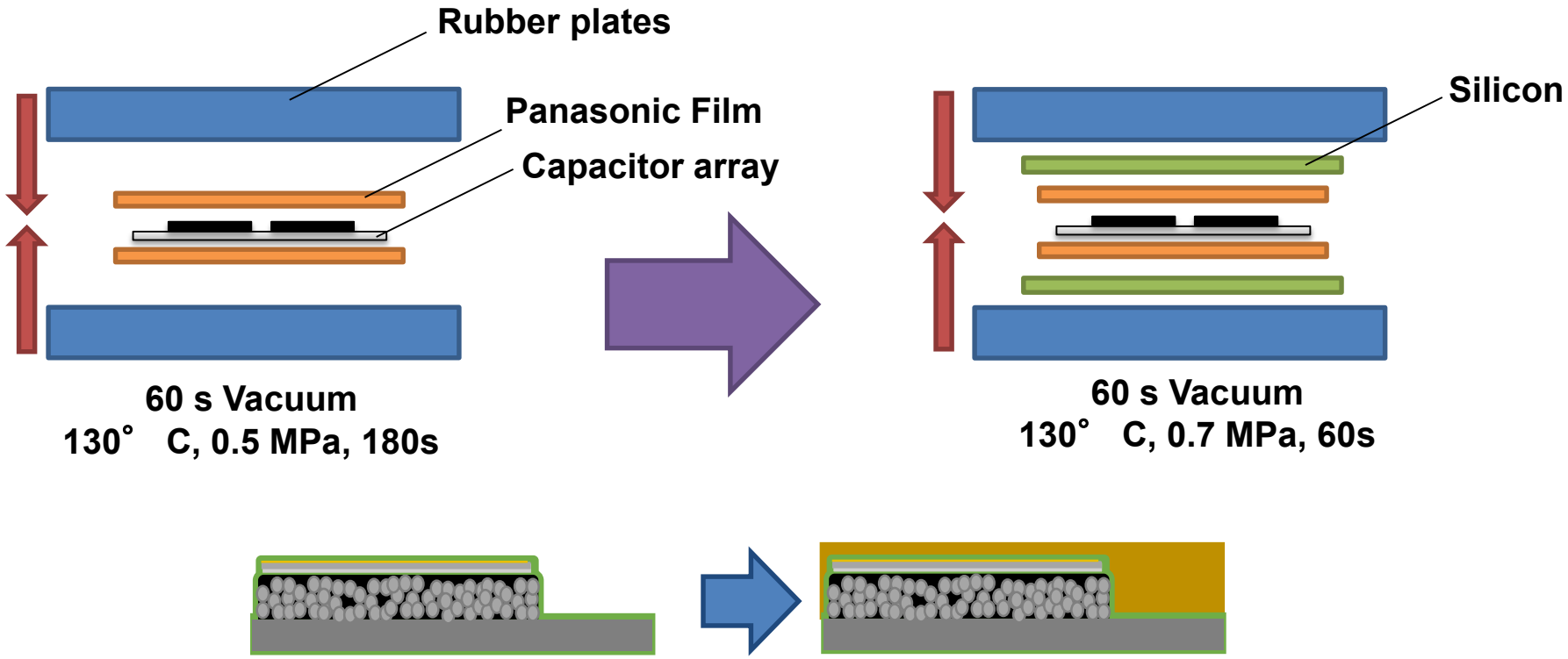


2 μm of Parylene C deposited on all samples

Previously showed thicker Parylene layer can be used to increase number of capacitors passing 85° C/85% relative humidity/3.3 V bias HAST for 335 hours

Parylene C Thickness	500 nm	700 nm	1000 nm
Total Passing Rate	14 %	57 %	75 %

Lamination with Panasonic Film

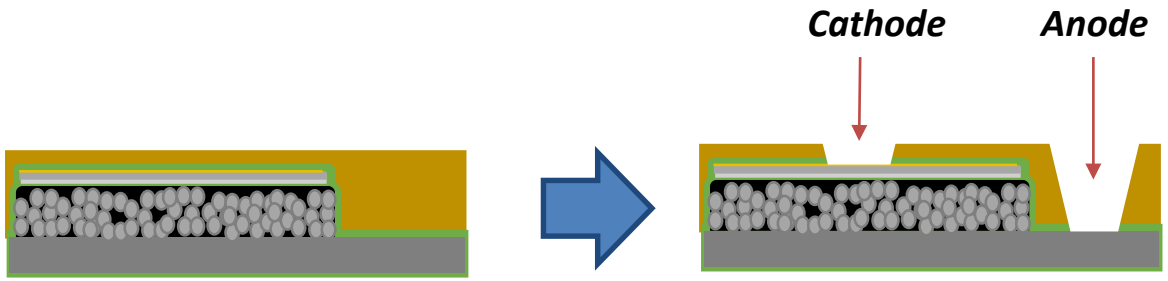


Laser Drilling of Vias using UV Laser

Drilling conditions:

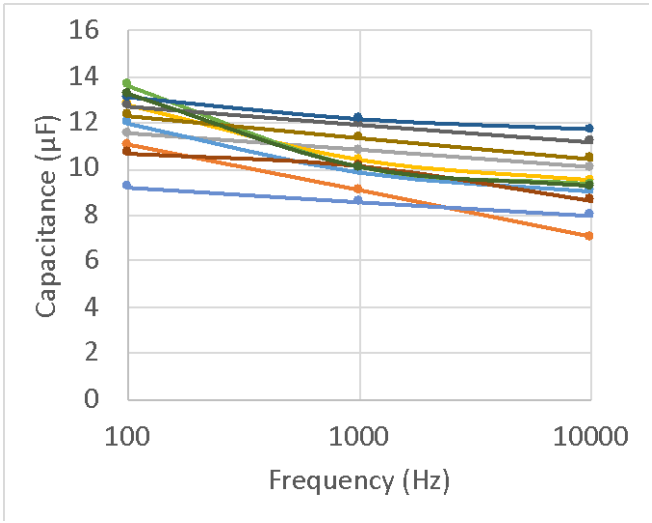
Film:		XV2106FG	XV2105FG	XV2103FG
Power	Anode	12 W	5 W	4.5 W
	Cathode	5 W	5 W	4 W
Repetitions	Anode	100	100	100
	Cathode	100	100	100
Via Opening Diameter	Anode	155 µm	155 µm	155 µm
	Cathode	155 µm	155 µm	155 µm

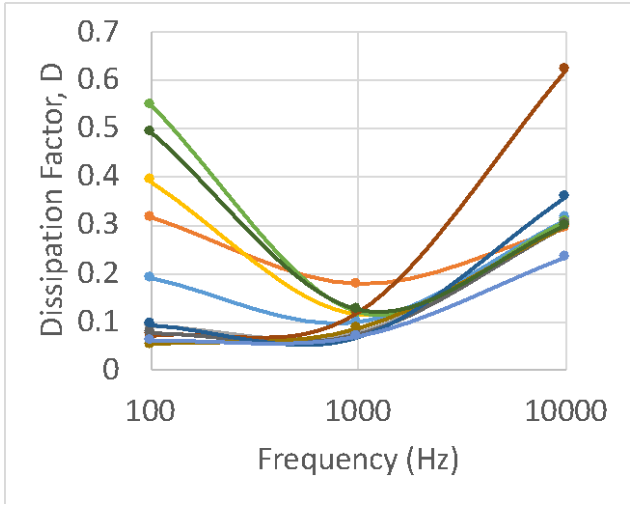
- **Followed by 12 min desmear in Permanganate etch to remove leftover polymer debris**



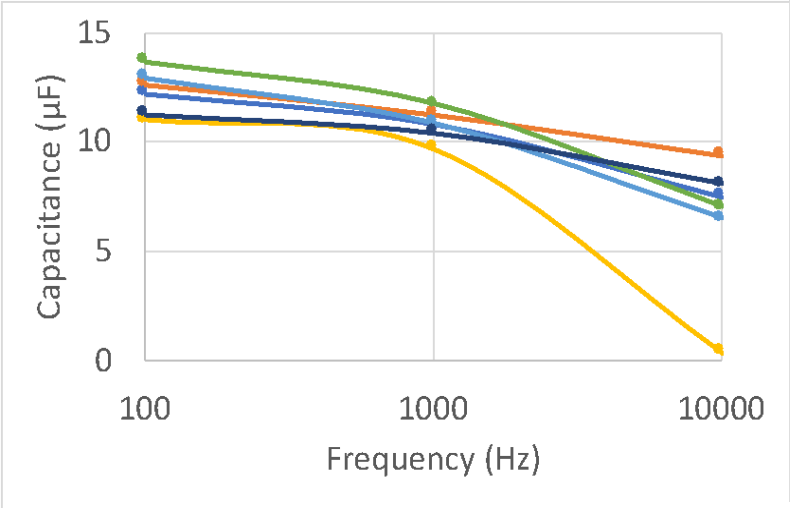
Electrical Characterization of Integrated Capacitors

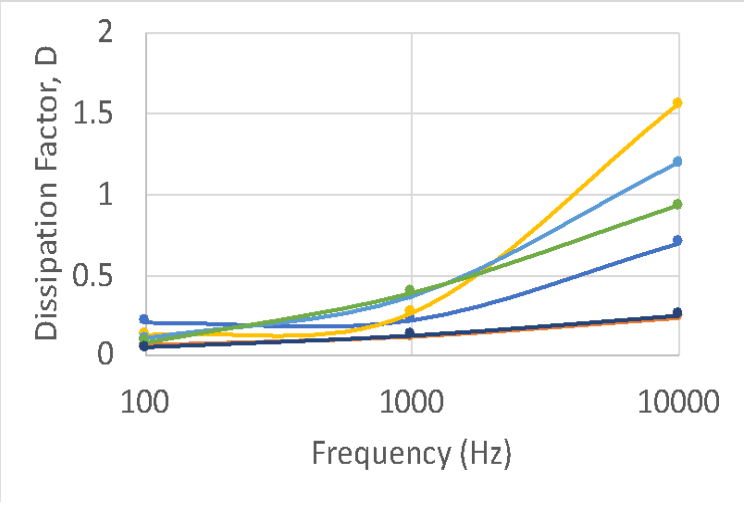
- Measurements of capacitors embedded in XV2103FG film



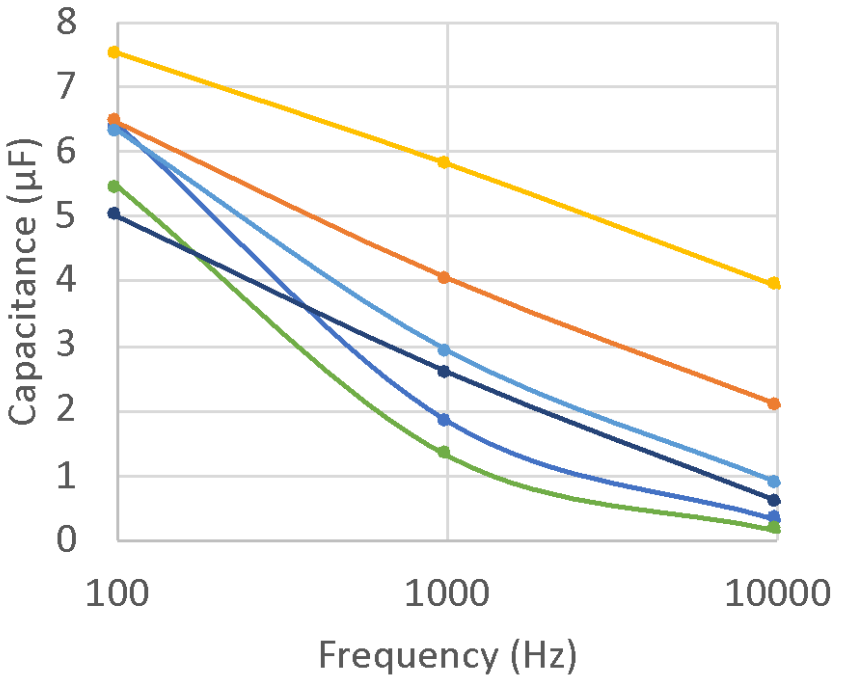


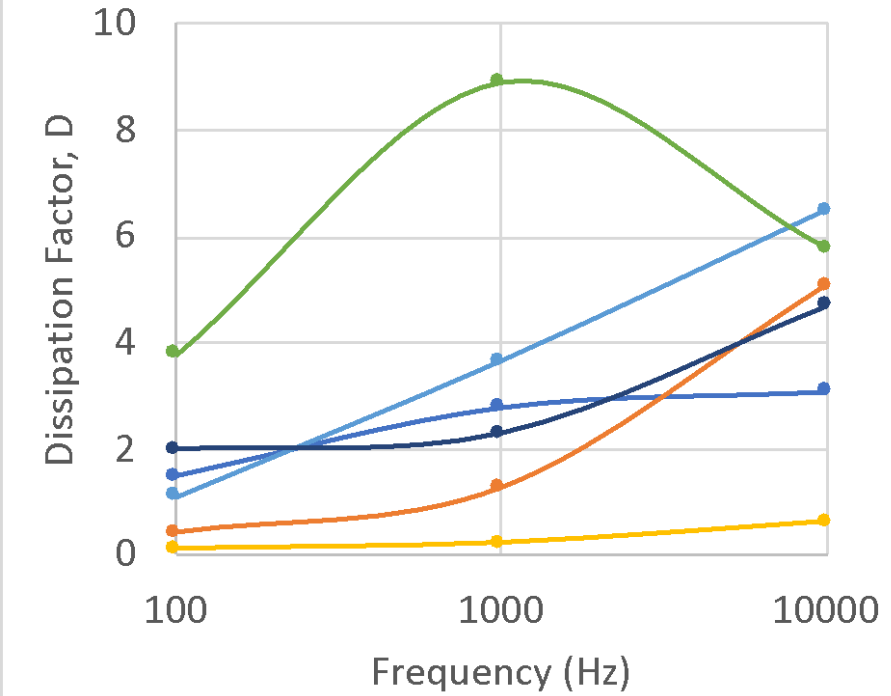
- Measurements of capacitors embedded in XV2105FG film





HAST Results





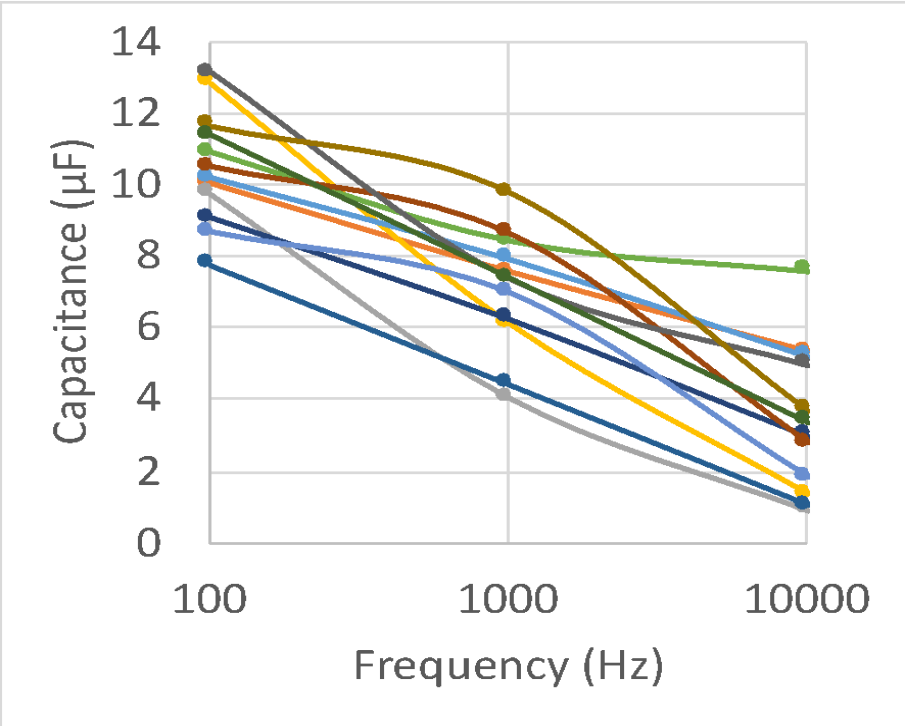
- **Measurements of capacitors embedded in XV2105FG film**

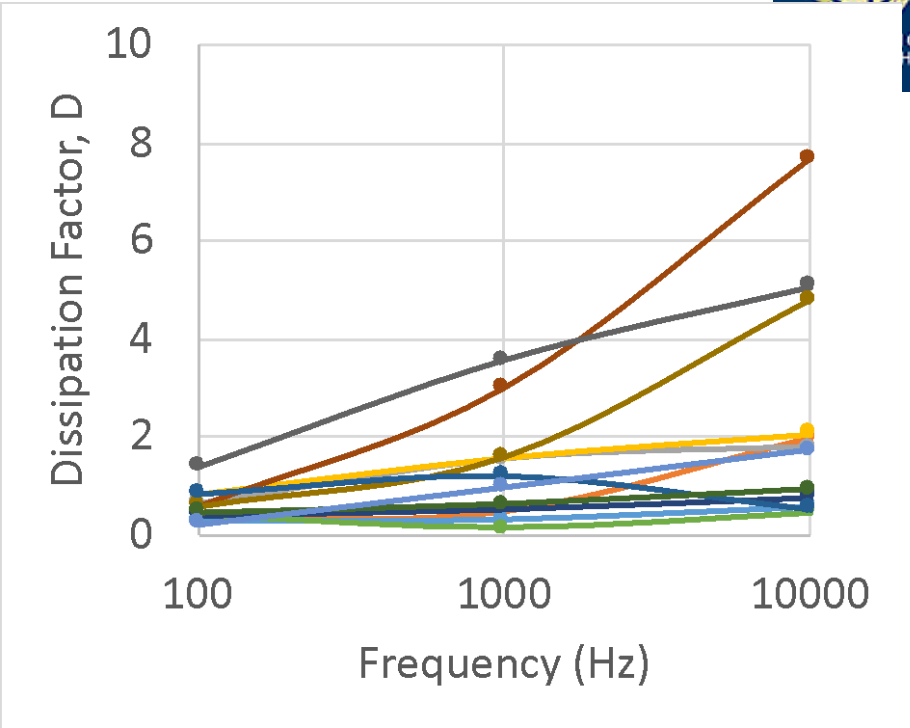
Average capacitance (1 kHz): 4.07 µF → (-63.8 %)

Average Dissipation Factor (100 Hz): 1.38 → (+228%)

Average ESR (100 kHz): 8.42 Ω → (x 5.32)

HAST Results





- **Measurements of capacitors embedded in XV2103FG film**

Average capacitance (1 kHz): 10.27 µF → (-3.85 %)

Average Dissipation Factor (100 Hz): 0.934 → (+93.4 %)

Average ESR (100 kHz): 13.91 Ω → (x 26.2)

Summary

- Capacitors successfully passed 85/85 HAST for 335 hours
  - Some capacitors show ability to pass 125/85 HAST for 96 hours
  - Least amount of degradation observed using XV2103FG film
- XV2103FG film showed the most promising results
  - Very little decrease in capacitance and increase in dissipation factor
  - Thinner form factor
- ESR increased dramatically in most cases, but unclear how much of this can be attributed to the increase in resistance coming from the solder versus the capacitors themselves
- Next phase of project will focus on capacitor integration with magnetic substrate to provide on-package LC power conversion network