SiC-Based Power Electronics for EV Drive: Introduction

Faculties: Dr. Vanessa Smet
Prof. Antonia Antoniou
Prof. C.P. Wong
Prof. Yogendra Joshi
Prof. Madhavan Swaminathan
Prof. Deepak Divan, Prasad Kandula
(Center for Distributed Energy)

Students: Haksun Lee
Michael Mauger
Kashyap Mohan
Jiaxiong Li
Justin Broughton
Ryan Wong
Hakki Torun

Industry Collaborators: Bosch, Toyota

Outline

- Background & Technical Challenges
- Objectives
- Technical Approach
- Prior Work
- Results & Key Accomplishments
- Comparison with Prior Art
- Summary

Background & Technical Challenges

Key Application: Electric Vehicles

- Modern EV usage

- Trend to increase integration density: in-wheel

Source: Protean (~50kW/0.5L)

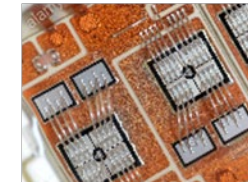
→ **Transition to SiC devices is key to reaching required power densities (2X)**

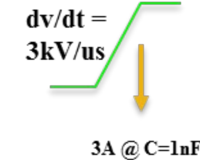
Challenges with SiC: Why Packaging is More Critical

- Increased switching speeds: aggravated effect of package parasitics
  - Parasitic L: increased di/dt with SiC
  - Parasitic C: increased dv/dt and common mode noise

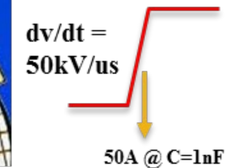
$$i_{CM} = C_{parasitic} \frac{dv}{dt}$$

Si-IGBTs





SiC-MOSFETs



- Shrinking of die size and increased power ratings: increased thermal density
  - Hot spot mitigation
  - Transient thermal performance more critical
  - While SiC devices can sustain higher T_{jmax}, the package will be exposed to increased operating temperatures as well → reliability?

→ **Packaging is today the limiting factor in realizing the promises of SiC**

Objectives

- **Develop and demonstrate advanced packaging solutions for SiC-based power electronics with:**
  - Modular design: flexibility in power level
  - Miniaturization: module size ~25% vs. Si → 100kW/0.5L for in-wheel inverters
    - ✓ High-frequency switching
    - ✓ Increased functional density with heterogeneous integration (e.g. cooling)
  - Minimized package parasitics ($L<5nH$, C_{AG},$C_{BG}<0.1pF$), increased dv/dt capability → wirebond-less
  - High operating temperatures (junction and coolant?) and improved thermal behavior
  - Fundamental understanding of multiphysics trade-offs

Parameters	Current Packaging Solutions	Our Targets
Breakdown Voltage	10kV	>30kV
Heat Flux	200W/cm^2	1kW/cm^2
Max. Junction Temperature	150-175°C	250°C
Thermal Performance	No thermal transient control	Thermal transient suppression
Reliability	Poor at full device rating	Improved

Technical Approach

ML-Assisted Design & Heterogeneous Functional Integration

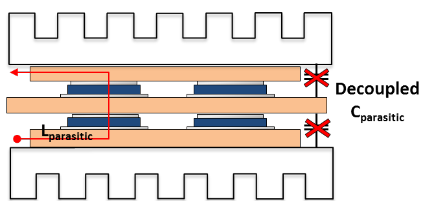
NEW Machine learning (ML) based power module optimization (Bayesian active learning)

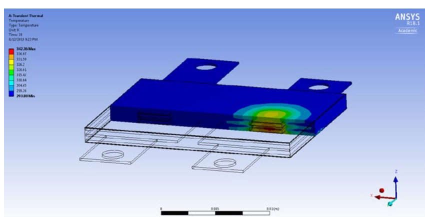
Circuit Topology (Center for Distributed Energy)

Poster by M. Mauger, P. Kandula, D. Divan **NEW**

- *Non-Consortium project (ARPA-E)*
- Soft switching (current switch)

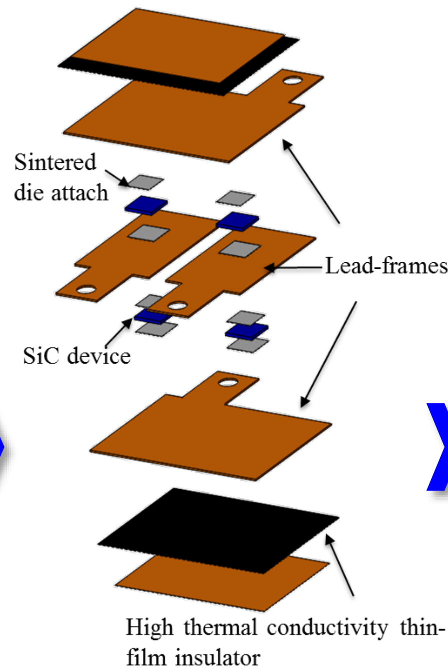
Concept: die stacking





Multiphysics Modeling

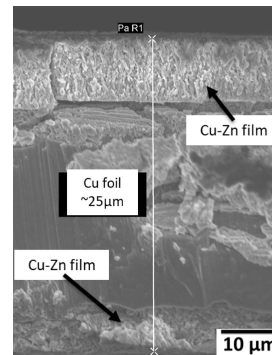
- Electrical, thermal, mechanical

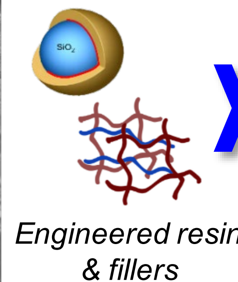


Material Innovations

- High-temperature, HV mold compounds (Prof. C.P. Wong)
- Sintered Cu die-attach (with Prof. A Antoniou)
- **NEW** Low-CTE composite conductors (with Prof. A. Antoniou)

NP-Cu die-attach





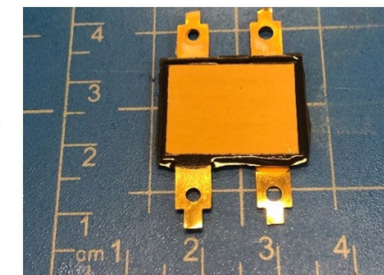
Engineered resin & fillers

3D Stacked Power Cards

Talk by H. Lee

- Die stacking
- Manufacturing
- Testing

From concept to realization: functional bridge rectifier

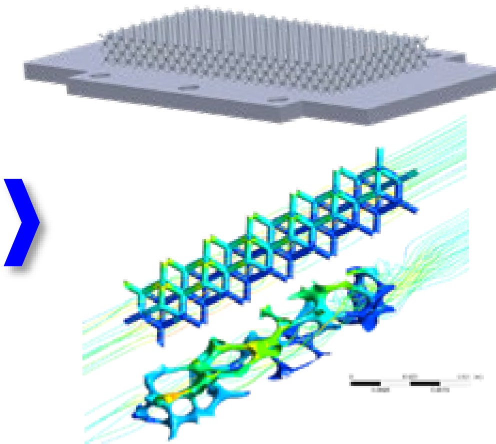


Cooling System

With Prof. Y. Joshi

- Advanced cold plates (2-phase)
- **NEW** Integrated cooling (new project, with Prof. A. Antoniou)

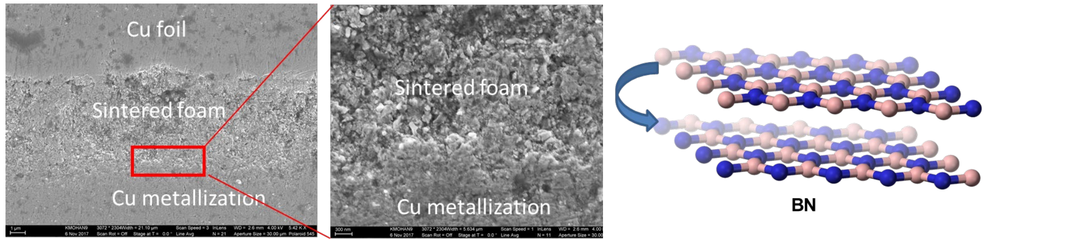
Advanced cold plate with additively manufactured foam



Prior Work: May IAB Recap

Material Developments

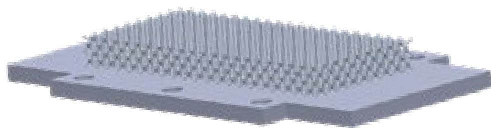
- NP-Cu die-attach insert with compliant Cu foil core (with Prof. A Antoniou)
- Resin / fillers formulation for high-temp. stability & high thermal conductivity (Prof. C.P. Wong)

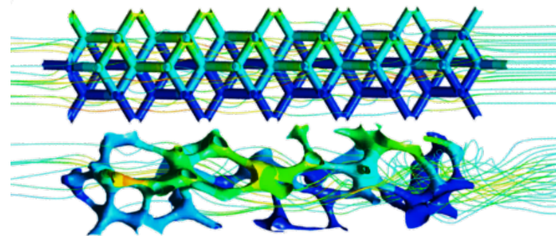


Advanced Cold Plates

Prof. Y. Joshi

- Flow loop setup complete
- Stochastic pore-scale model in agreement with experimental results: additively manufactured foams perform best

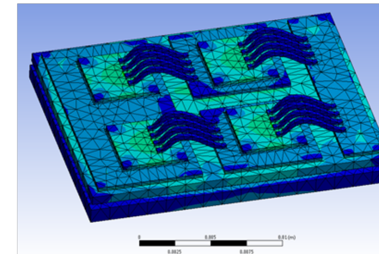


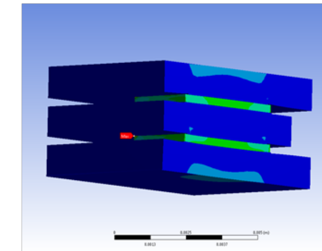


3D Stacked Power Module

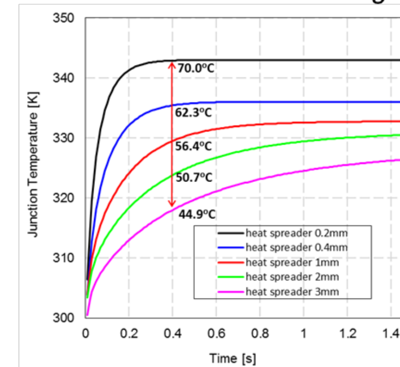
- Thermal modeling: ~5X reduction in junction-to-case Rth vs. conventional module
- Trade-off in Cu thickness for stress management: 200μm
- Unit fabrication process steps established

Conventional power module vs. 3D stacked power module

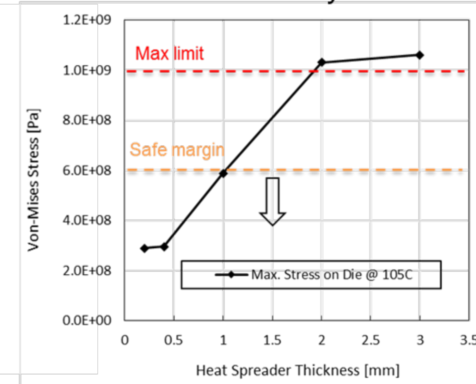




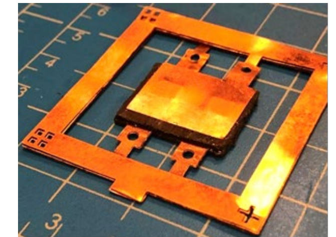
Thermal modeling

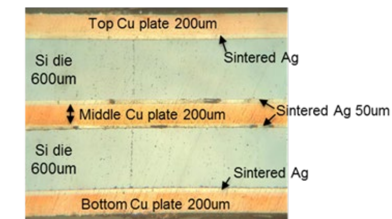


Stress analysis



Mechanical process demonstrator



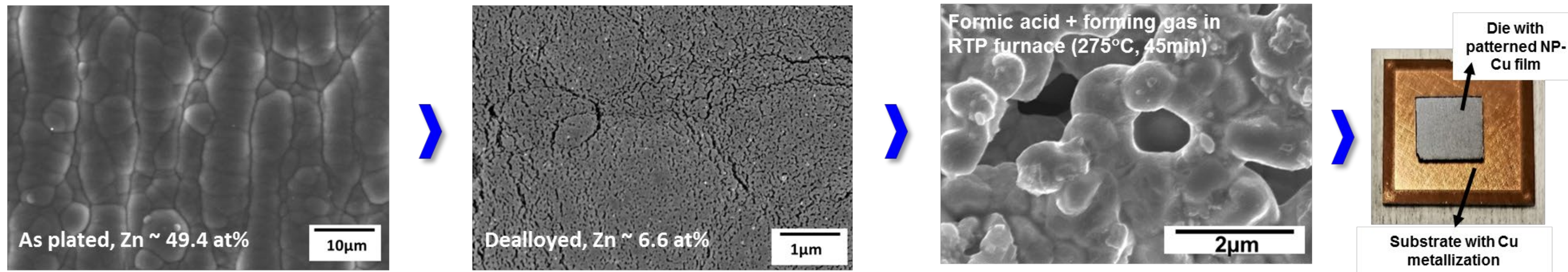


Results & Key Accomplishments: Material Innovations

NP-Cu Die-Attach

Collaboration with Prof. A. Antoniou, On Semiconductor, poster by K. Mohan

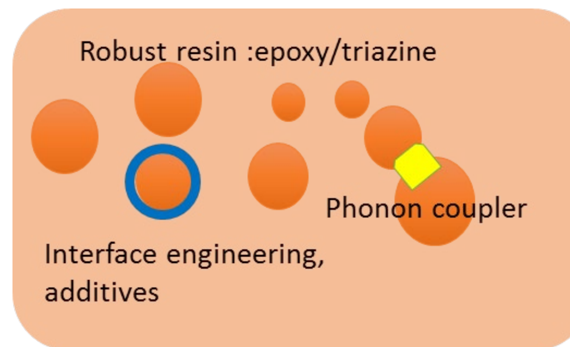
- ❑ Identified promising precursor alloy composition and dealloying parameters for SAP process manufacturability
- ❑ High densification confirmed (in formic acid)
- ❑ Expected to reach shear strength values of 40-50MPa



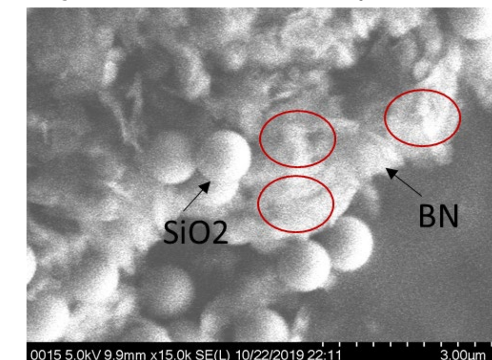
Mold Compounds

Prof. C.P. Wong, poster by J. Li

- ❑ Demonstration of high Tg cyanate ester/ epoxy (CE/EP) copolymer (>250°C)
- ❑ Progress in synthesis of BN-coated SiO_2 for high thermal epoxy composite
- ❑ Progress in formulation of resin systems for high BDV



High Thermal BN/SiO2 Hybrid Filler

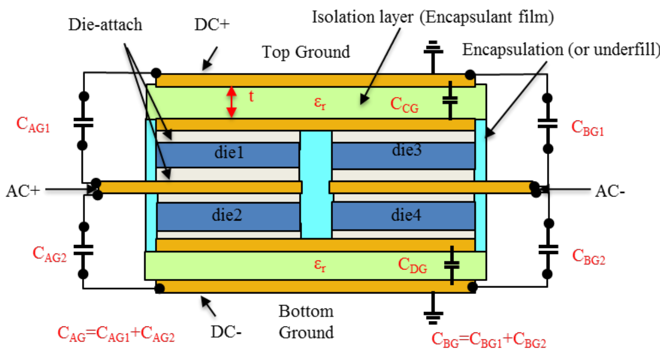


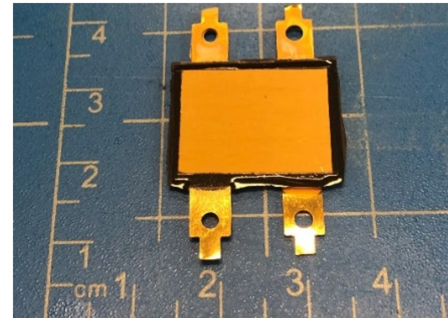
Results & Key Accomplishments: Power Module Integration & Cooling

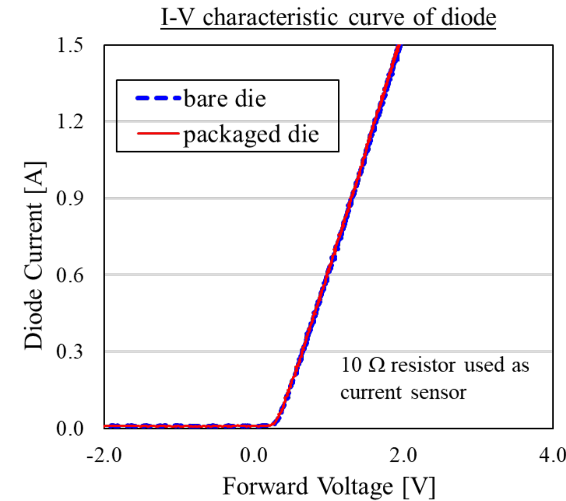
3D Stacked Power Module

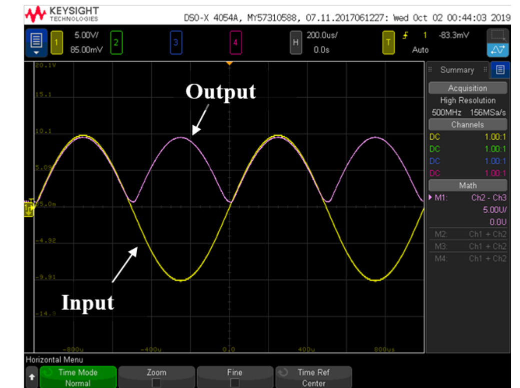
Talk & poster by H. Lee

- Electrical simulation & measurements: significant improvements in package parasitics
- Full bridge rectifier with 200V/15A Si diodes fabricated and tested







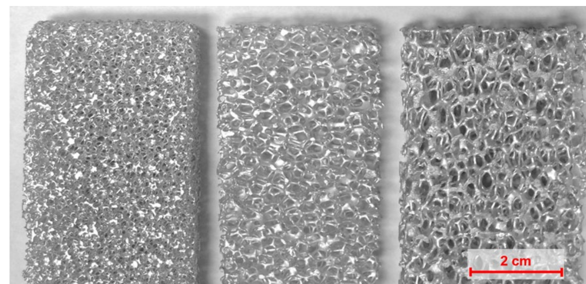


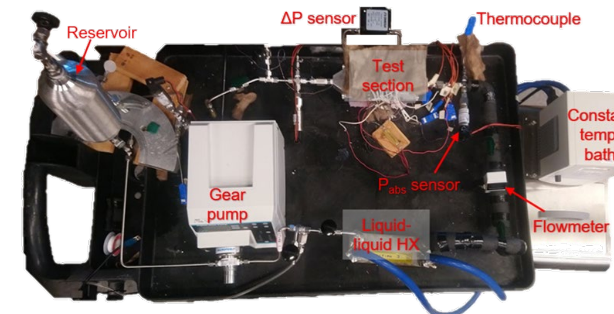
Resistive load (78 kΩ) at the output of rectifier

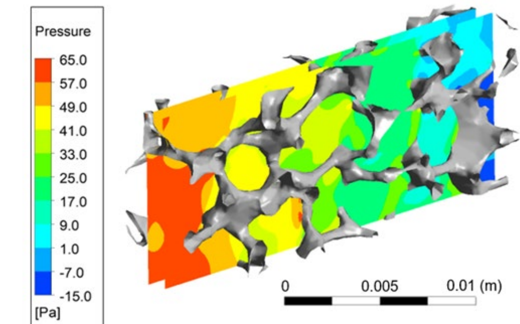
Advanced Cold Plates

Prof. Y. Joshi, poster by J. Broughton

- Dual computational-experimental approach
- Performance comparison between traditional vs. AM foams





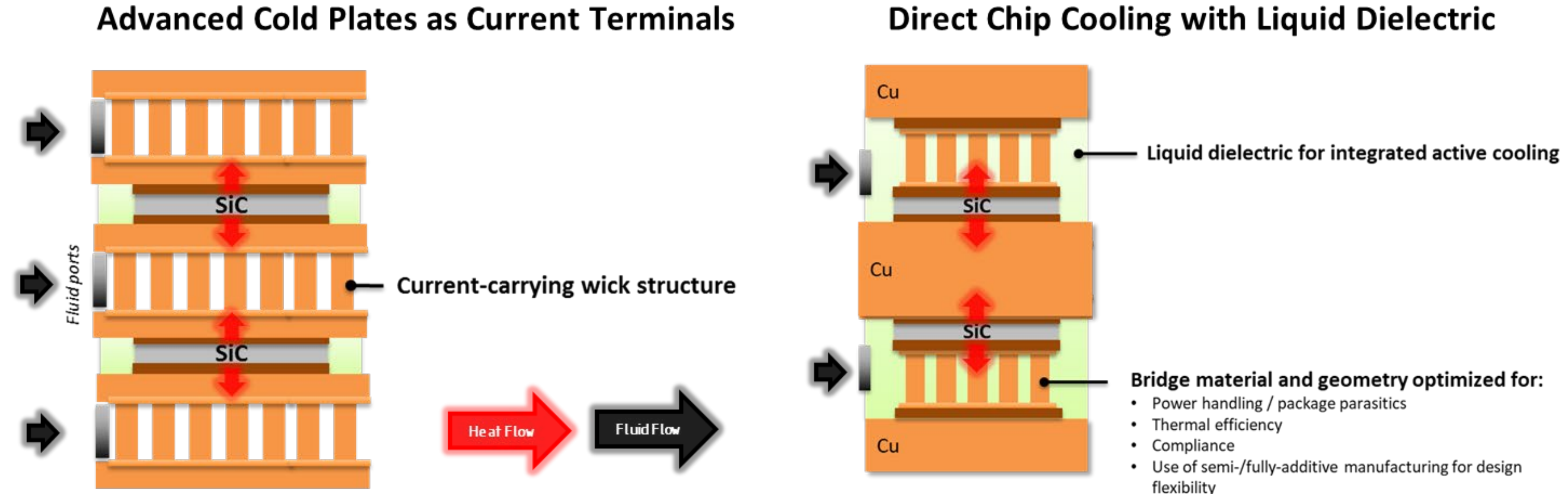


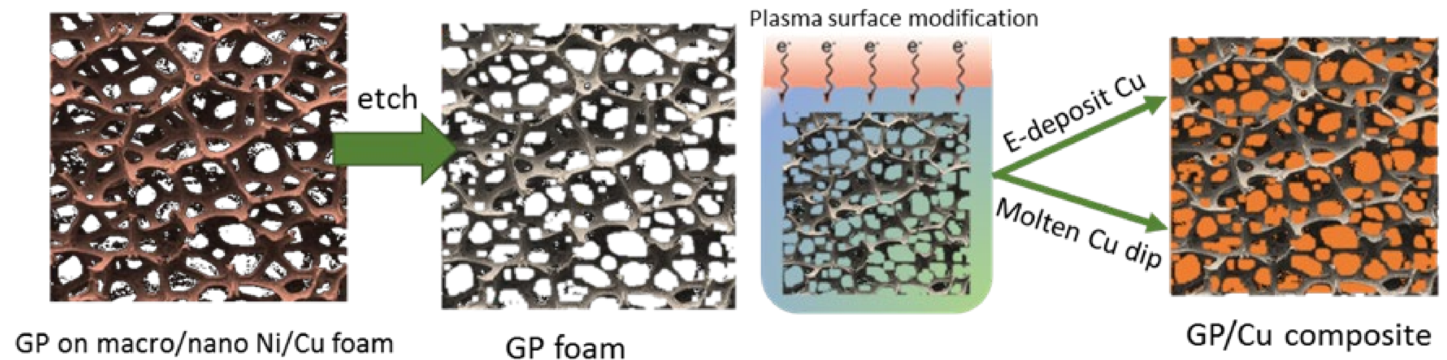
Increasing Functional & Power Density: Integrated Cooling

NEW

In collaboration with Prof. Y. Joshi & Prof. A. Antoniou, Bosch
Poster by R. Wong

- Key concept: bring cooling closer to the heat sources (devices, high current terminals)
- Create hybrid electrical / thermal structures
  - Multiphysics, multiscale modeling
  - Machine-learning assisted design optimization
- Material innovations: use 3D interconnected **Graphene (GP) foams** to create low-CTE / high-conductivity Cu-GP composites

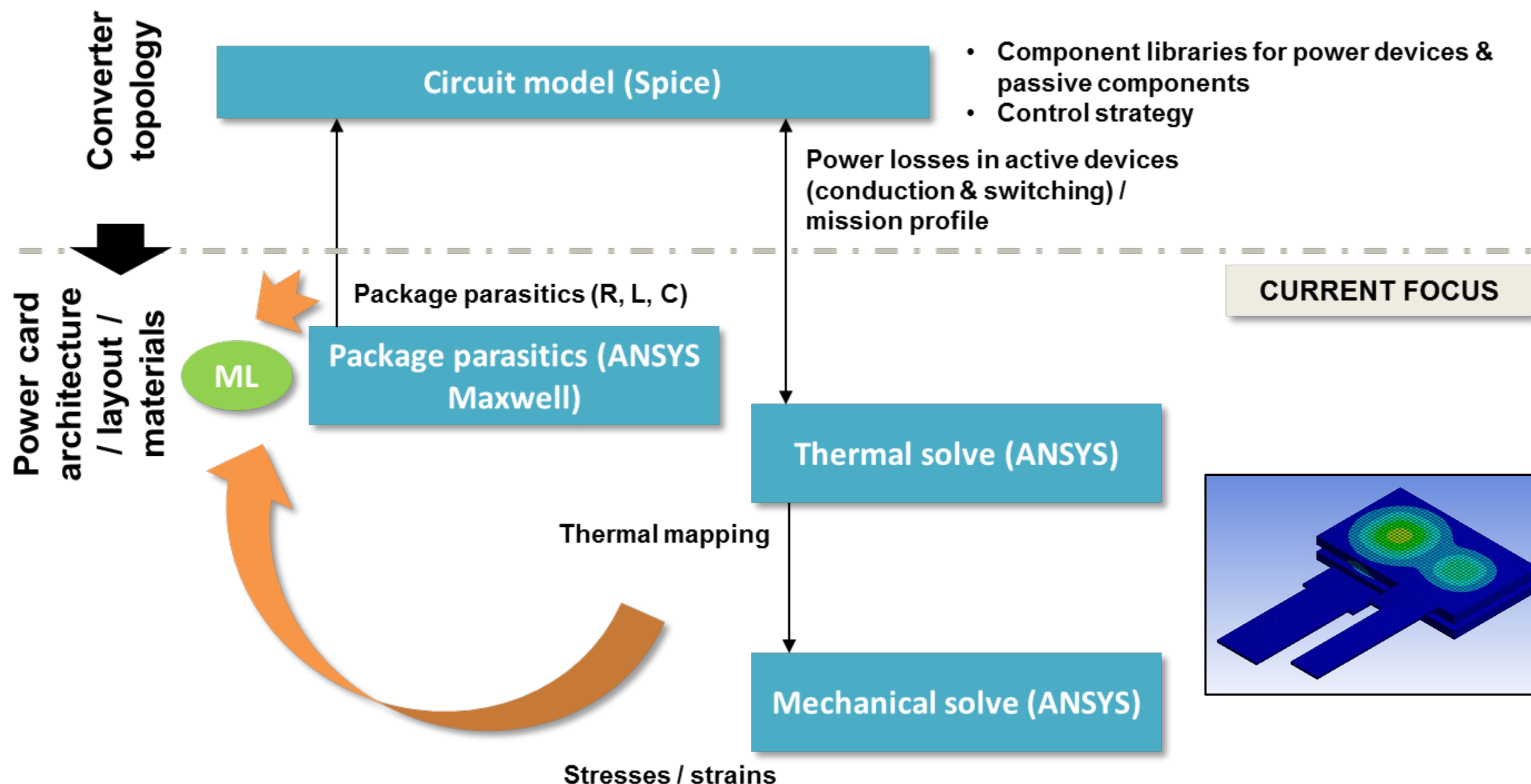


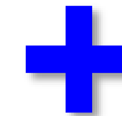


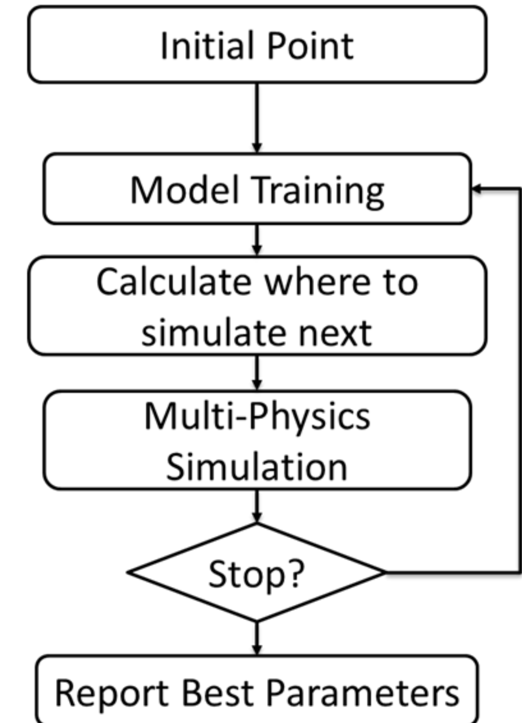
NEW Shaping the Landscape of Future WBG-Based Power Electronics

In collaboration with Prof. M. Swaminathan, Toyota
Talk & poster by H. Torun & R. Wong

- ❑ Combine machine / active learning and multiphysics analysis to optimize, and ultimately generate new, **non-intuitive** SiC-based inverter package architectures
- ❑ Build and characterize prototypes based on ML-assisted design







Comparison with Prior Art

Standard

Courtesy of H. Lee

Denso Bosch Mitsubishi — **Direct Lead Bonding**

Delphi Infineon ORNL — **Double-sided DBC**

Univ. of Arkansas Semikron Schweizer — **Component Integration**

Univ. of Grenoble NCSU ARL — **3D Power Integration**

- Combined benefits from 3D integration, heterogeneous integration & functional integration
- Focus on manufacturability & compatibility with industry-standard processes
- Inclusion of machine learning for multi-objective power module optimization
- Unique potential to go from co-design to prototyping and testing with focused GT team

Summary

- Research program is growing with an ecosystem of expert faculties coming together
- Addressing the transition to SiC from many angles to identify key integration strategies and package architectures, particularly for EVs
- Work is ongoing in parallel with Prof. S.C. Shen on vertical GaN devices (goal is to develop a GaN IGBT) as next roadmap
- Aiming at growing our prototyping and testing capability with more supply chain involvement