Design & Demonstration of 3D Stacked Rectifier Module

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Outline

- Goals & Objectives
- Prior Work
- Technical Approach
- Results & Key Accomplishments
- Comparison with Prior Art
- Schedule
- Summary

Goals and Objectives

- Design, demonstrate and characterize a new class of ultra-low parasitics, 3D SiC power modules with high efficiency, high dv/dt capability, and enhanced thermal management and thermomechanical reliability

<table>
<tr><th></th><th>Parameter</th><th>Target</th><th>Prior Art</th><th>Challenges</th><th>Research Tasks</th></tr>
<tr><td rowspan="2">Electrical</td><td>Parasitic inductance</td><td>-20% reduction *</td><td>5.0 ~ 52 [nH]</td><td rowspan="6">1. Trade-offs in multi-physics design
- High-speed switching
- High thermal density
- High-temp. operation

2. Vertical conduction methods
- Bulky fixtures
- Complex process (ex. via drilling)
- Limited conductor thickness

3. Characterization of 3D module
- Measurement of extremely small L(<nH) and C(<pF)</td><td rowspan="6">1. 3D package design
- Low-parasitics L and C
- Low-thermal resistance
- Enhanced reliability

2. Fabrication & Assembly of lead-frame based compact 3D module
- Materials and process design
- Simple stacking process

3. Characterization of 3D module
- Electrical (L, C, waveforms)
- Thermal resistance
- Reliability performance</td></tr>
<tr><td>Parasitic capacitance</td><td>-100% reduction *</td><td>75 ~ 140 [pF]</td></tr>
<tr><td>Thermal</td><td>Thermal resistance</td><td>-20% reduction *</td><td>0.1 ~ 1.1 [$^oC/W$]</td></tr>
<tr><td rowspan="3">Thermomechanical</td><td>High temperature storage (200^oC)</td><td>1000 hr</td><td>1000 hr</td></tr>
<tr><td>Thermal cycling ($-40^oC/+125^oC$)</td><td>$N_f > 1000$</td><td>$N_f < 1000$</td></tr>
<tr><td>Temperature-Humidity (85^oC/85% RH)</td><td>1000 hr</td><td>1000 hr</td></tr>
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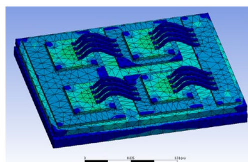
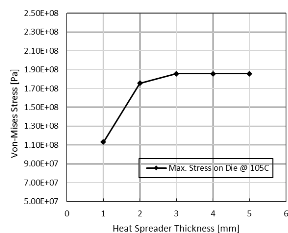
*** Compared to a reference design**

Prior Work

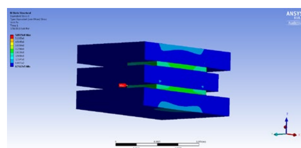
Thermomechanical Analysis and Comparison

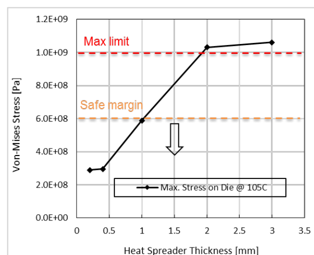
Wire bond module





3D module





Uniform Temperature Elevation @ 105°C (Temperature Cycling Precursor)

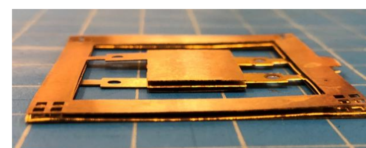
		Wire bond module 5mm	3D module 0.2mm
Die	Maximum Von-Mises Stress [MPa]	186	289 (+55.4% increase)
Die Attach	Maximum Von-Mises Stress [MPa]	43.7	40.9(-6.4% decrease)
	Maximum Plastic Strain	2.96e-2	1.75e-2(-40.8% decrease)

Super Imposed Temperature Distribution @ 100W per die (Power Cycling Precursor)

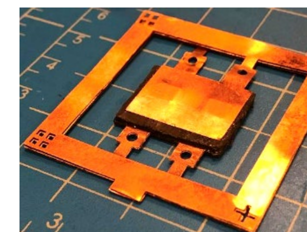
		Wire bond module 5mm	3D module 200um
Die	Maximum Von-Mises Stress [MPa]	160.4	124.6 (-22.1% decrease)
Die Attach	Maximum Von-Mises Stress [MPa]	44.4	28.3 (-36.3% decrease)
	Maximum Plastic Strain	1.95e-2	0.47e-2 (-75.9% decrease)

Unit Process Development & Fabrication

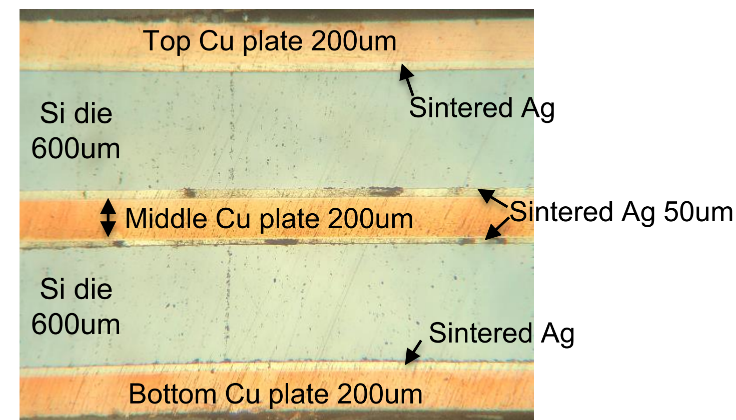
3D stacking process



Molding process



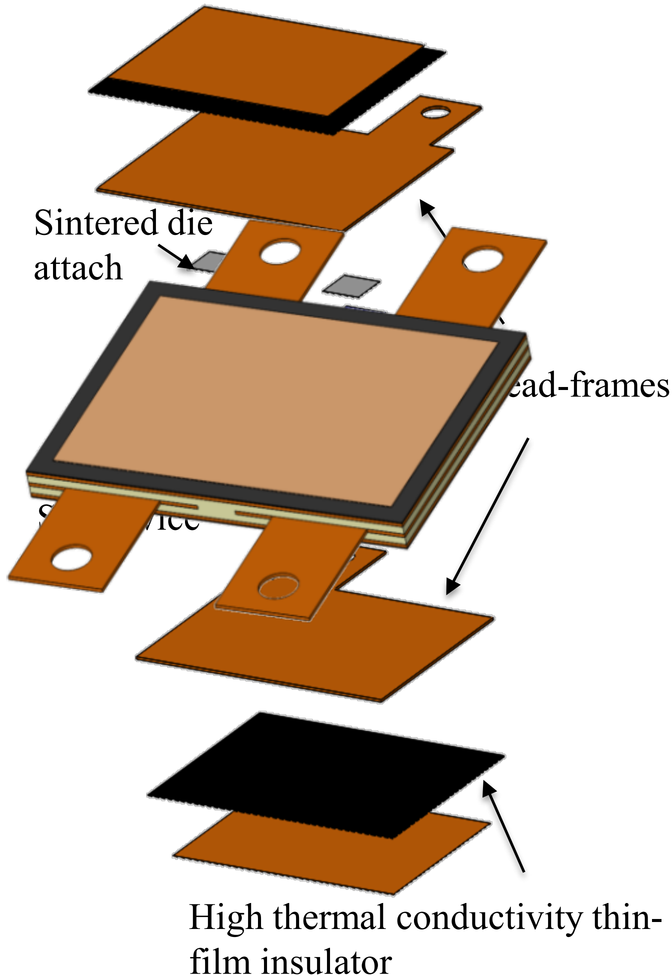
Module cross-section with Si dummy dies



- Uniform temperature elevation show decrease in stress & strain of die-attach, increase in die stress (still lower than the safe limit)
- Superimposed temperature distribution shows overall decrease in stress & strain of die and die-attach indicating superior reliability performance in actual operation
- Unit processes were developed for the fabrication and assembly of 3D stacked power module

Technical Approach

- True 3D integration with vertical stacking of power devices



Electrical Benefits

$L_{parasitic}$
$C_{parasitic}$

Minimum Parasitic inductance

Decoupled parasitic capacitance

Decoupled $C_{parasitic}$
$L_{parasitic}$

- Minimized parasitics L&C suitable for high speed switching

Thermal Management

Metallization thickness scaling up to X10

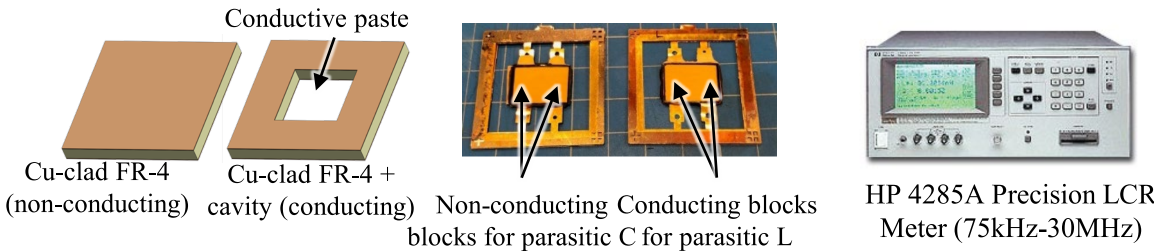
- Thick metal structures for high thermal capacitance
- Double-sided large area interconnect
- Minimized thermal gradient within the package

Manufacturing

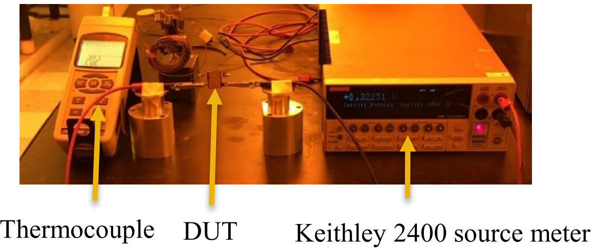
- Highly modular (ease of scalability to higher power)
- Compatible with current and future manufacturing processes (no fixture, no complex via drilling processes)

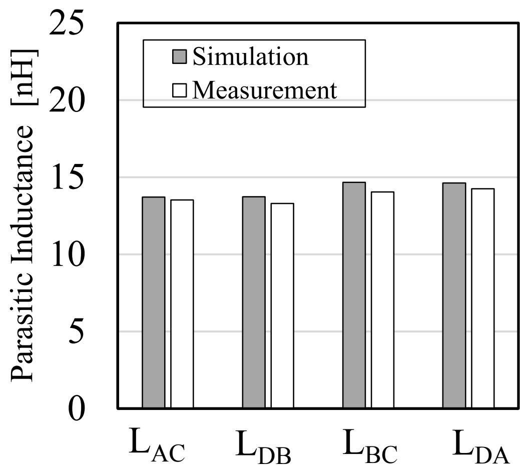
Results & Key Accomplishments

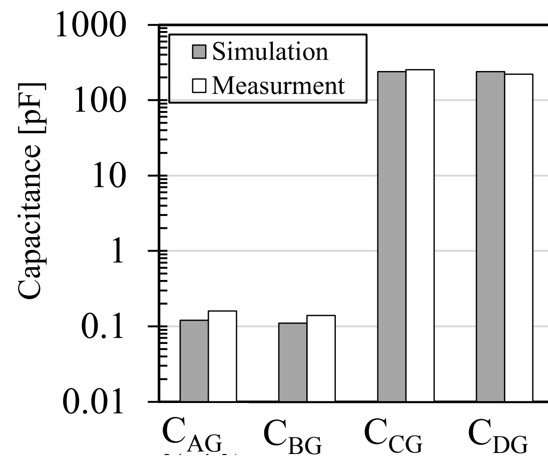
Test vehicles with conducting/non-conducting blocks



Thermal measurement Set-up





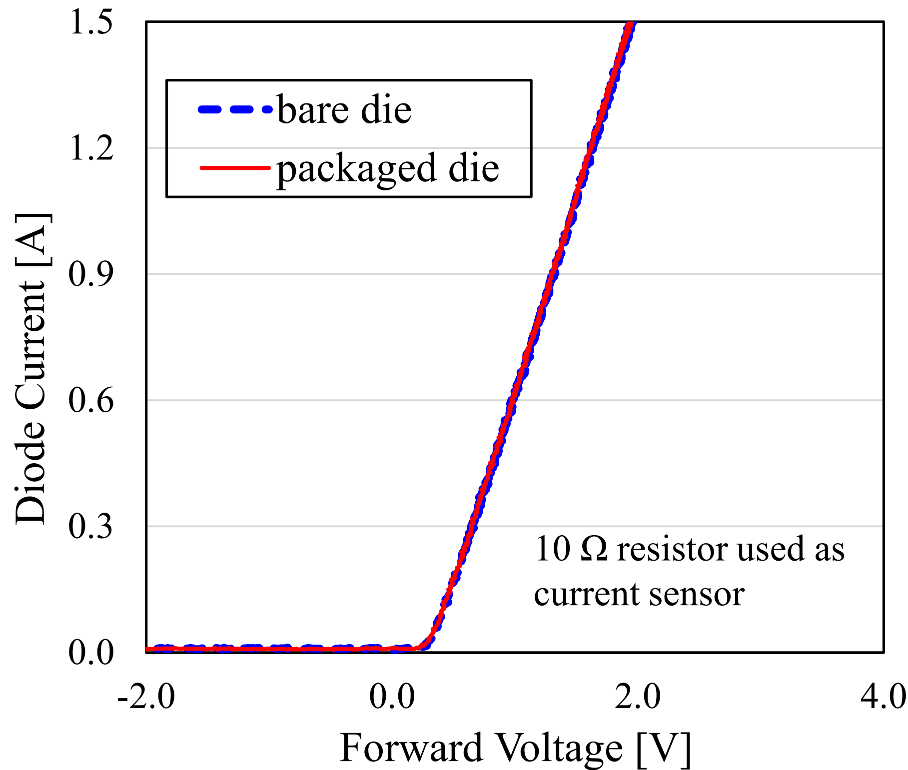


	Simulation	Measurement
Thermal resistance Junction to Ambient [°C/W]	20.0	19.5

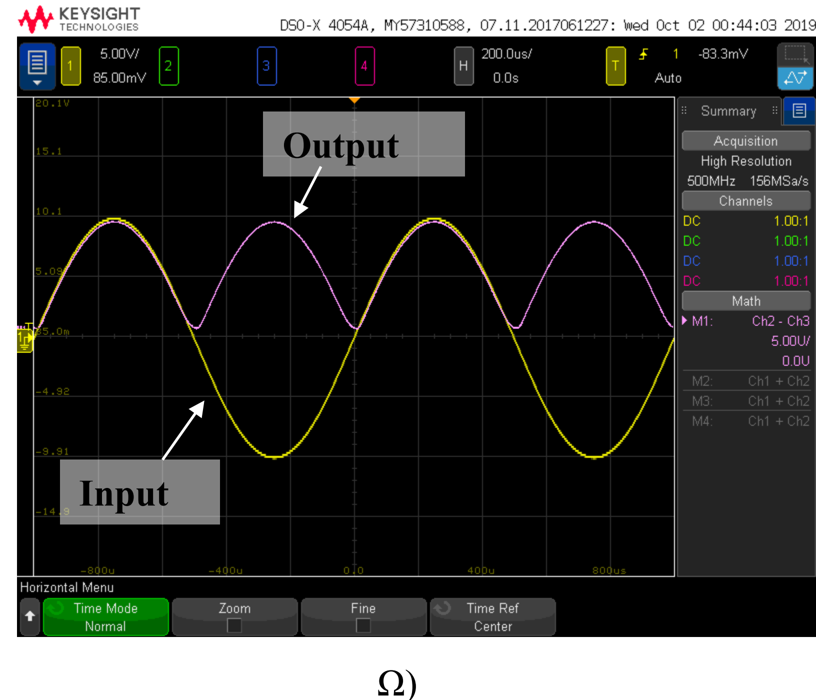
- Test vehicles with conducting/non-conducting blocks, to replace the diodes (non-linear device parasitics)
- <4% difference between simulation and measurements in all the inductance values
- ~30% difference in C_{AG} C_{BG}, but still the values are very small (fringe fields), 4~9% difference in C_{CG} and C_{DG} affected by copper foil lamination process
- Using the junction temperature rise measurement, the junction-to-ambient thermal resistance was calculated

Results & Key Accomplishments

I-V characteristic curve of diode



Input/output waveforms of FBR module

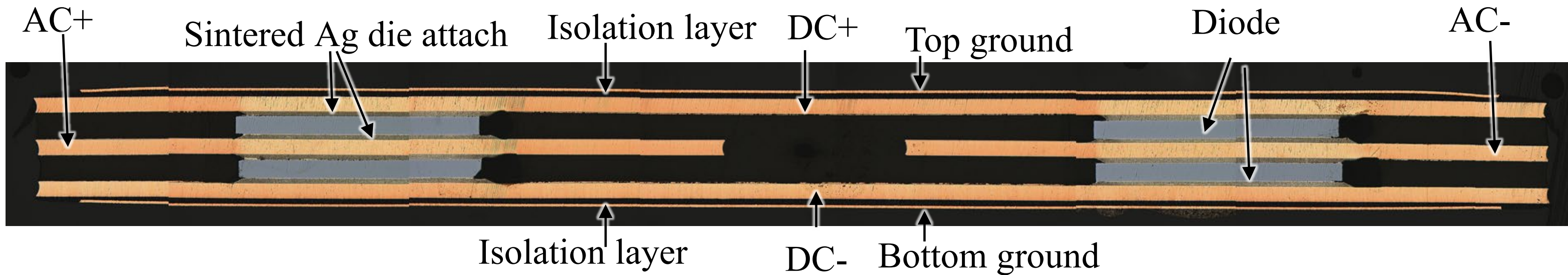


Ω)

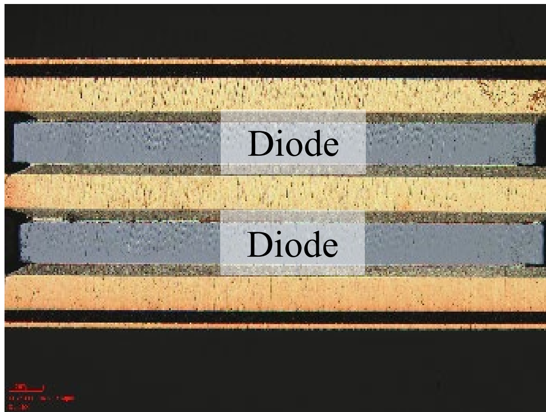
- The I-V characteristic curves of the diode were measured before and after packaging
- Measurements show identical I-V curve characteristics, indicating the 3D stacking process and the 3D package did not change or affect the regular operation of the diodes
- Input/output measurements show the 3D module is functioning well as a rectifier, indicating all four diodes are packaged correctly without any open/short failures

Results and Key Accomplishments

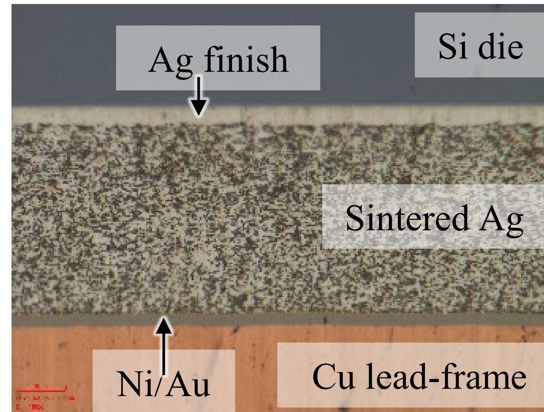
Stitched images of overall module cross-section



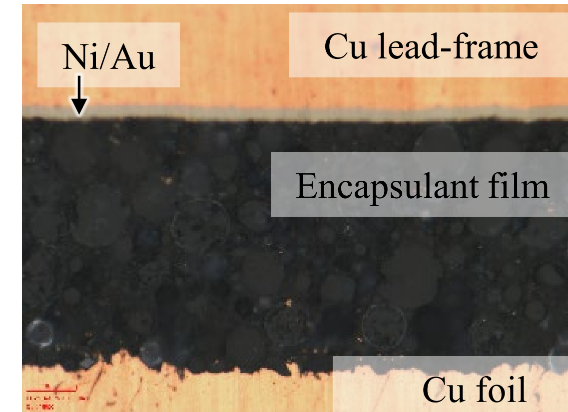
Stacked diodes



Die-attach layer

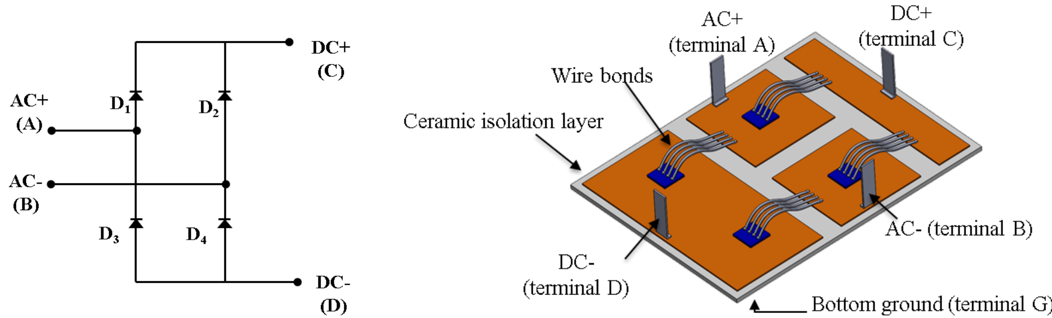


Isolation layer

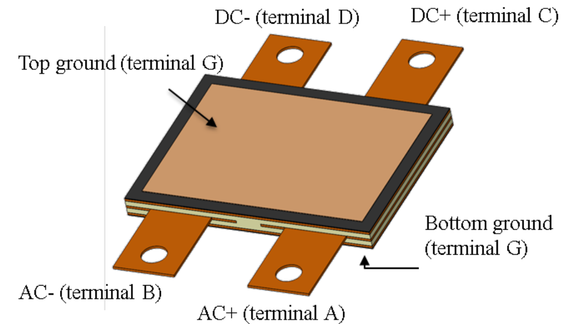


Comparison with Prior Art

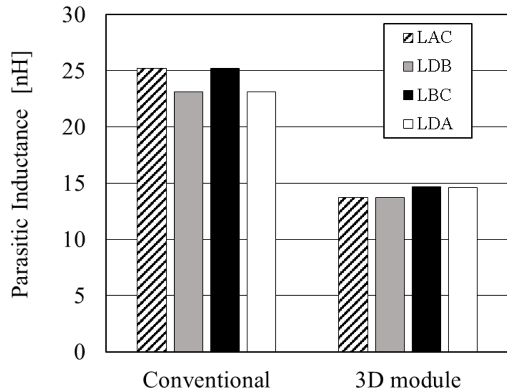
Conventional module

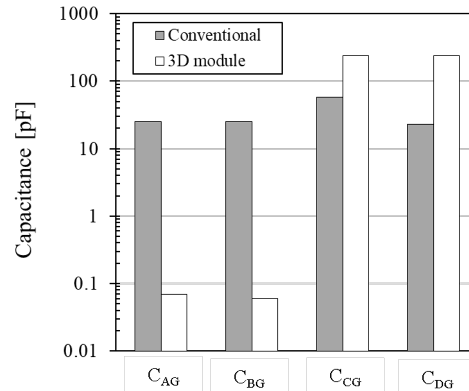


3D module

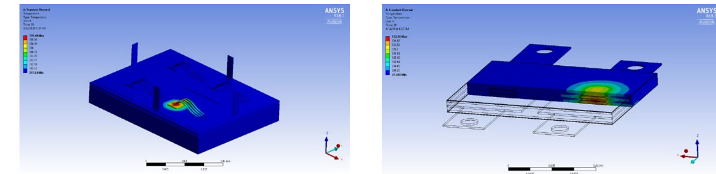


Parasitics L and C





Thermal resistance



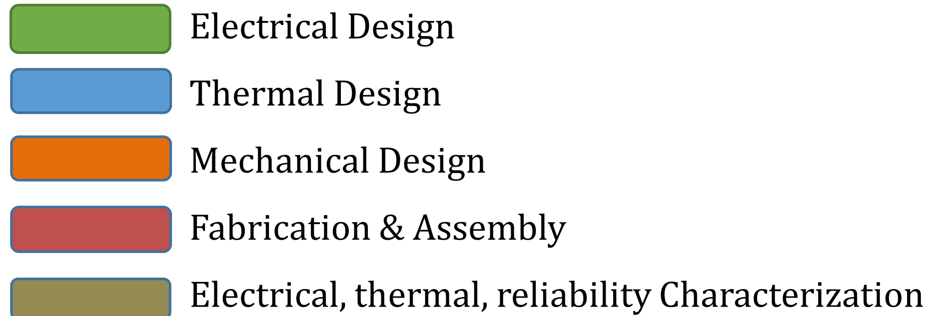
	DBC module	3D Module
Thermal resistance (junction-to-case) [°C/W]	0.83	0.14

1. Package parasitic inductance **-40%** compared to the reference design
2. Package parasitic capacitance C_{AG} & C_{BG} ~**100X** smaller compared to the reference design
3. Package thermal resistance **5X** smaller compared to the reference design
4. Manufacturing process compatible with current tools, infrastructures and processes

Schedule

		2019	2020				2021		
		Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
progress	Electrical design – noise modeling								
progress	Thermal design and optimization								
progress	Mechanical design and optimization								
progress	half-bridge module-fabrication								
progress	Electrical, thermal, reliability characteriztion								
	Electrical design –symmetric layout								
	Thermal design and optimization								
	Mechanical design and optimization								
	Current switch module-fabrication								
	Electrical, thermal, reliability characteriztion								

Light blue: SiC half-bridge power module
Dark blue: SiC current switch module
Light Yellow: Current time window



Summary

Designed and demonstrated a full bridge rectifier power card using the proposed novel 3D stacked power modules with:

1. Package parasitic inductance **-40%** compared to the reference design
2. Package parasitic capacitance C_{AG} & C_{BG} ~**100X** smaller compared to the reference design
3. Package thermal resistance **5X** smaller compared to the reference design
4. Manufacturing process compatible with current tools, infrastructures and processes

Remaining work for SiC half-bridge module and current switch module

- Detailed noise modeling with studies on the impact of 3D package designs
- Thermal and reliability modeling
- Fabrication and assembly with an emphasis on gate terminal wiring
- Switching performance characterization through double-pulse testing
- Reliability assessment including testing in harsh environments