Embedded inductors and Power Stage Co-Design for 48V to 1V Integrated Voltage Regulators

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Research Centers
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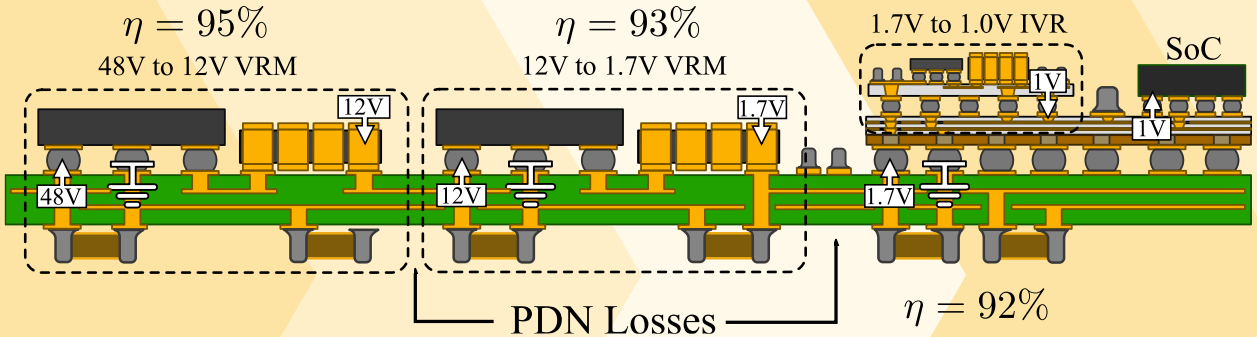
1. Motivation and Objectives

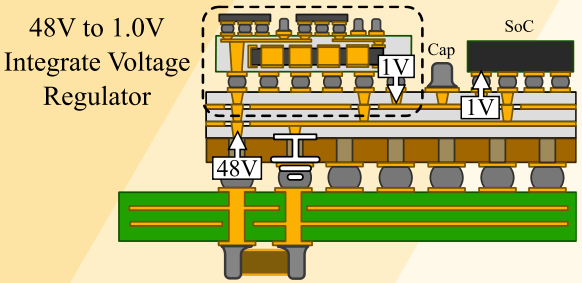
Motivation

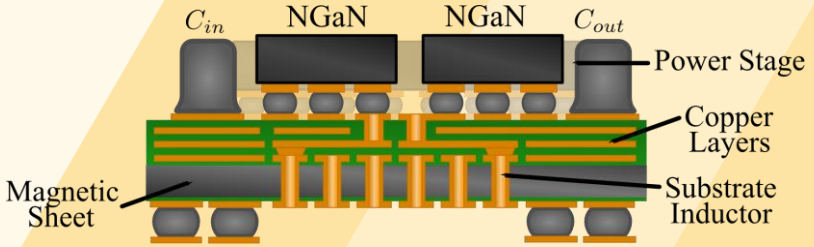
- Power Distribution Networks (PDN) in data centers and servers have multiple down-conversion stages from the AC grid to the SoC load.
- There are many power loss sources in the PDN chain from 48V backplane to 1V System-on-Chip.
- System efficiencies can be as low as 70%



Objective

- Design and demonstrate a 48V to 1V IVR with GaN FETs and embedded inductors.
- Efficiency greater than 90% (Power stage: 95% and Inductor: 95%)
- 1V output voltage, 2.5A output current per phase
- 10 MHz switching frequency to allows passives components miniaturization

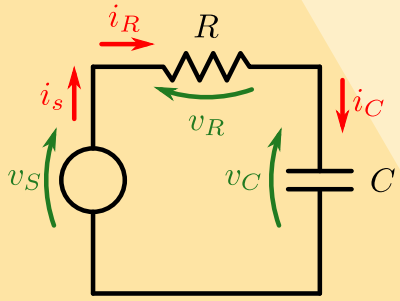




2. Power Loss Analysis

2.1 Power loss due to parasitic capacitances

Let consider the simple RC network, where C is charge by a generic source.



$$v_s(t) = Ri_s(t) + v_C$$

$$v_s(t) = R\dot{q}(t) + \frac{q(t)}{C}$$

$$q(0) = 0 \text{ and } q(T) = Q$$

The power loss in the resistor

$$P = R\dot{q}^2$$

We want to find $i_s(t)$ that minimize the energy loss in R when charging the capacitor in a time T to a charge Q,

$$\min_{v_s(\cdot)} \int_0^T R\dot{q}(t)^2 dt \quad \text{such that} \quad \dot{q} = -\frac{q}{RC} + \frac{v_s}{R}$$

A **constant current** source minimize the power loss to charge the capacitor to $v_C(T)$

We obtain $\dot{q} = \frac{Q}{T} = I_s$ and $v_s(t) = \frac{Q}{TC}t + \frac{2RQ}{T} = \text{linear ramp}$. Then energy loss in R with a constant current source I_s is:

$$E_R = I_s^2 RT$$

If instead we have a constant voltage source V_s, the energy lost in the resistor is:

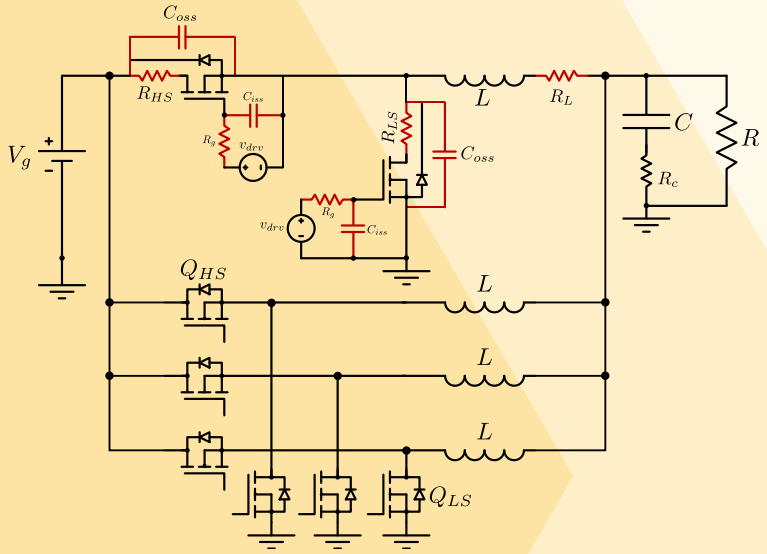
$$E_R = \frac{CV_s^2}{2}$$

A **constant voltage** source produce energy loss that is independent on the value of the resistor and time.

2. Power Loss Analysis

2.2 Single Inductor Based Buck Converter Topologies at 10MHz, 48V to 1V, 10A

Hard Switched Buck Converter



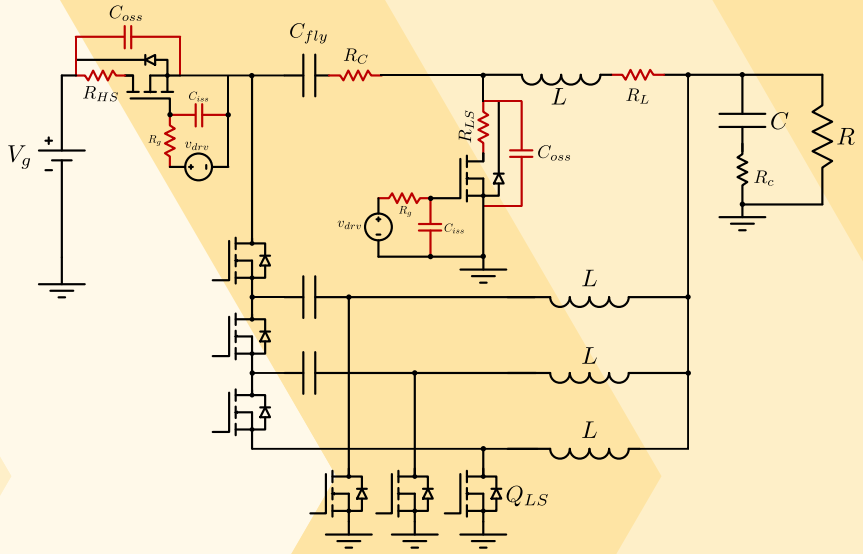
Duty cycle = 2.2%

V_{DS} = 48V

IVR $\eta = 46\%$

mW	HS	LS
P_{cond}	15	93
P_{iv}	91	8
P_{gate}	17	97
P_{oss}	2346	0
P_{sd}	0	62

Hard Switched Series Capacitor Buck Converter [1]



Duty cycle = 9.0%

V_{DS} = 12V

IVR $\eta = 72\%$

mW	HS	LS	Loss mechanism
P_{cond}	29	89	Conduction by R_{HS}, R_{LS}, R_L
P_{iv}	38	8	I-V overlap during on-off transition
P_{gate}	32	94	Gate charge
P_{oss}	400	0	Output capacitance C_{oss}
P_{sd}	0	67	Reverse conduction by body diode

Elements in red burn power, reducing the efficiency

Every time the high-side (HS) switch is turn on, $C_{oss}V_g^2/2$ energy is lost

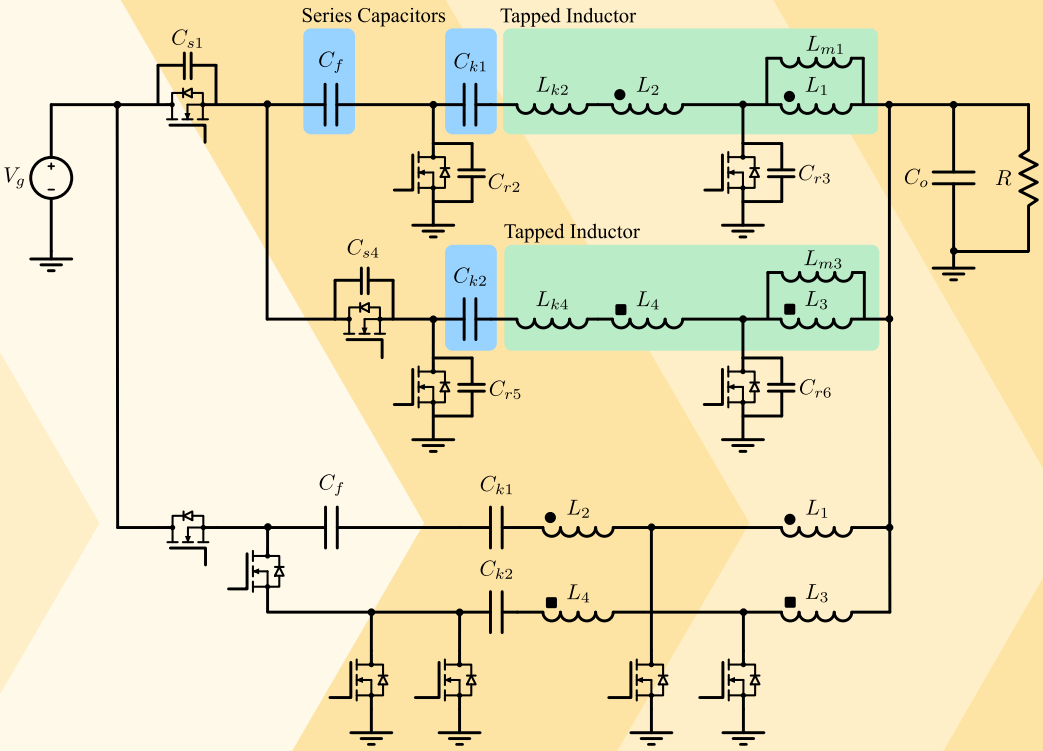
Every time any switch is turn on and off, $C_{iss}V_{drv}^2$ energy is lost

[1] Yungtaek Jang, et.Al., "Multiphase buck converters with extended duty cycle," APEC 2006

2. Power Loss Analysis

2.3 Coupled/Tapped Inductor Bases Buck Converter Topologies [2]

- Inductance L_k act as current source that can charge/discharge the output capacitance.
- The switch capacitor and tapped inductor further extend the duty cycle.
- We have two more transistors that add gate charge losses and series resistance.
- Ck1 and Ck2 also adds series resistance.



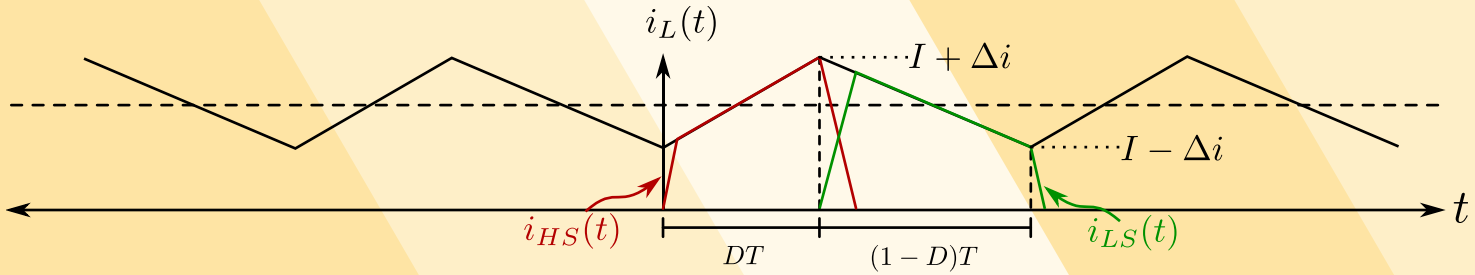
To enable next generation IVR, we need an inductor than can

- Be used as single and coupled or tapped inductor
- Be embedded in the package substrate
- Be compatible with multi-phase converters
- **Have ultra-high efficiency**
- **Have very high inductance density to DC current ratio**

[2] K. I. Hwu, et. Al., "An Expandable Two-Phase Interleaved Ultrahigh Step-Down Converter With Automatic Current Balance," 2017

2. Power Loss Analysis

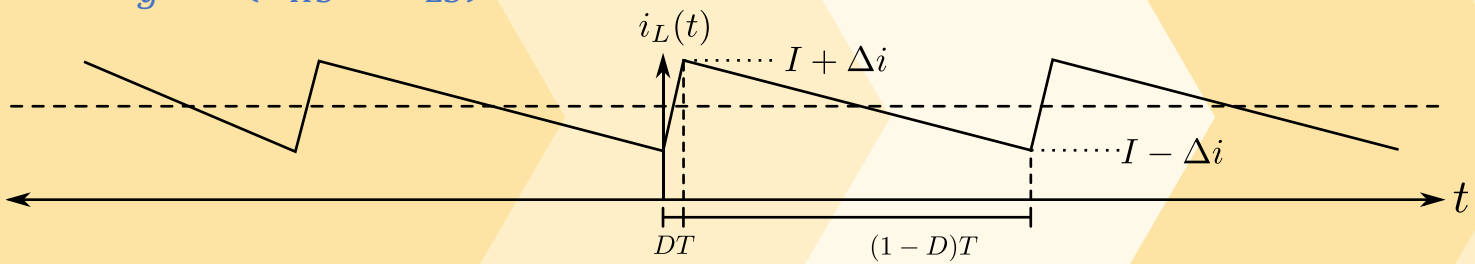
2.4 Inductor Power Loss Spectrum



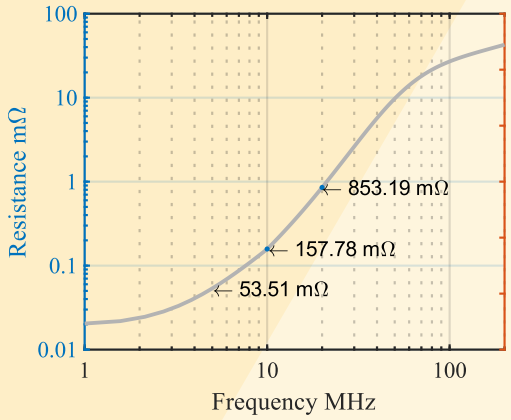
Generalized inductor current ripple

$$D = \frac{V_{out} + I(R_L + R_{LS})}{V_g - I(R_{HS} - R_{LS})} \approx 2.2\%$$

But in a 48V to 1V converter the duty cycle is only D = 2.2%



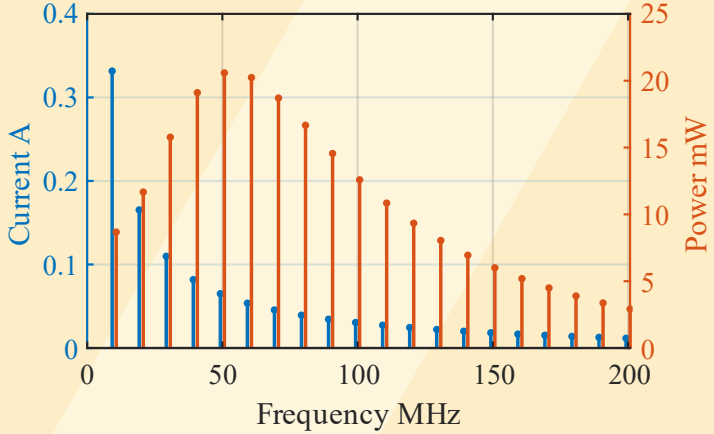
The current ripple look like a ramp



The inductor resistance change with frequency

Each frequency harmonic in the current ripple contribute to the power loss

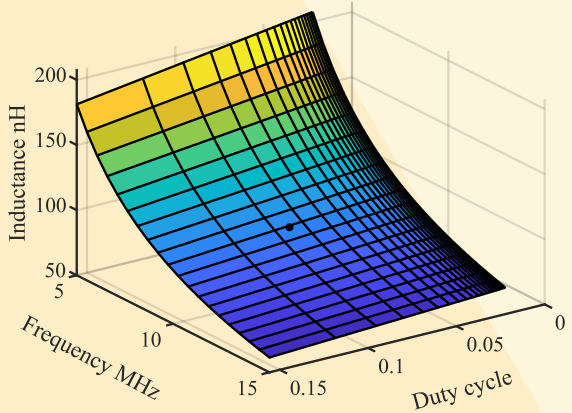
Low duty cycle current ripple has a significant amount of harmonics



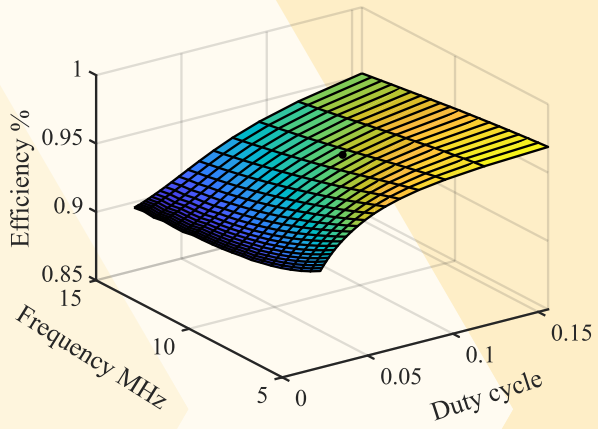
2. Power Loss Analysis

2.5 Inductor's Inductance, Efficiency, Current Ripple Space

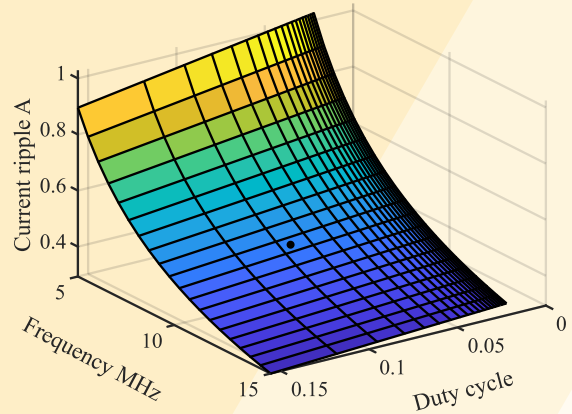
Inductance with Current Ripple = 0.5A



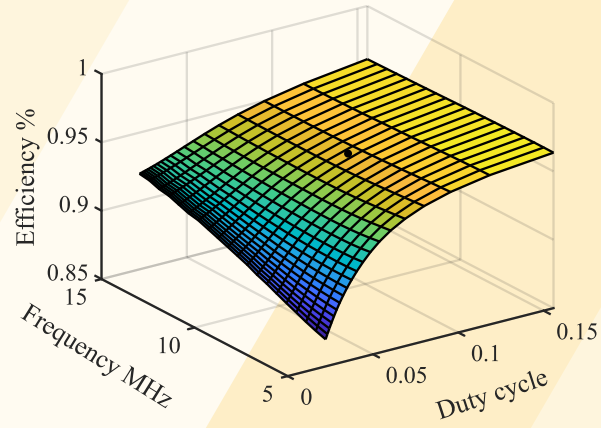
Inductor Efficiency with Current Ripple = 0.5A



Inductor Current Ripple with L = 100nH



Inductor Efficiency with L = 100nH



Below 10MHz the inductance should be greater than 100nH

With duty cycle less than 8% the efficiency drops abruptly

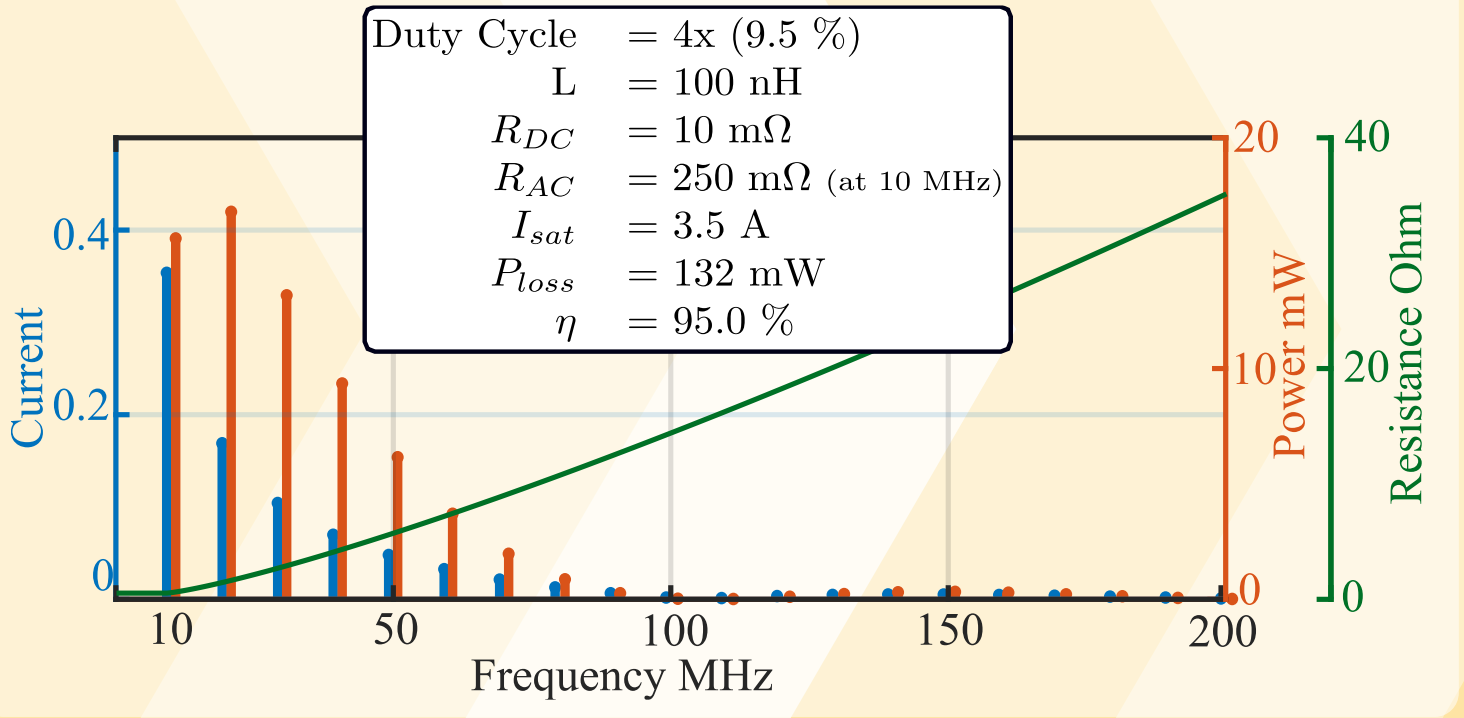
For inductor efficiency of 95% the minimum duty cycle is 8%

With inductance 100nH and frequency below 10 MHz the current ripple is greater than 0.5A

3. Minimum Inductor Requirement

3.1 Inductor constraints

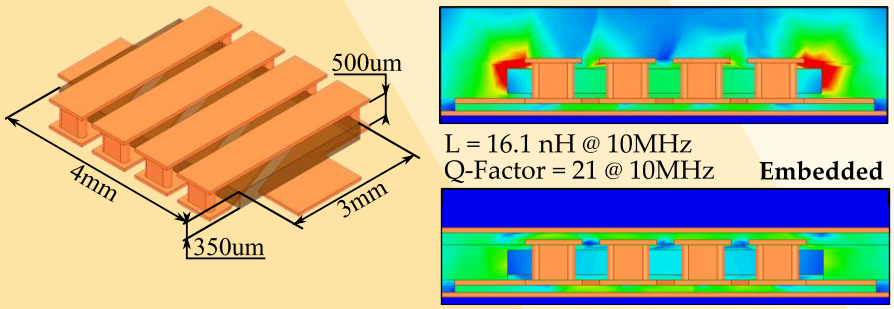
The previous analysis allows us to determine the minimum inductor parameters to achieve 95% of inductor efficiency



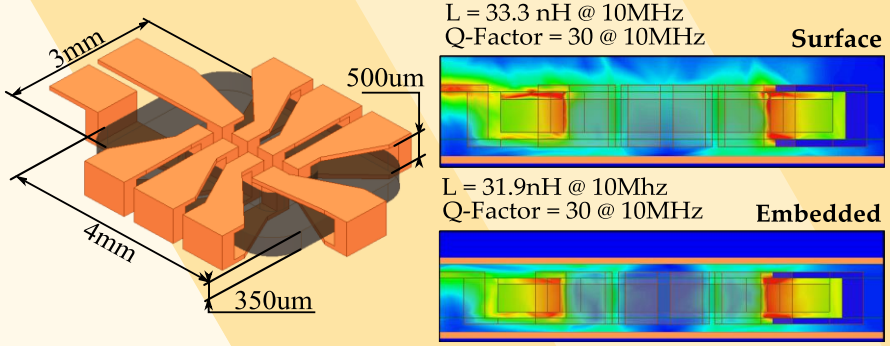
Intel IVR Package Inductor [3]:	140Mhz, L=3.17nH,	R_{DC}=12mΩ,	R_{AC}=102.1mΩ,	2.5A
Ferric IVR Chip Inductor [4]:	100Mhz, L=10nH,	R_{DC}=112mΩ,	R_{AC}=348mΩ,	0.75A

[3] William J. Lambert, *et.al.*, Intel FIVR, TCPMT 2016
[4] Ferric Technology, APEC 2017

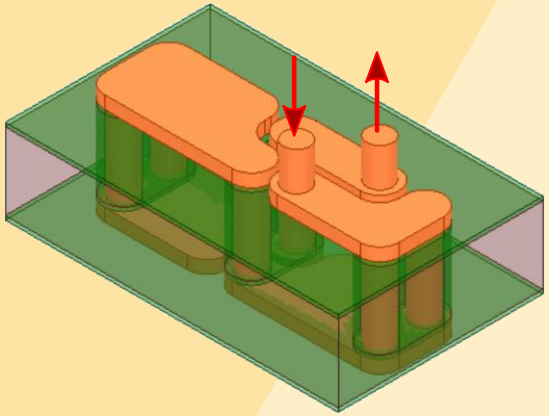
Open magnetic loop inductors can lose more than 35% of inductance when are embedded [5]



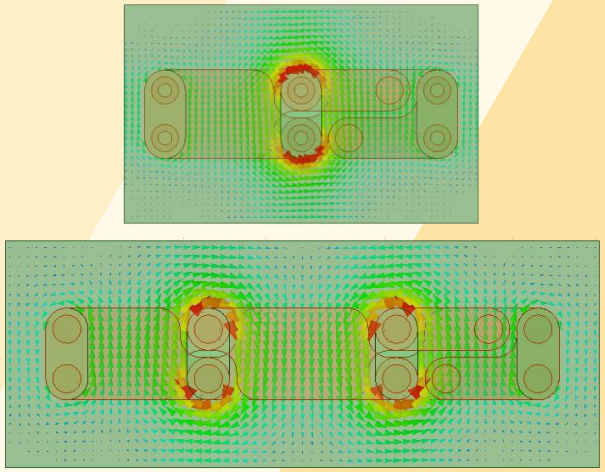
Closed magnetic inductors are almost not affected by near conduction planes [5]



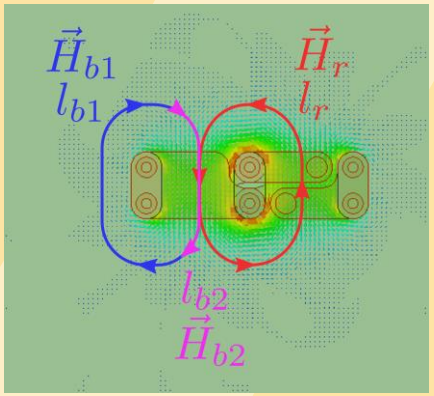
A via is the simplest structure that has a close magnetic path.



The inductor cell present a toroidal field distribution.



It also has an enclose field distribution, confined to the cell.



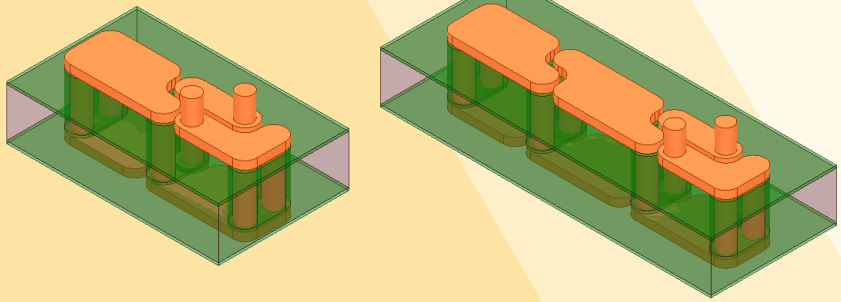
$$H_{b1} \approx 0$$

$$H_{b2} \approx H_r$$

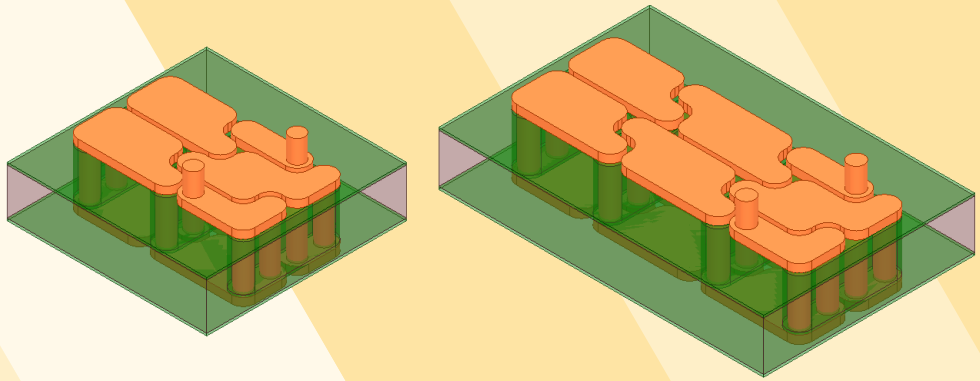
[5] Claudio Alvarez, *et.al.*, "Open and Closed Loop Inductors for High-Efficiency System-on-Package Integrated Voltage Regulators", ECTC 2019

The inductor cell can be scaled to form several different configurations.

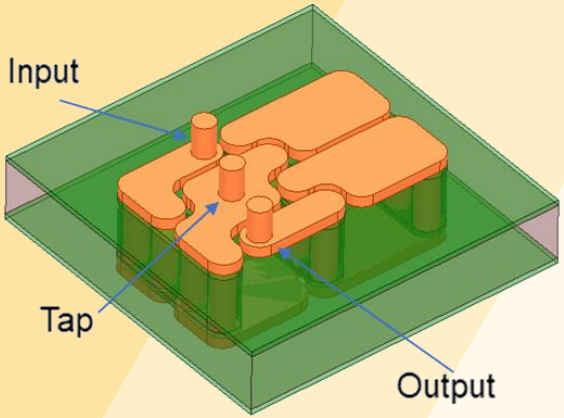
Increase the self inductance



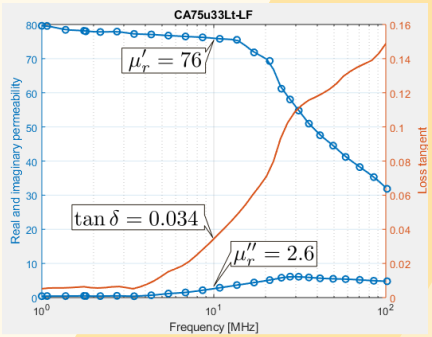
Increase both the self and mutual inductance

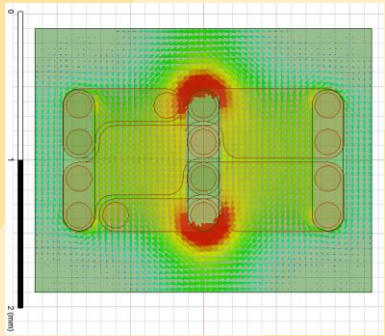


Tap inductors can be easily obtained with coupling ratio greater than 0.90



Required Magnetic Material





I_{DC} [A]	2.5
L [nH]	117
L_{den} [nH/mm³]	53
R_{DC} [mΩ]	9.3
R_{AC} [mΩ]	297

Duty cycle [%]	9.5
Output power [mW]	2500
DC Losses [mW]	58.1
AC Losses [mW]	39.3
Inductor Efficiency [%]	96%

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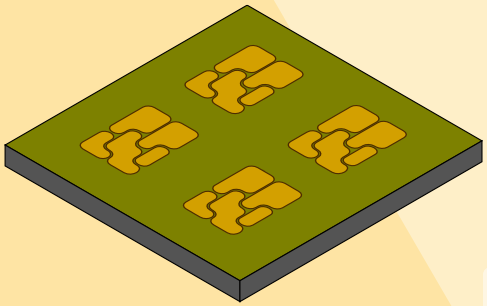
4.3 Simulated Inductor properties for different materials



- Several inductors can be build on the same magnetic sheet substrate.
- Because of the enclose magnetic path properties, no unwanted coupling between adjacent inductors is created.

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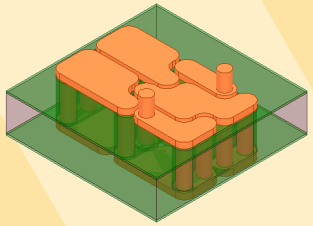


Table of inductor properties for the configuration 2 inductor (code IND036).

f_{sw} = 10 MHz	Panasonic Mat A	Panasonic Mat B	Vendor 1 Mat C	Vendor 2 Mat D	Vendor 2 Mat E
Permeability μ_r'	150	50	49	44	139
Loss tangent $\tan\delta$	0.146	0.200	<0.030	<0.030	<0.030
Thickness µm	130	200	100,200, 250,300	50,100, 200	100,180
Inductor Configuration 2					
Thickness µm	130	200	300	200	180
I_{DC} [A]	**<1.0**	3.5	3.5	3.5	**<1.0**
L [nH]	66.6	34.6	50.4	31.3	83.3
L_{den} [nH/mm3]	151.6	62.2	69.4	56.1	136.9
R_{DC} [mΩ]	9.8	10.7	12.0	10.7	10.1
R_{AC} [mΩ]	635	449	101	73	127
R_{AC} [mΩ/nH]	**9.6**	**13**	2.0	2.3	1.5

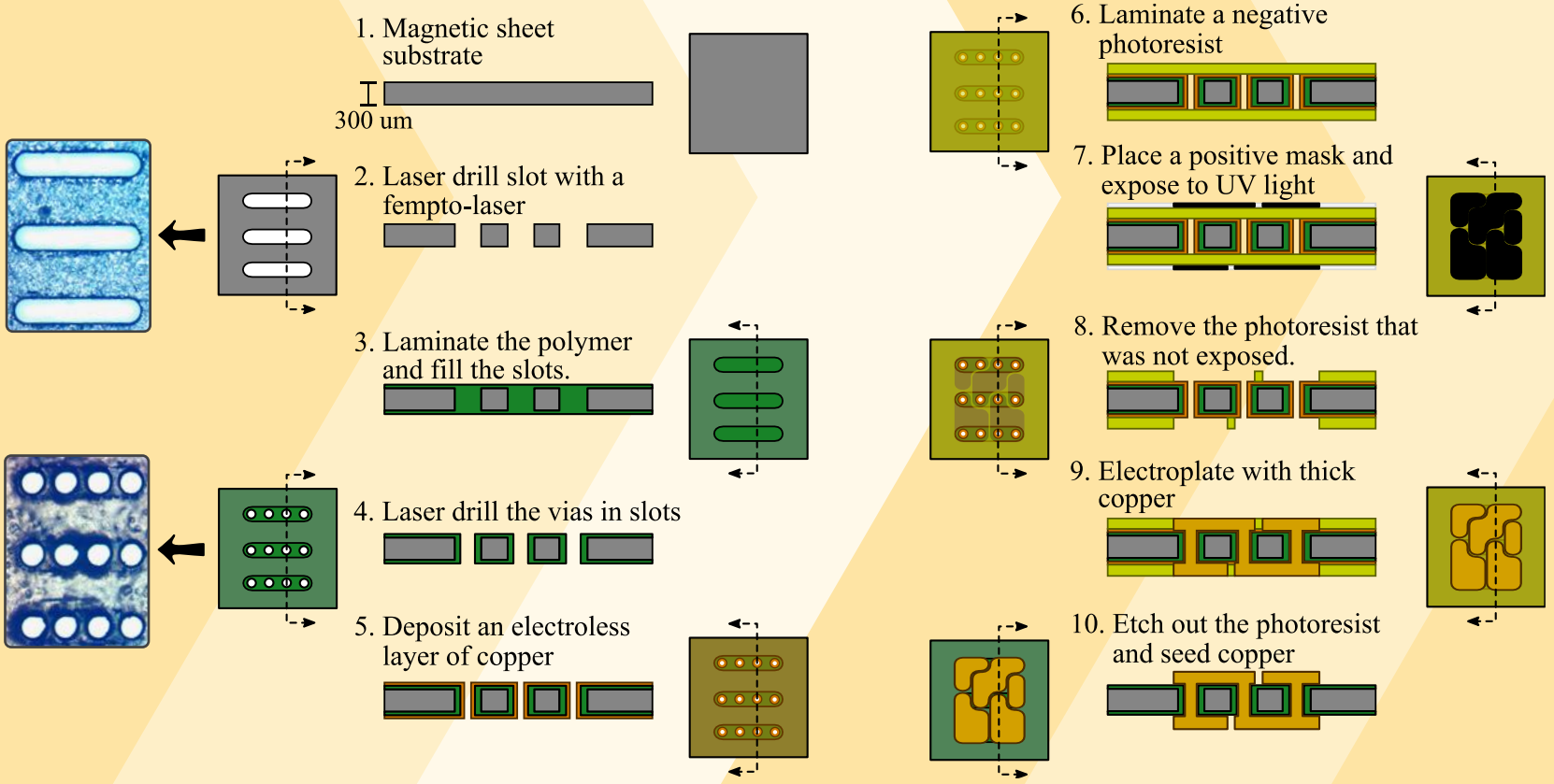
Note: For materials C, D, and E the loss tangent is not accurate due to datasheet extraction was used to obtain them.

5. Fabrication Process

The process is divided in four major steps

1. Mechanical laser drilling *(steps 1 to 4)*
2. Electroless seed copper layer *(step 5)*
3. Lithography *(steps 6 to 8)*
4. Copper electroplating *(steps 9 and 10)*

The entire process is handled in the Packaging Research Center (PRC) at Georgia Tech.



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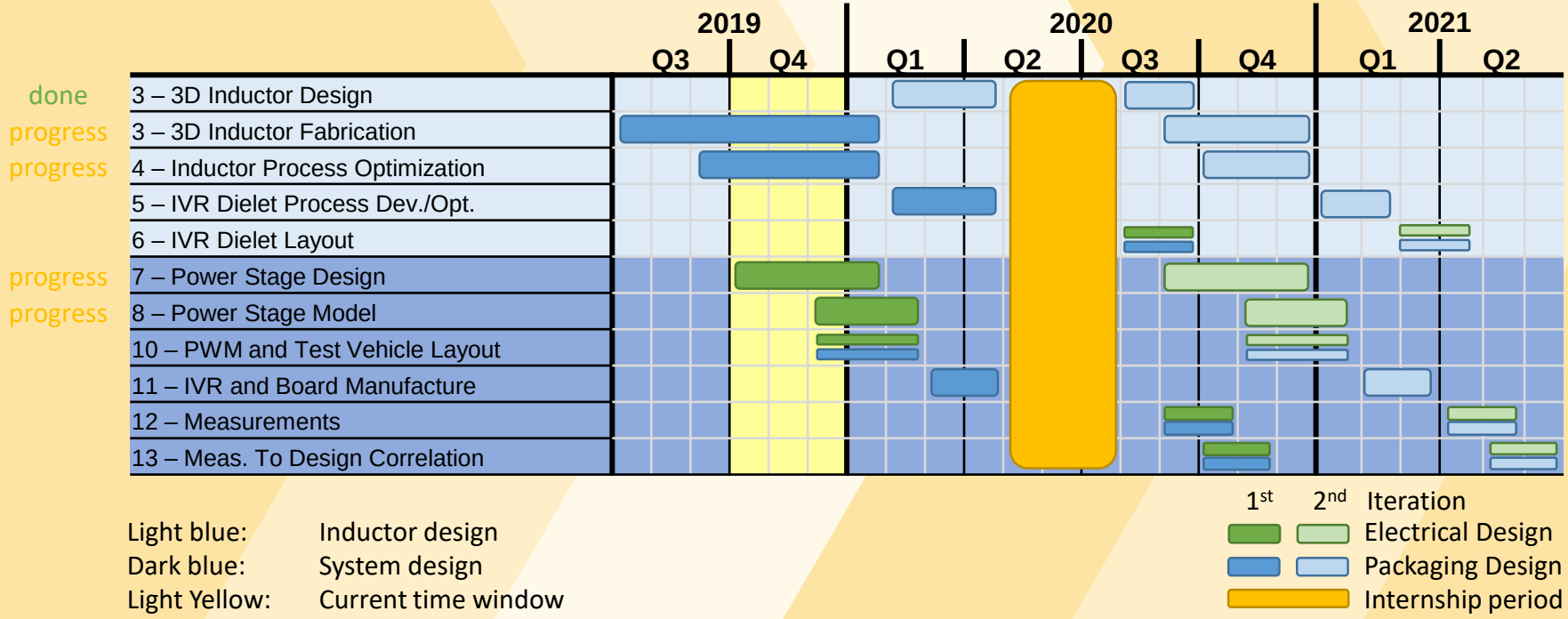
6. Project Timeline

- Single inductor is already designed
- Fabrication is in process of optimization
- A single inductor based 4-phases buck is in design step
- A Journal paper will be prepared with the analysis results so far

- Next step will be preparing a measurement setup to measure the inductor under DC current bias and with triangular current waveform.
- Next iteration will be the design of a tapped inductor based converter



Light blue: Inductor design
Dark blue: System design
Light Yellow: Current time window