Design & Demonstration of 3D Stacked Rectifier Module

Faculty: Dr. Vanessa Smet
Prof. Rao Tummala

Students: Haksun Lee

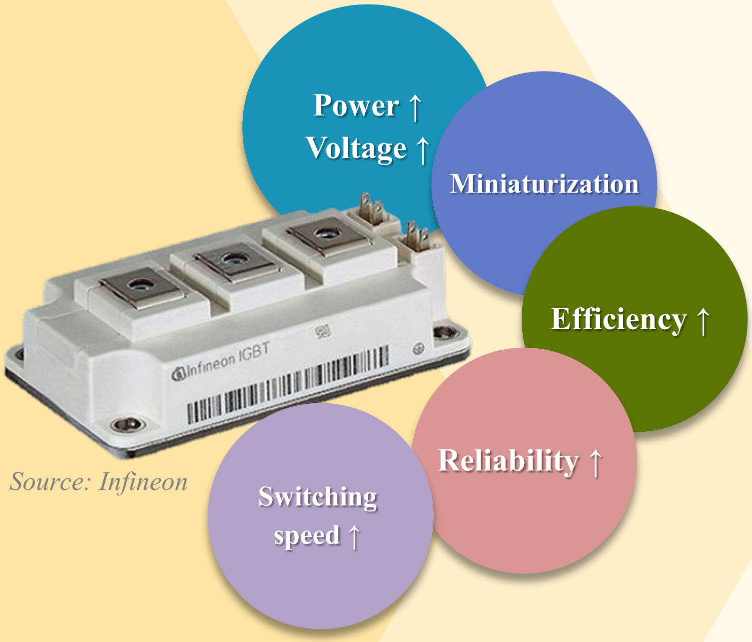
Industry: Nobuo Ogura (Nagase)

Acknowledgements

This work has been supported by PRC Industry Consortium

1. Strategic Need

Requirements for future power modules



Power ↑
Voltage ↑

Miniaturization

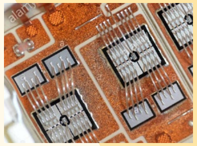
Efficiency ↑

Reliability ↑

Switching speed ↑

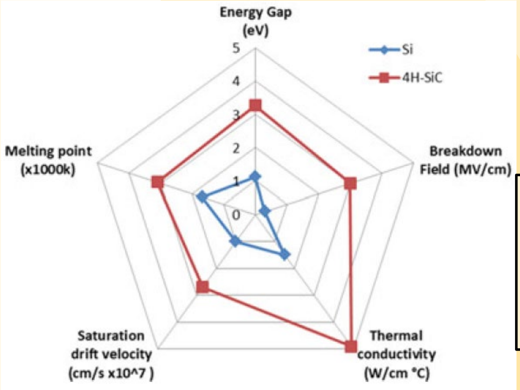
Source: Infineon

Si-IGBTs



SiC-MOSFETs

Source: CREE



[1]

- Excellent properties of SiC make them a perfect candidate for future power conversion applications

Low Voltage

Medium Voltage

High Voltage

< 200V

600V

900V

1200V

1700V

3300V

> 6500V

Si devices

SiC devices

3. Objectives

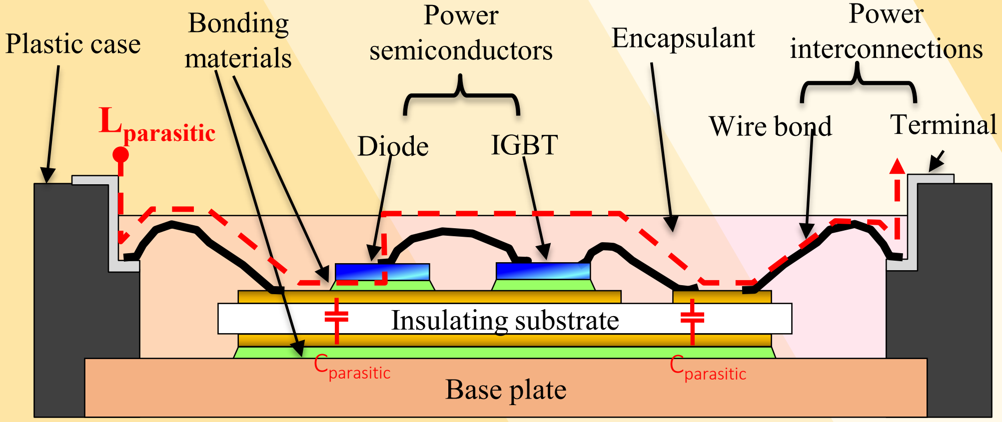
- Design, demonstrate and characterize a new class of ultra-low parasitics, 3D SiC power modules with high efficiency, high dv/dt capability, and enhanced thermal management and thermomechanical reliability

	Parameter	Target	Prior Art	Challenges	Research Tasks
Electrical	Parasitic inductance	-20% reduction *	5.0 ~ 52 [nH]	**1. Trade-offs in multi-physics design** - High-speed switching - High thermal density - High-temp. operation **2. Vertical conduction methods** **-** Bulky fixtures - Complex process (ex. via drilling) - Limited conductor thickness **3. Characterization of 3D module** - Measurement of extremely small L(<nH) and C(<pF)	**1. 3D package design** - Low-parasitics L and C - Low-thermal resistance - Enhanced reliability **2. Fabrication & Assembly of lead-frame based compact 3D module** - Materials and process design - Simple stacking process **3. Characterization of 3D module** - Electrical (L, C, waveforms) - Thermal resistance - Reliability performance
	Parasitic capacitance	-100% reduction *	75 ~ 140 [pF]		
Thermal	Thermal resistance	-20% reduction *	0.1 ~ 1.1 [^{o}C/W]		
Thermomechanical	High temperature storage (200^{o}C)	1000 hr	1000 hr		
	Thermal cycling (-40^{o}C/+125^{o}C)	$N_f > 1000$	$N_f < 1000$		
	Temperature-Humidity (85^{o}C/85% RH)	1000 hr	1000 hr		

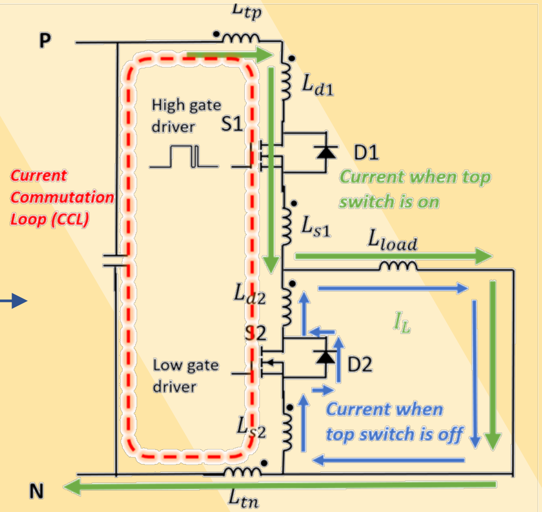
*** Compared to a reference design**

4. Challenges

Parasitic Inductance and Parasitic Capacitance



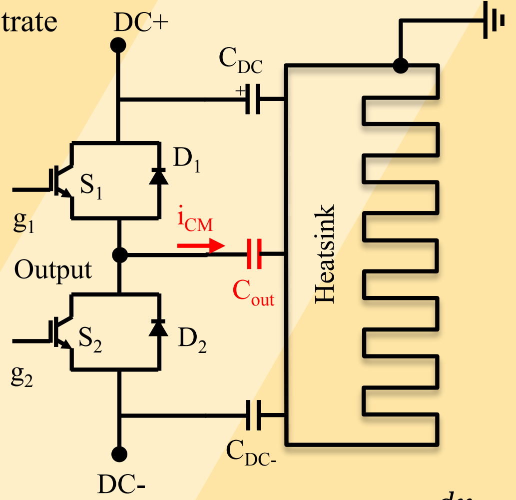
Terminals, wires, traces

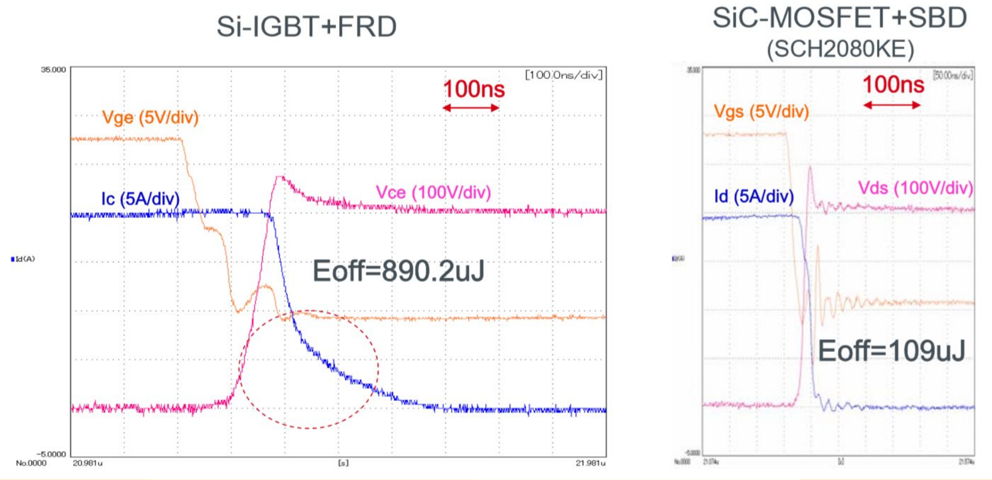


$$L_{CCL} = L_{tp} + L_{d1} + L_{s1} + L_{d2} + L_{s2} + L_{tn} \qquad Q_{CCL} = \frac{1}{R_{total}} \sqrt{\frac{L_{CCL}}{C_{total}}}$$

$$V_{S1} = V_{DC} + L_{CCL} \cdot di/dt$$

Conductor plates on DBC substrate





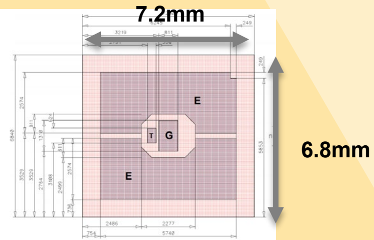
Source: ROHM

$$i_{CM} = C_{parasitic} \frac{dv}{dt}$$

6. Challenges

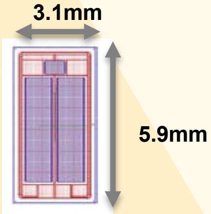
Thermal Challenges

Si-IGBT 1200V 50A



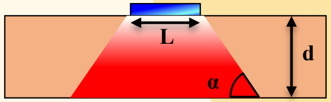
Source: Infineon

SiC-MOSFET 1200V 63A



Source: CREE

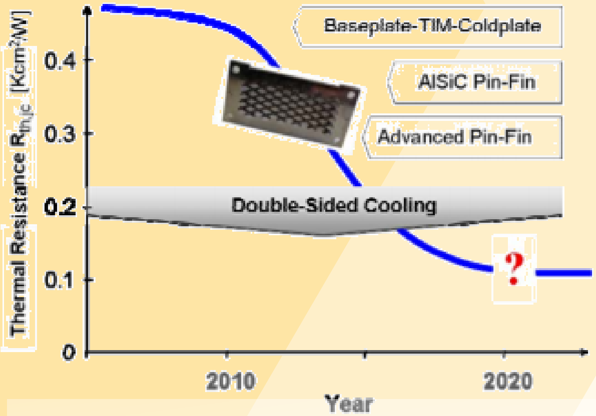
$$R_{th} \approx \frac{d}{\lambda \cdot (L + d \cdot \tan\alpha)^2}$$



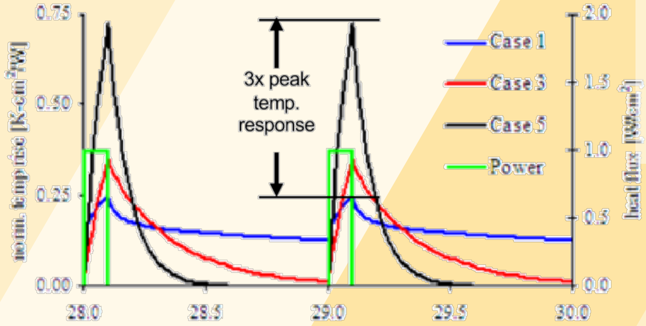
- **d = heat spreader thickness**
- **λ = heat conductivity of heat spreader**
- **α = thermal spreading angle**
- **L = chip edge length**

[4]

- Die size shrinkage from Si to SiC will result in higher thermal densities within the package
- More emphasis on heat spreading and cooling is required



[5]



[6]

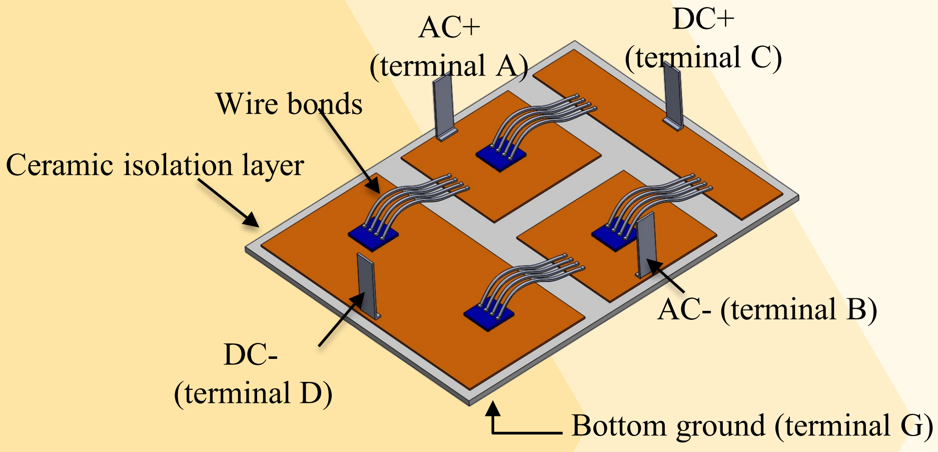
- Steady-state package improvements may not improve transient thermal performance → overdesign

$$\left.\begin{aligned} R_{th} &= \frac{x}{kA_c} \\ C_{th} &\approx \rho c_p A_c x \end{aligned}\right\} \quad \tau \approx R_{th} C_{th} = \frac{\rho c_p}{k} x^2$$

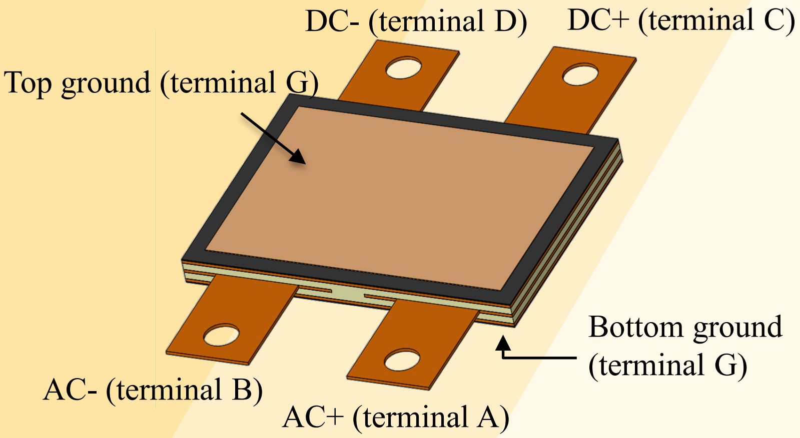
- Single-sided cooling methods generally have relatively high thermal resistances, even with advanced cooling strategies
- In order to meet future thermal management cost target for EV/HEV, double-sided cooling will be necessary

7. Package Designs

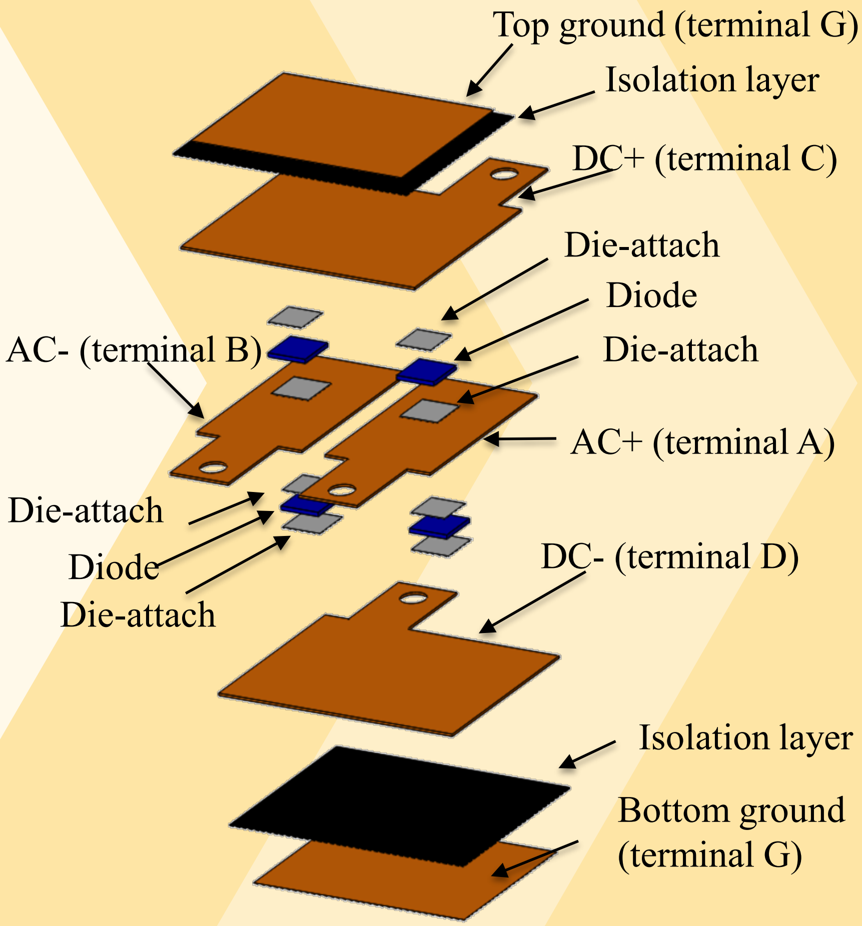
Conventional Power Module



3D Stacked Power Module

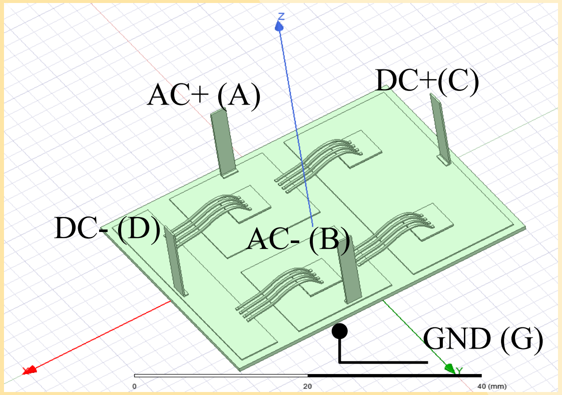


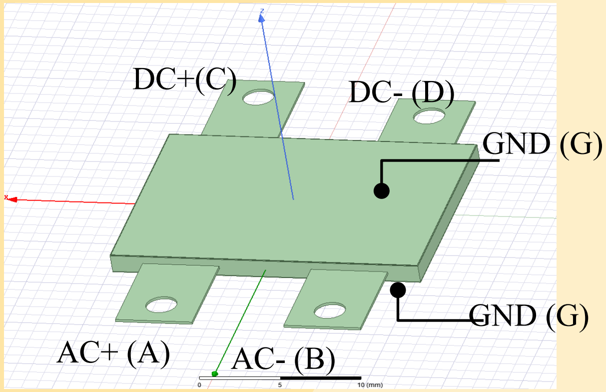
3D Stacked Power Module (Expanded)

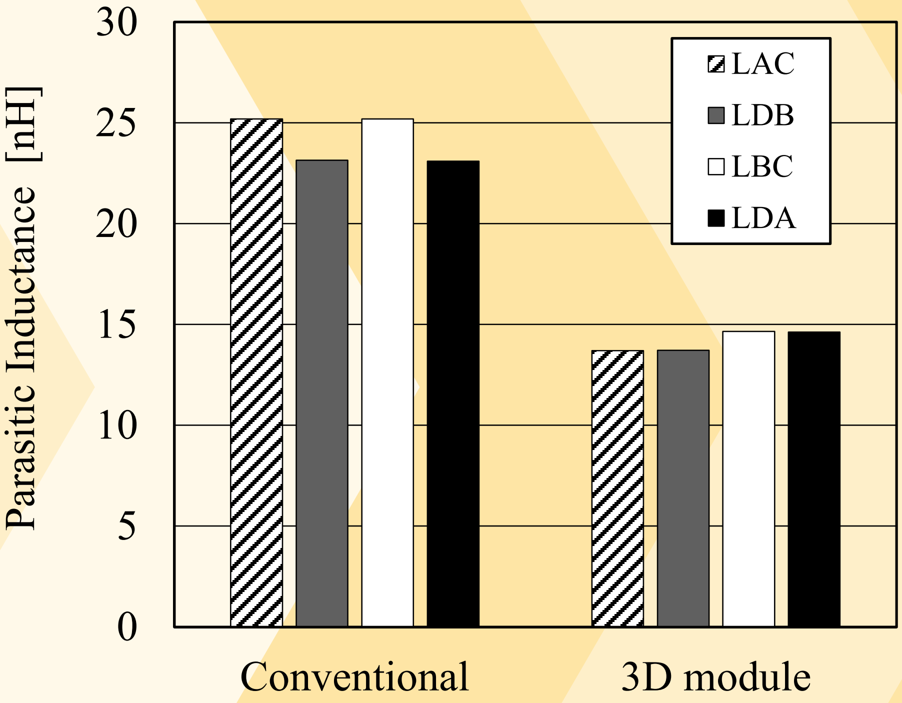


7. Electrical Simulation

Simulation of parasitic L



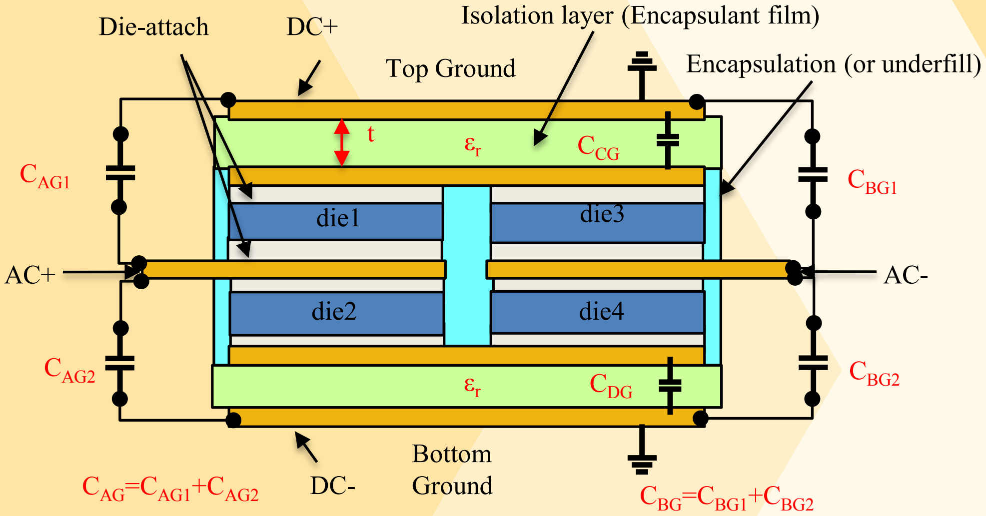


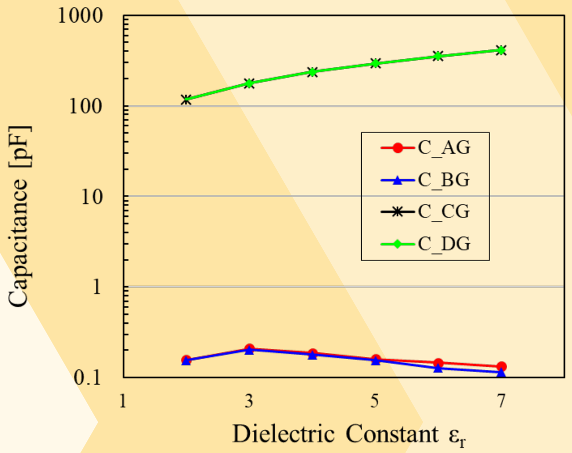


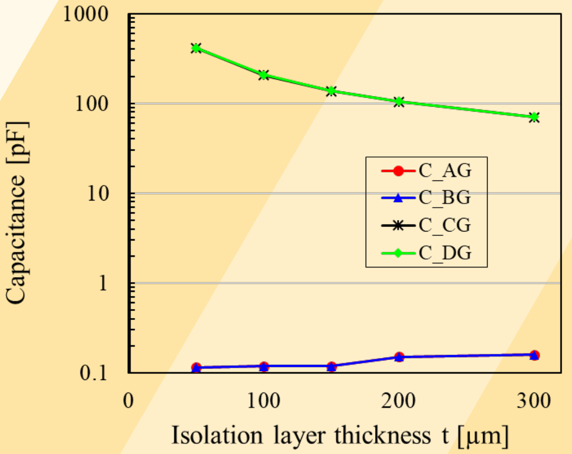
- Parasitic inductances from terminal to terminal were extracted using ANSYS Q3D @ 500kHz
- 3D module has about 40% reduced parasitic L, due to removal of wire bonds and vertical stacking

8. Electrical Simulation

Simulation of parasitic C



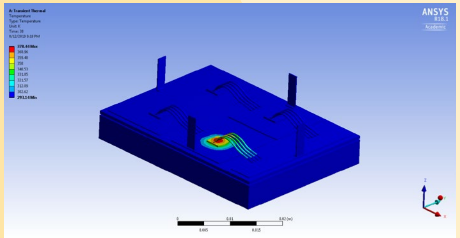




- Parasitic capacitances from terminal to terminal were extracted using ANSYS Q3D @ 500kHz
- The dielectric constant and thickness of encapsulation film layer had no significant impact on C_{AG} & C_{BG}
- C_{CG} & C_{DG} increase with increased dielectric constant, while they decrease with increased thickness
- High dielectric constant (e.g. 6~7) with thin encapsulant film (< 100um) is desirable for preferred parasitic configuration

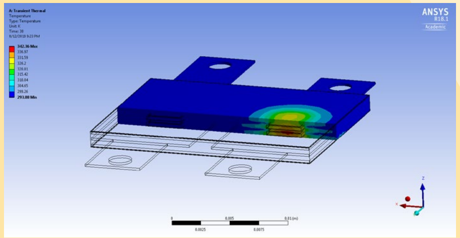
9. Thermal Simulation

Conventional module

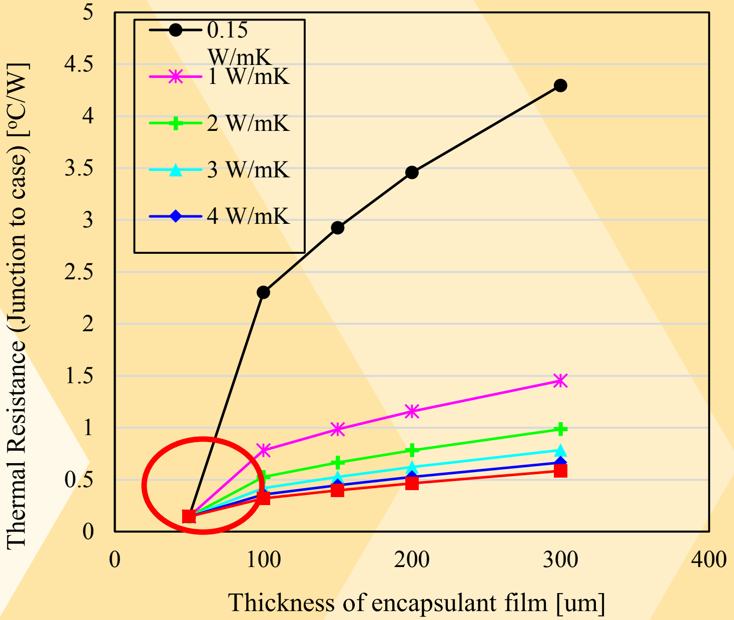


DBC (Al_2O_3 600um, Copper 200um)
Heat spreader 5mm (copper)
h=10,000W/m^2K, 293K ambient
P=100W per die volume

3D module



Lead-frame thickness =200um
Encapsulant film 50um, 3 W/mK
h=10,000W/m^2K, 293K ambient
P=100W per die volume



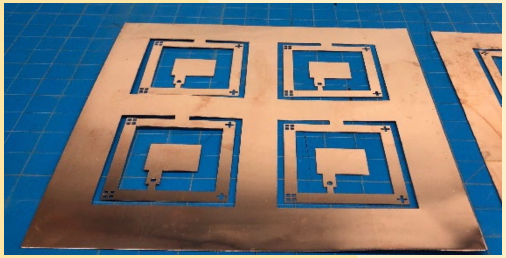
Lead-frame thickness 200um
h=10000W/m^2K
Heat generation = 100W per die volume

	DBC module	3D Module
Thermal resistance (junction-to-case) [ºC/W]	0.83	0.14

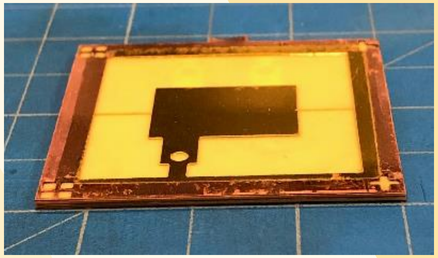
- Compared to conventional package, the thermal resistance is ~5X smaller in the 3D case

10. Fabrication & Assembly

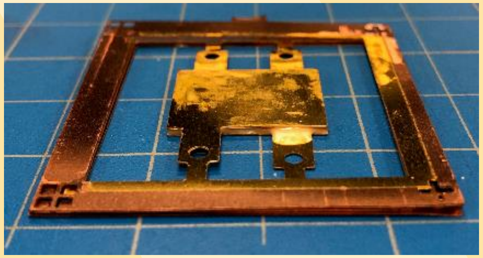
Wet-etched copper plates

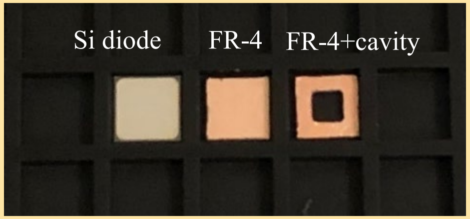


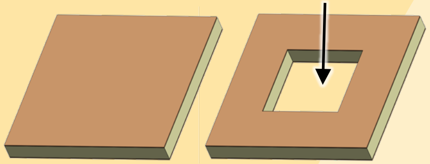
After sintering process with spacers



After molding process



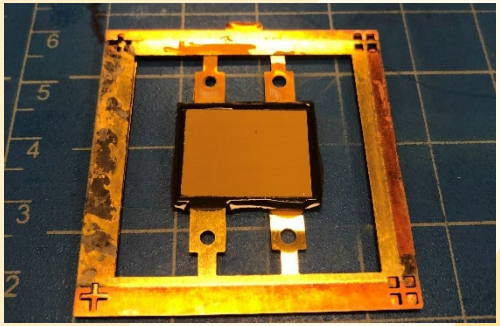




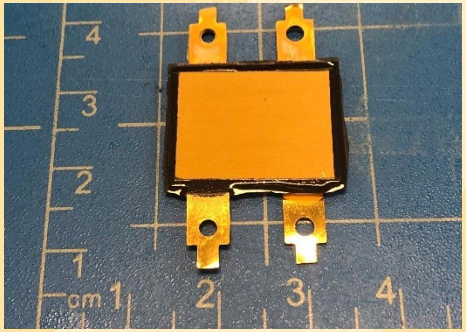
Cu-clad FR-4 (non-conducting)

Cu-clad FR-4 + cavity (conducting)

Lamination of encapsulant film with copper foils



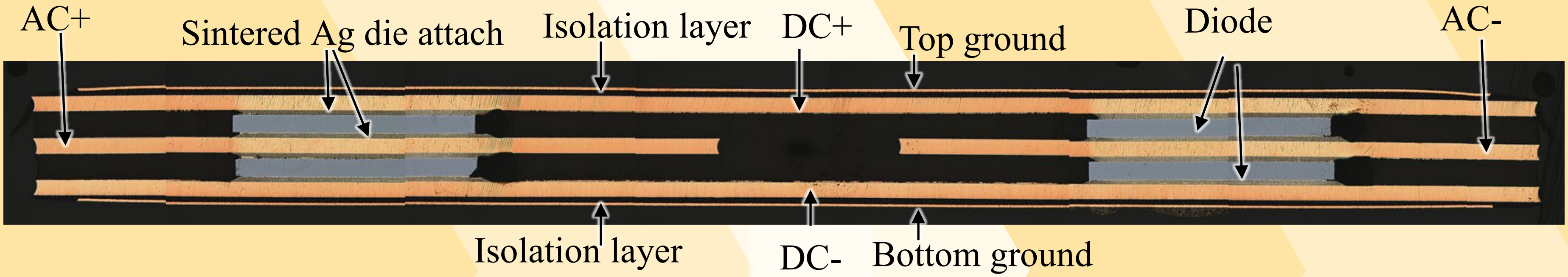
Completed module



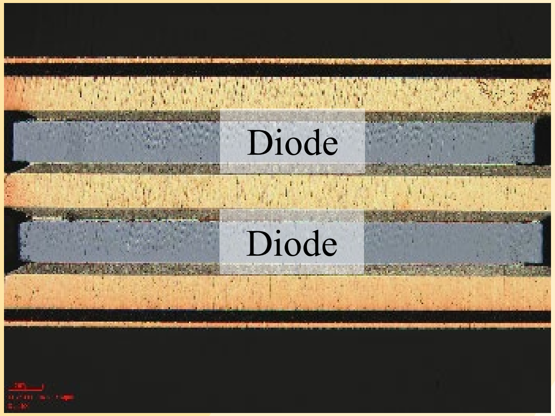
- Mechanical test vehicles using dummy conducting/non-conducting blocks to replace the active diodes were also made using the same process flow to measure parasitic inductances and capacitances

11. Package Cross-Section

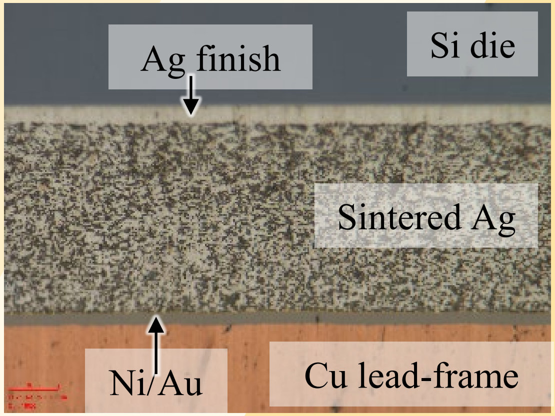
Stitched images of overall module cross-section



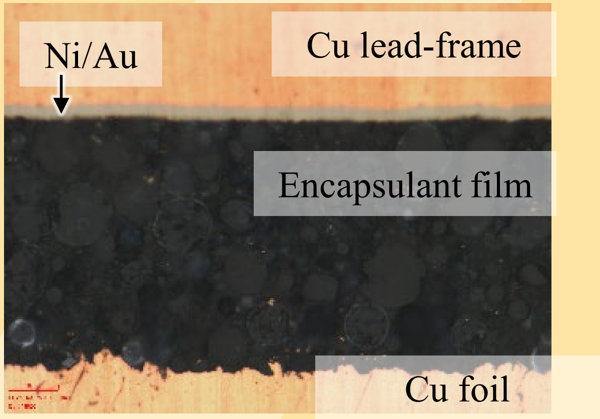
Stacked diodes



Die-attach layer

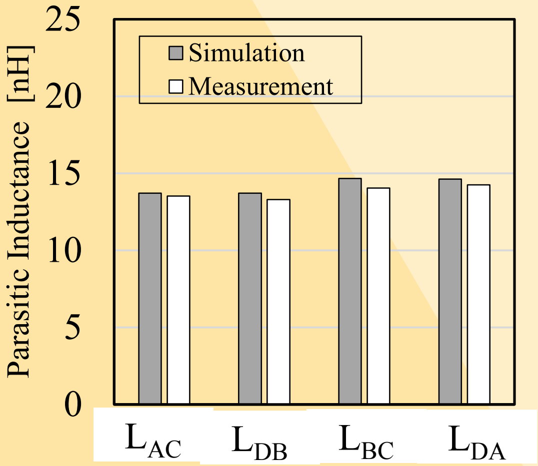


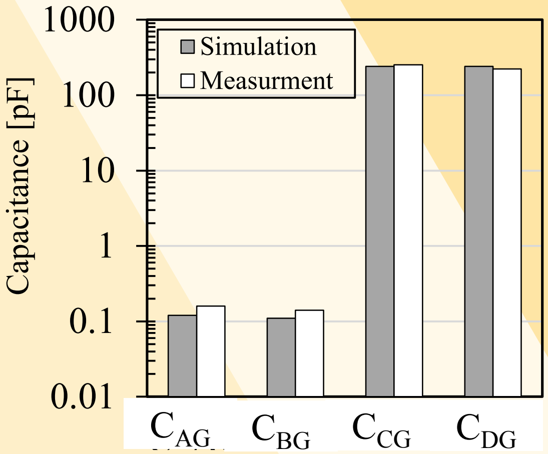
Isolation layer



12. Module Characterization

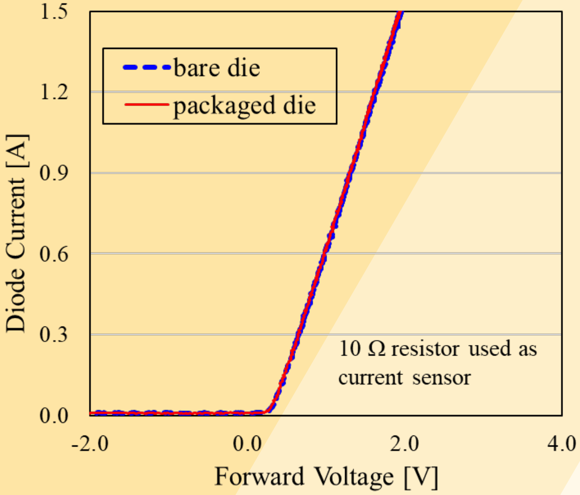
Parasitics L&C measurements



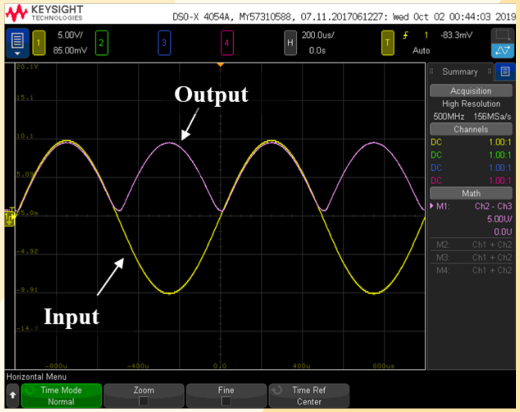


HP 4285A Precision LCR Meter (75kHz-30MHz)

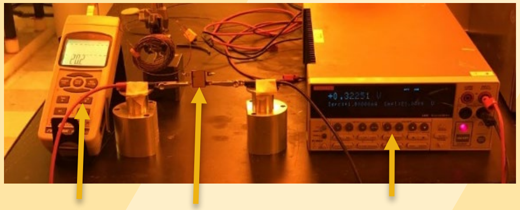
I-V characteristic curve of diode



Input/output waveforms of FBR module



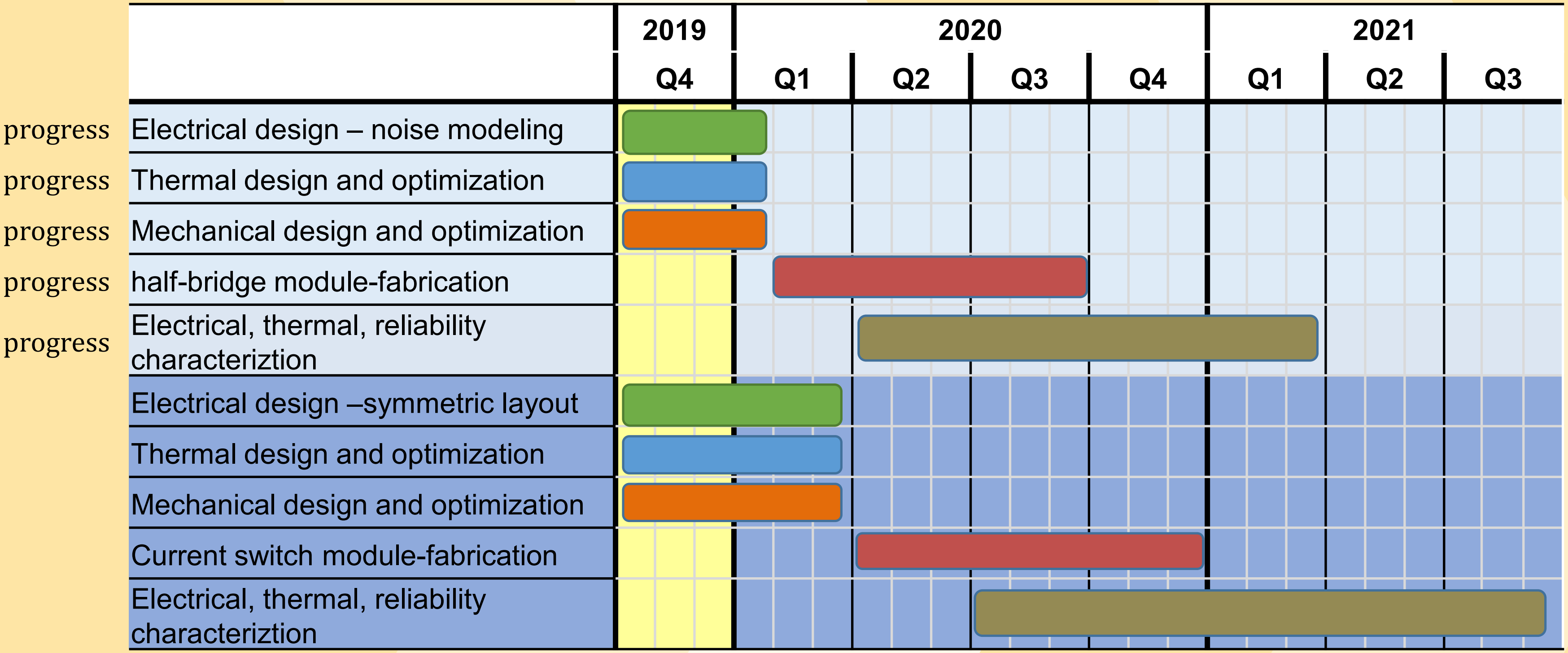
Resistive load (78 kΩ) at the output of rectifier



Thermocouple DUT Keithley 2400 source meter

	Simulation	Measurement
Thermal resistance Junction to Ambient [^{o}C/W]	20.0	19.5

13. Schedule



		2019	2020				2021		
		Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
progress	Electrical design – noise modeling	🟩	🟩						
progress	Thermal design and optimization	🟦	🟦						
progress	Mechanical design and optimization	🟧	🟧						
progress	half-bridge module-fabrication		🟥	🟥	🟥				
progress	Electrical, thermal, reliability characteriztion			🟫	🟫	🟫	🟫		
	Electrical design –symmetric layout	🟩	🟩						
	Thermal design and optimization	🟦	🟦						
	Mechanical design and optimization	🟧	🟧						
	Current switch module-fabrication			🟥	🟥	🟥			
	Electrical, thermal, reliability characteriztion				🟫	🟫	🟫	🟫	🟫

Light blue: SiC half-bridge power module
Dark blue: SiC current switch module
Light Yellow: Current time window

🟩 Electrical Design
🟦 Thermal Design
🟧 Mechanical Design
🟥 Fabrication & Assembly
🟫 Electrical, thermal, reliability Characterization