Thermal and Thermomechanical Analysis of GPE Packages:
Integrated Heat Spreader Design for High Heat Flux Densities and Reliability

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Thank you!

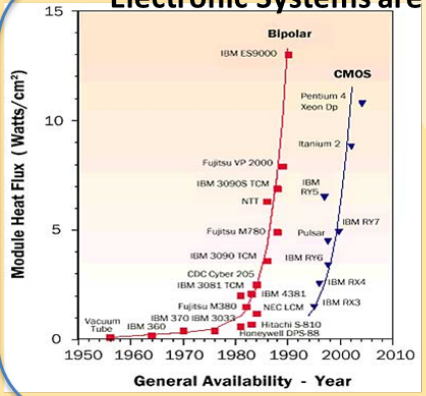
1. Objectives

- Modeling, design, fabrication and demonstration of low stress, high thermal conductivity, low thermal resistance interfaces between device and Cu heat spreader in glass embedded packages
- Integration of thermal management solution into a MCM GaN PA/CMOS GPE package with EMI shielding

Parameter	Prior Art	Target	Challenges	Research Tasks
Tj (°C)	< 85		Thermal vs. Stress (Performance trade-off)	Transient, multi-physics modeling and design of interface to the chip (material properties and geometry) for low-stress and high thermal conductivity
Heat Flux (W/mm²)	3-10			
Bulk thermal conductivity (W/mK)	5-399	≥400		
CTE (× 10⁻⁶)/K	-30-17.8	≤4.2	Minimizing thermal interfacial resistance: Ultra-thin, compliant, high thermal conductivity interface	Design, demonstrate, and characterize material for low stress, high thermal conductivity, low thermal resistance interface between device and Cu heat spreader
Thermal Resistance (mm²K/W)	5-30	<2		
			Low temp, low pressure processing	Material processing through electrodeposition
Thickness (μm)	200-500	<100	Integration of heterogeneous structures with long-term reliability	Integration of process in multi-chip, GPE module with fine-line RDL, EMI shielding, and thermal decoupling

2. Strategic Need

Electronic Systems are Becoming Thermally Limited



Paredes, 2014

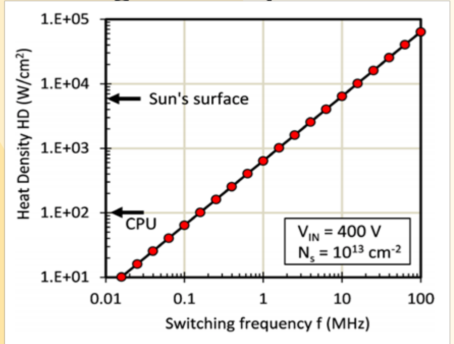
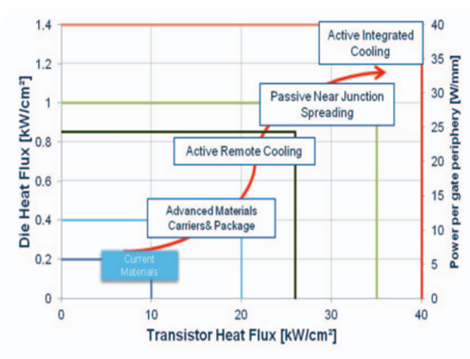


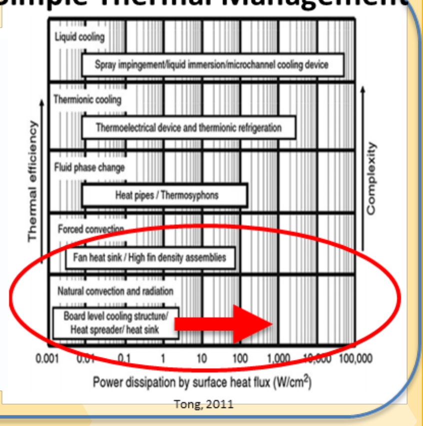
Figure 26. Calculated heat densities of GaN chip depending on output frequency under hard switching condition.

Fuller, Millet, 2011

Expanding Thermal Efficiency of Simple Thermal Management

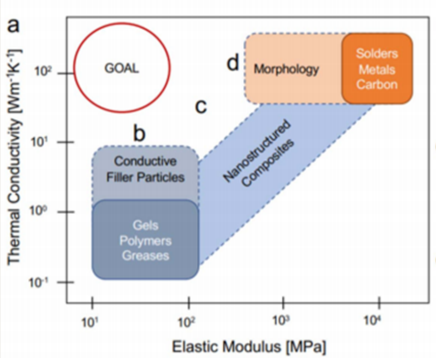


Guggenheim, 2017

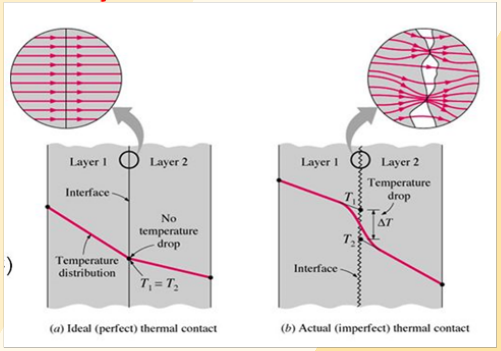


Tong, 2011

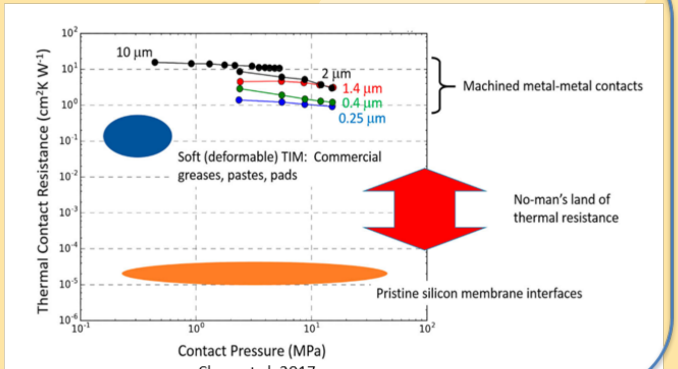
Material Innovation for High Thermal Conductivity but Low Thermal Contact Resistance Interfaces to Handle Max Heat



Chen, et al. 2019



Baiku, 2015

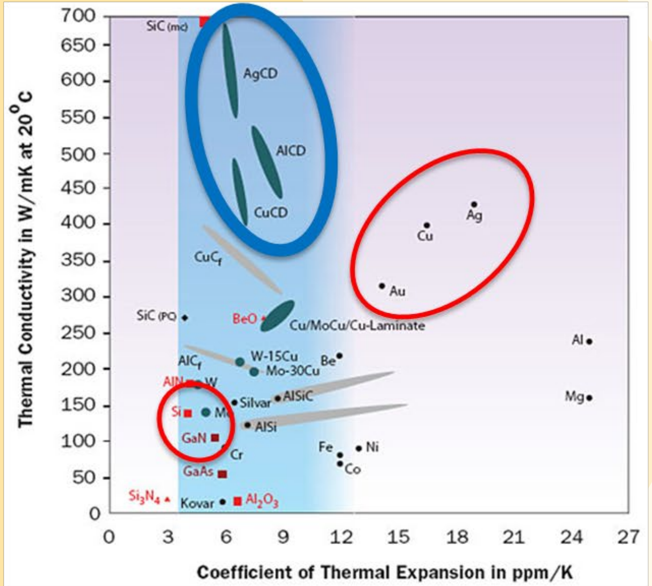


Chen, et al. 2017

Need for new class of passive substrate-integrated thermal management solutions that will be able to handle increased heat densities of emerging power ICs

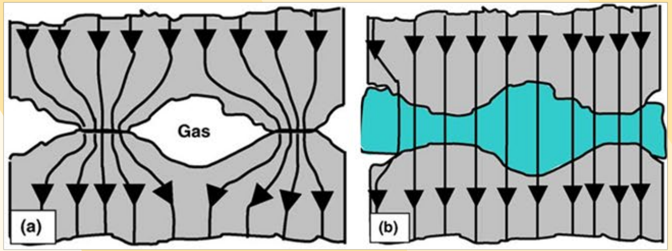
3. Challenges

Stress vs. Thermal Conductivity: Tradeoff



- Metals, such as Cu, have excellent thermal conductivity but suffer from higher CTE compared to Si/GaN/SiC/Glass
- Composite materials are being created to solve this challenge

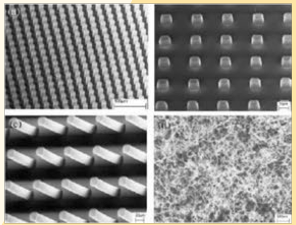
Minimizing Thermal Interfacial Resistance



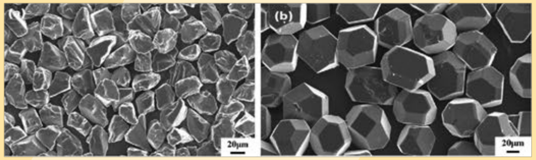
$$\mathrm{R_{TIM}} = \frac{BLT\ (\downarrow)}{k_{TIM}\ (\uparrow)} + R_{C1} + \cancel{R_{C2}}$$

- To minimize thermal contact resistance, need perfect contact
- Ultra-thin material that can conform to surface

Low-Temperature, Low Pressure Processing



CNTs

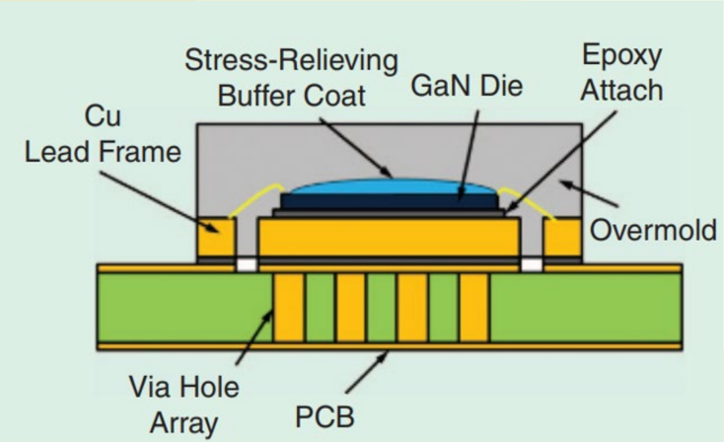


Diamond-Based Materials

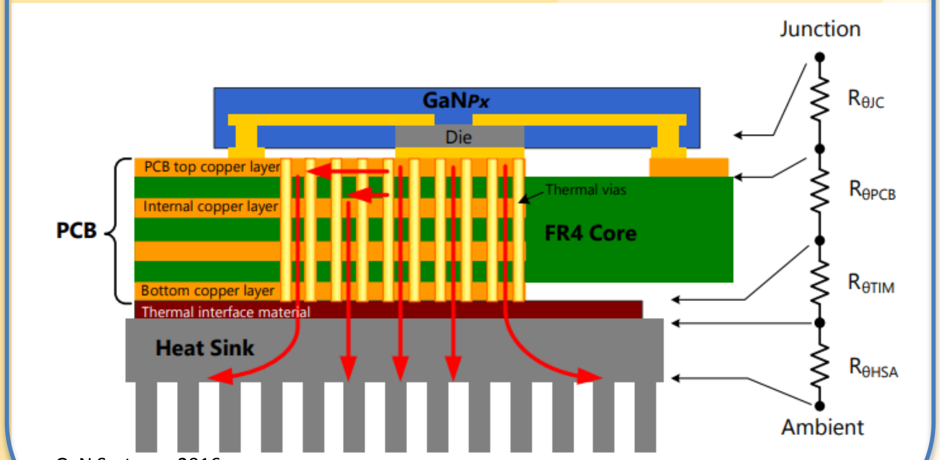
- Processing of exotic materials are high-temp (~800°C) and high pressure (~60MPa)
- Temperatures and pressures should ideally be compatible with existing CMOS processes

4. Prior Art

Thermal Vias

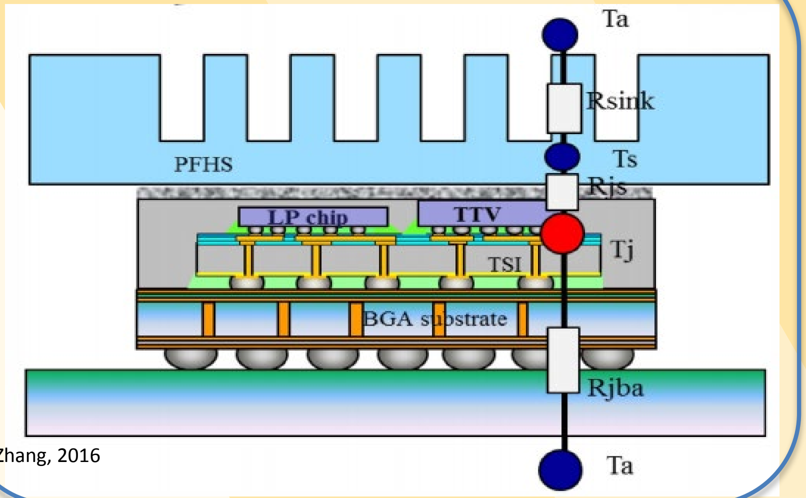


Mach , Muller, 2016



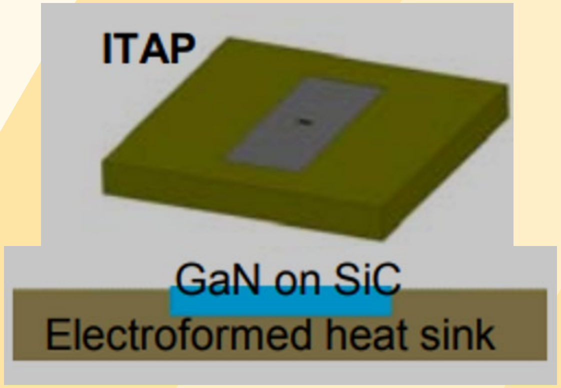
GaN Systems, 2016

Exposed Backside Heat Spreader



Zhang, 2016

Electroformed Heat Sink

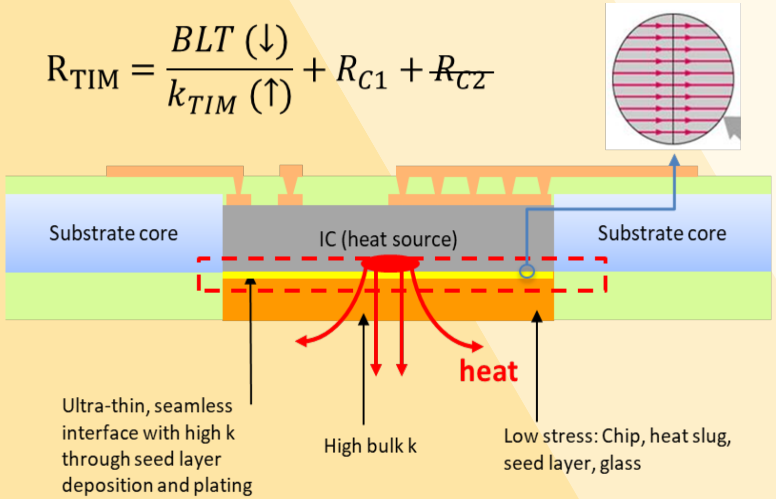


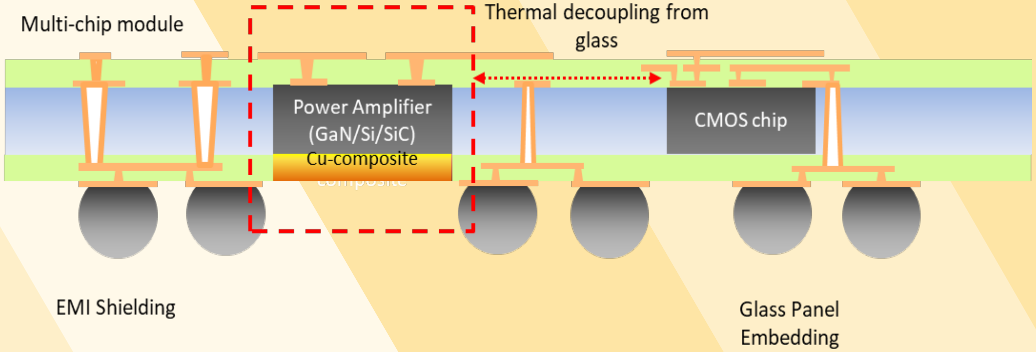
Margomenos, 2014

Thermal solutions are being placed extremely close to the die surface to minimize thermal resistance

5. Unique Approach

$$R_{TIM} = \frac{BLT\ (\downarrow)}{k_{TIM}\ (\uparrow)} + R_{C1} + \cancel{R_{C2}}$$





Key Innovations:

- Near-zero thermal interface resistance between chip and heat spreader though sputtering of ultra-thin film, conductive seed layer and electrodeposition processes
- Design of interface material properties and geometry for thermal and stress mitigation
- Integration into multi-chip GPE package with fine-line RDL, EMI shielding, and thermal decoupling using glass

Research Methodology:

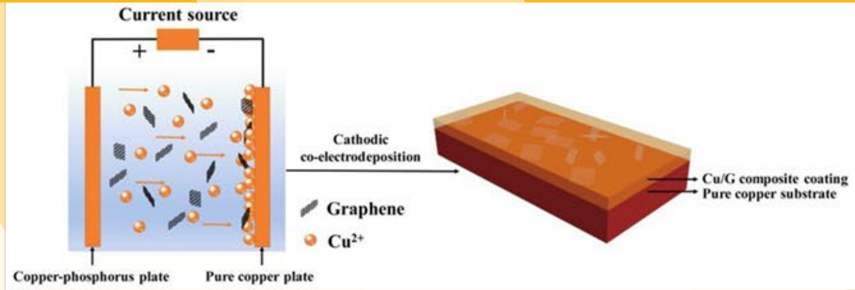
Transient, multi-physics modeling and design of interface to the chip (material properties and geometry) for low-stress and high thermal conductivity

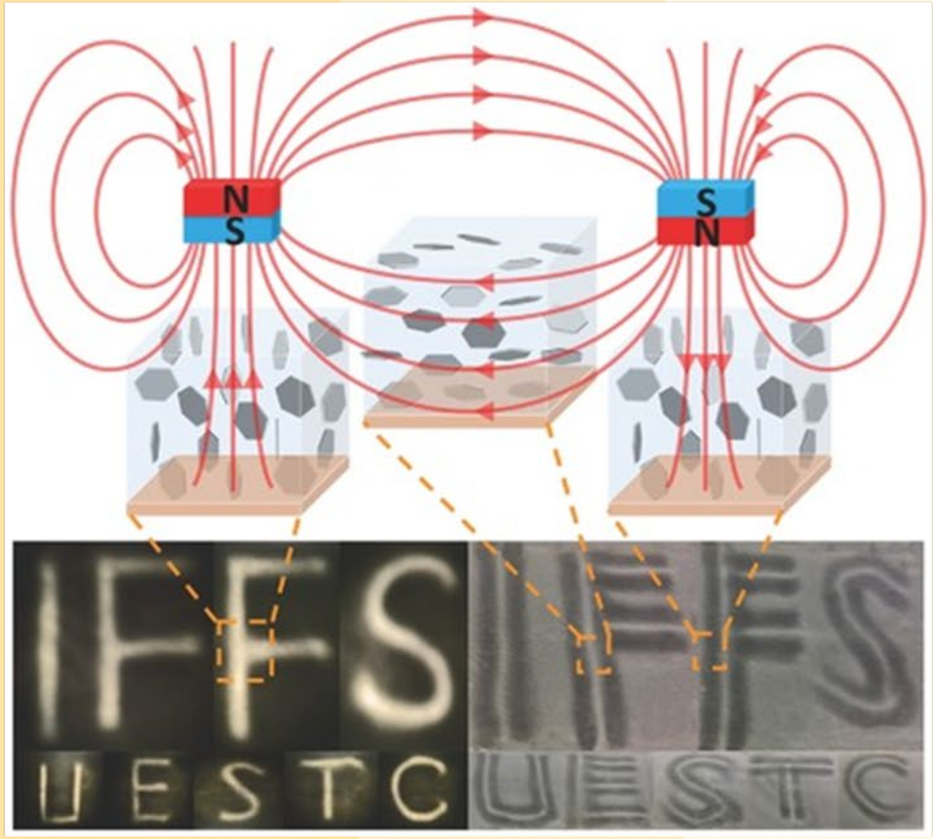
Design, demonstrate, and characterize material for low stress, high thermal conductivity, low thermal resistance interface between device and Cu heat spreader

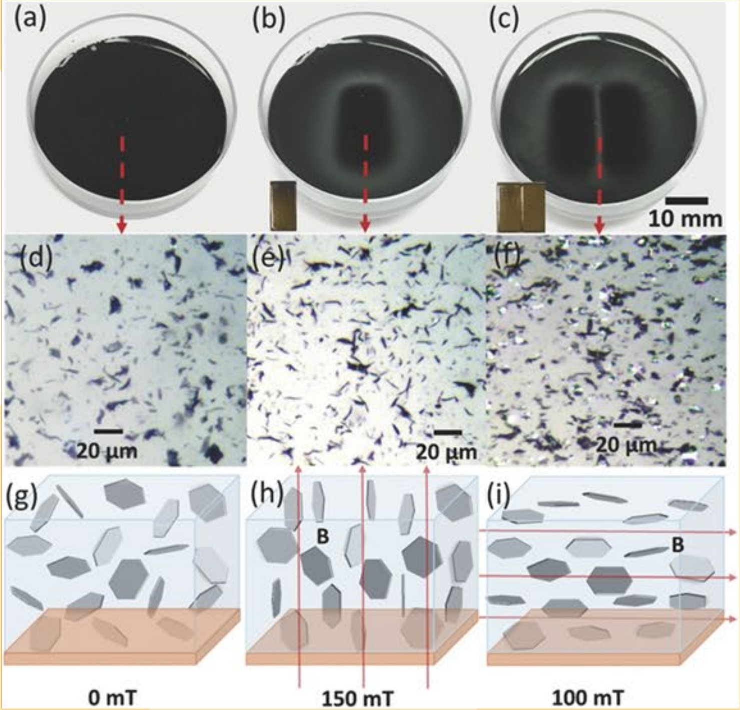
Integration of process in multi-chip, GPE module with fine-line RDL, EMI shielding, and thermal decoupling

5. Unique Approach (Cont.)

Aligned Electrodeposited Copper-Graphene Composites







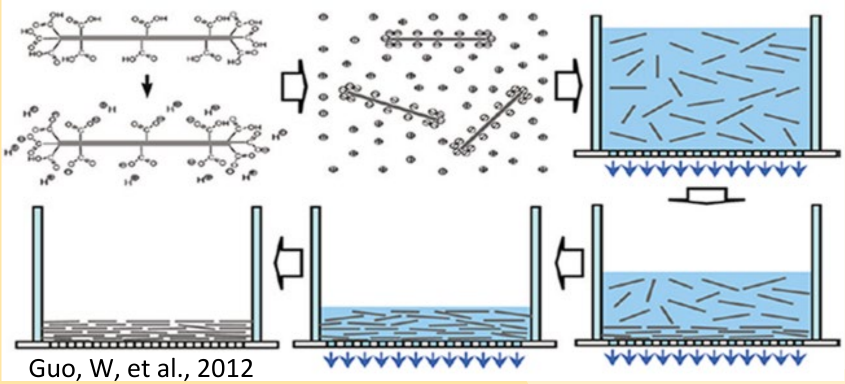
Lin, Feng, et al. "Orientation control of graphene flakes by magnetic field: broad device applications of macroscopically aligned graphene." *Advanced Materials* 29.1 (2017): 1604453.

- Exploring electrodeposition of magnetically-aligned Cu-graphene composites for high heat flux, low-CTE, low-stress heat transfer material

5. Unique Approach (Cont.)

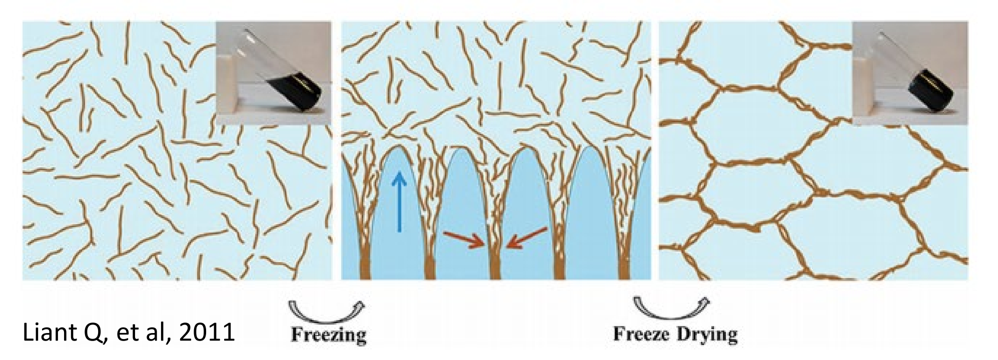
Alignment Methods for Graphene Composites

Vacuum Filtration Method



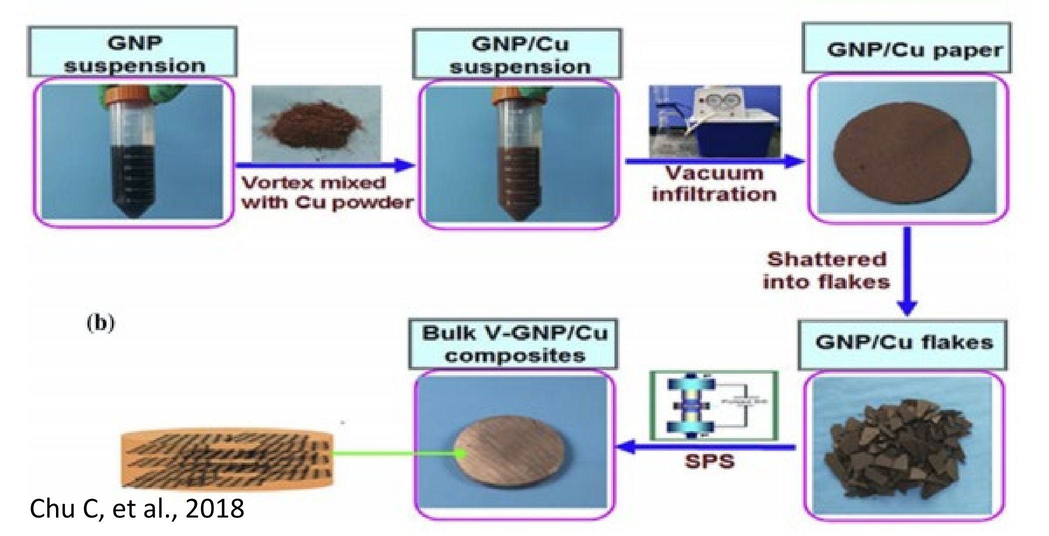
Guo, W, et al., 2012

Unidirectional Freeze-Cast Method



Liant Q, et al, 2011

Vacuum Filtration and Spark Plasma Sintering



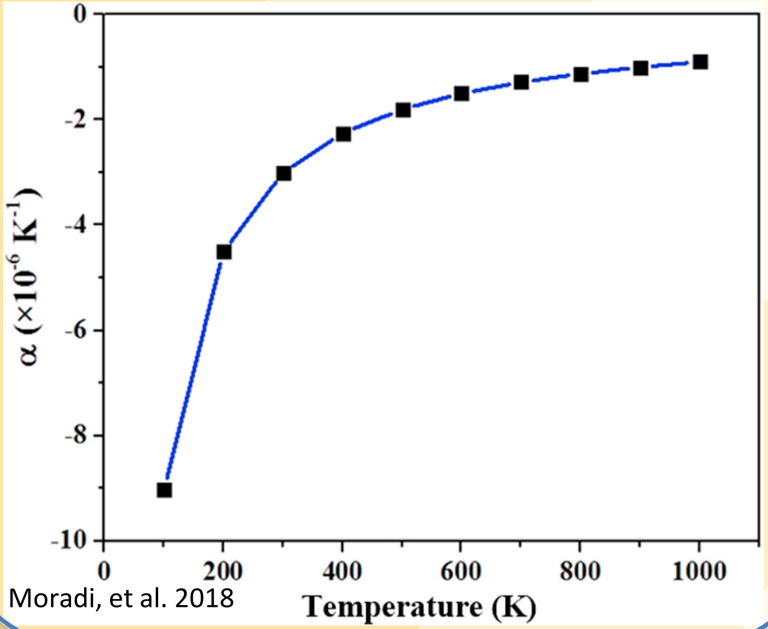
Chu C, et al., 2018

- Aligned graphene composites utilize the properties of graphene to max potential
- These alignment methods are not practical for electronics packaging

5. Unique Approach (Cont.)

Aligned Cu-Gr Composites

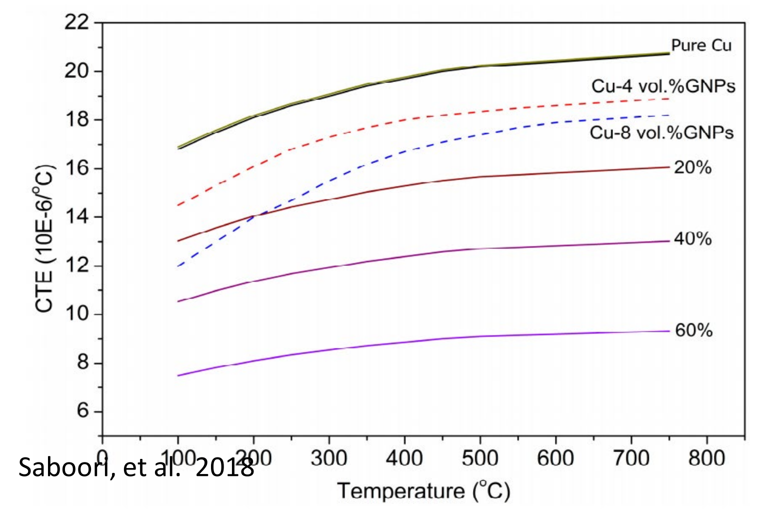
Graphene Exhibits Negative CTE



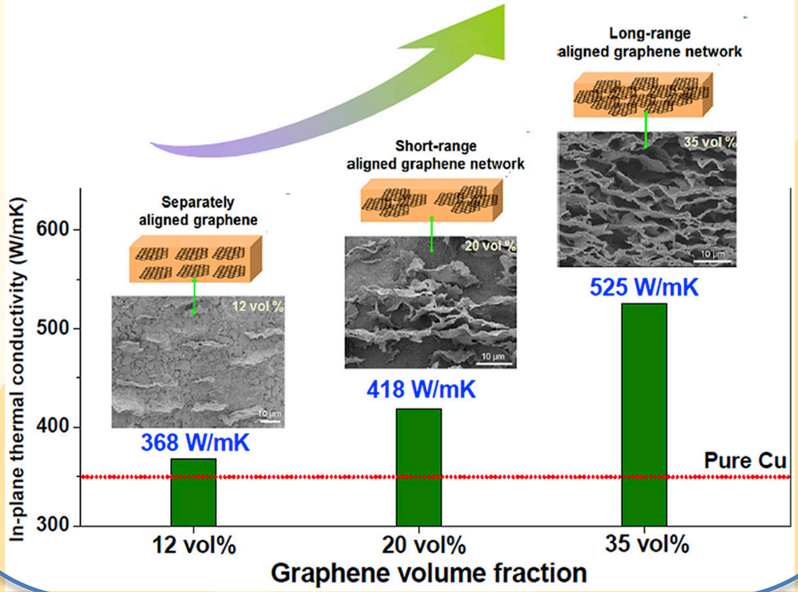
Moradi, et al. 2018

- Graphene can be used to enhance the thermal conductivity of copper
- Graphene (negative CTE) can be used to tailor the CTE within Cu-GR composite
- Aligning graphene within composite is critical to achieving theoretical values

Aligned Graphene enhances Cu CTE and Thermal Conductivity



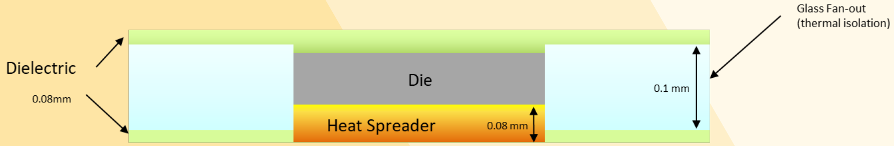
Saboori, et al. 2018



6. Results

Thermal and Thermomechanical Modeling: Geometry

Geometry Considerations for Thermal and Thermomechanical Model



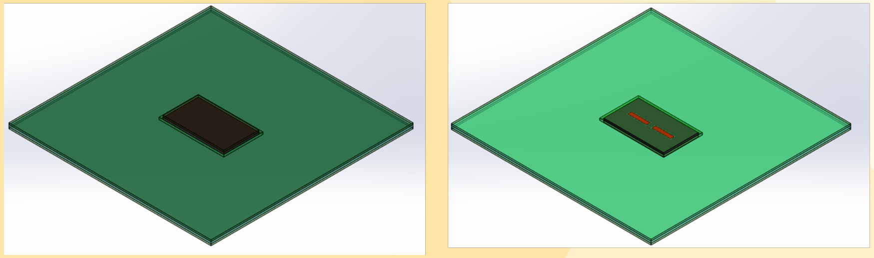
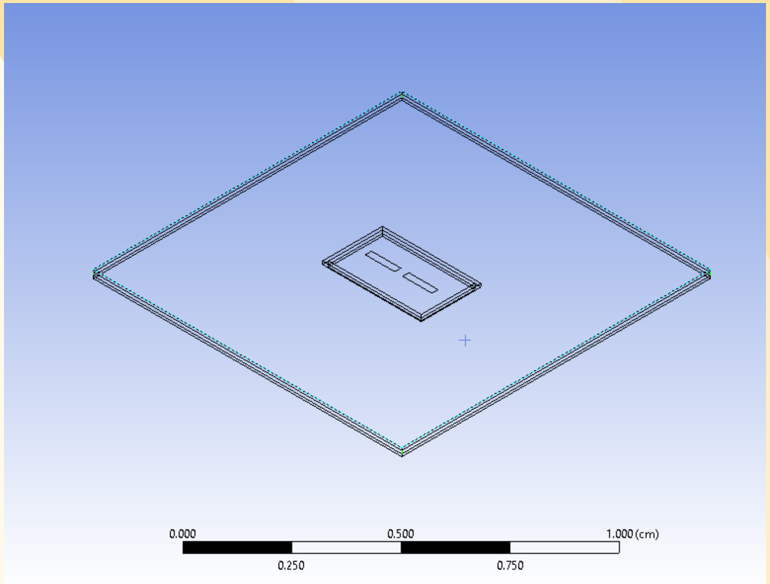


Image of chip embedded in cavity without dielectric layers:
Red bars denote locations of applied heat flux



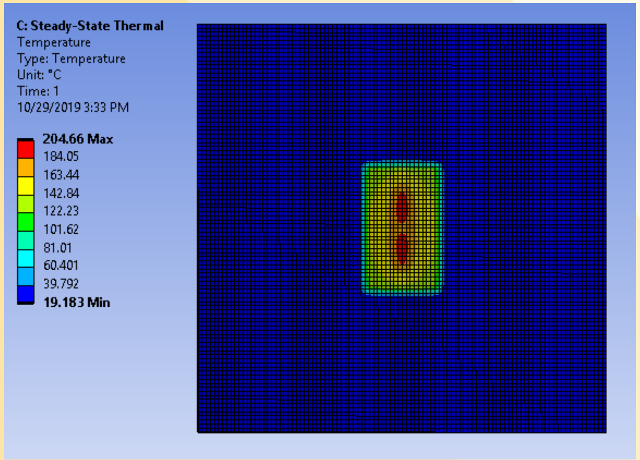
Wireframe figure of entire package to be modeled

- Embedded chip within glass panel
- Forced convection applied on backside of panel; natural convection applied to all other surfaces
  - Coefficients can be varied to emulate different external heat exchange methods
- Heat input applied to gate approximations on the die: 14.4W
  - This will be varied in the future to explore multiple scenarios
- Three case scenarios examined: no heat spreader, encapsulated die within dielectric, and directly bonded copper heat spreader

6. Results

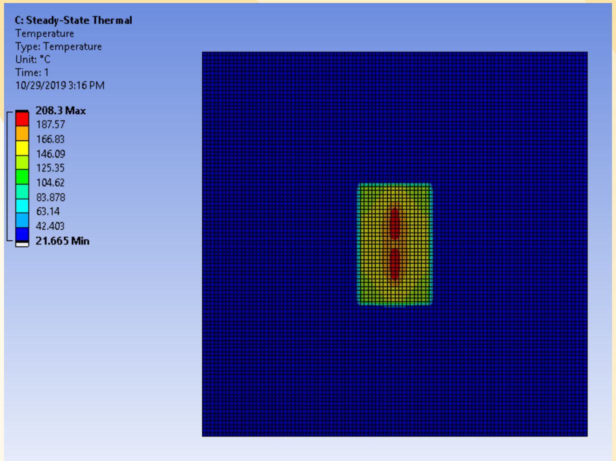
Thermal and Thermomechanical Modeling:

Chip Encapsulated in Dielectric



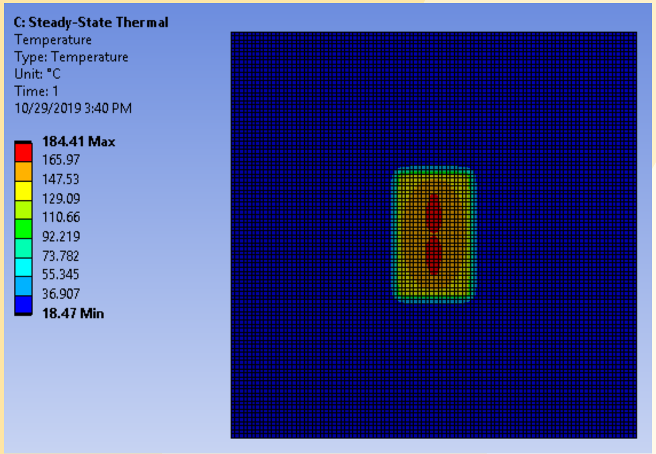
Max Die Temp: 204.66°C

Backside of Chip Exposed to Air



Max Die Temp: 206.3°C

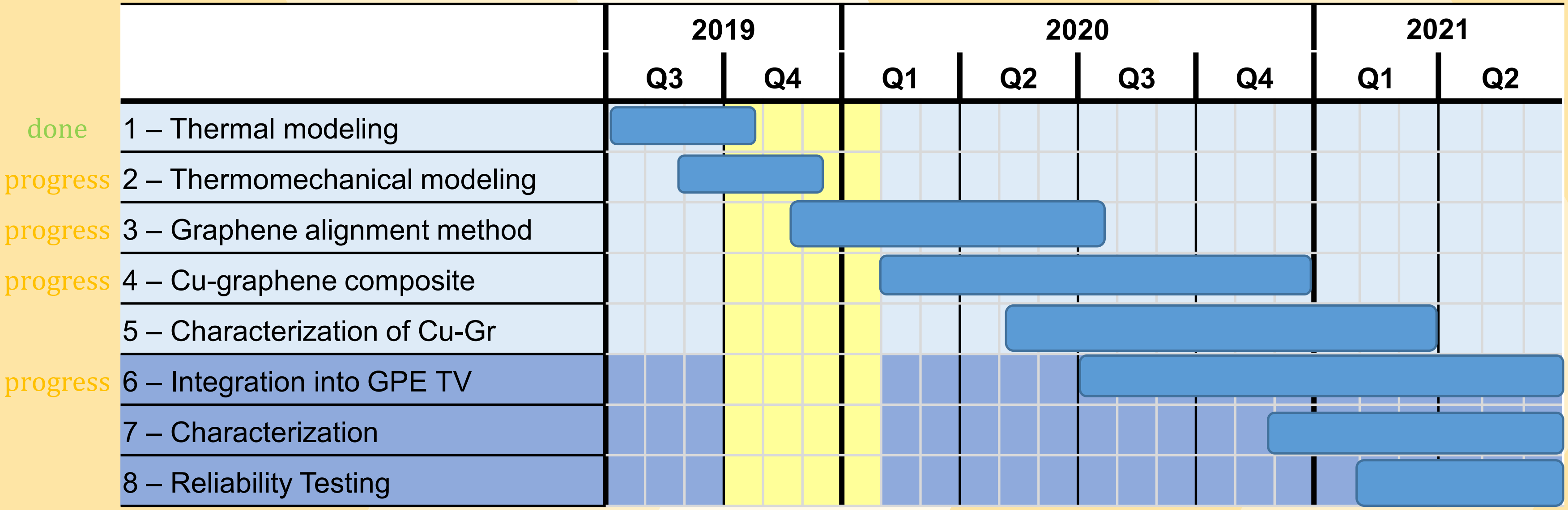
Direct-Bonded Cu Heat Spreader



Max Die Temp: 184.64°C

- Direct-bonded Cu heat spreader has ~20 - 25°C decrease in maximum die temperature over other scenarios
- Glass package keeps the heat isolated and localized within package – good for multi-chip packages
- Packages will be modeled to understand localized stresses

7. Schedule



Light blue: Material design
Dark blue: System design
Light Yellow: Current time window

8. Summary and Future Work

Summary

- Thermal analysis of glass-panel embedded package
- Proposal of magnetically aligned, electroplated Cu-Gr composites for low-CTE, high thermal conductivity, low thermal interface resistance

Future Work

- Thermomechanical analysis of glass-panel embedded package
- Demonstration of magnetically-aligned Cu-Gr composite material
- Integration of Cu-Gr composite material into GPE test vehicle
- Characterization and reliability testing of composite material