Sub-THz Wireless Modules using Organic Substrates

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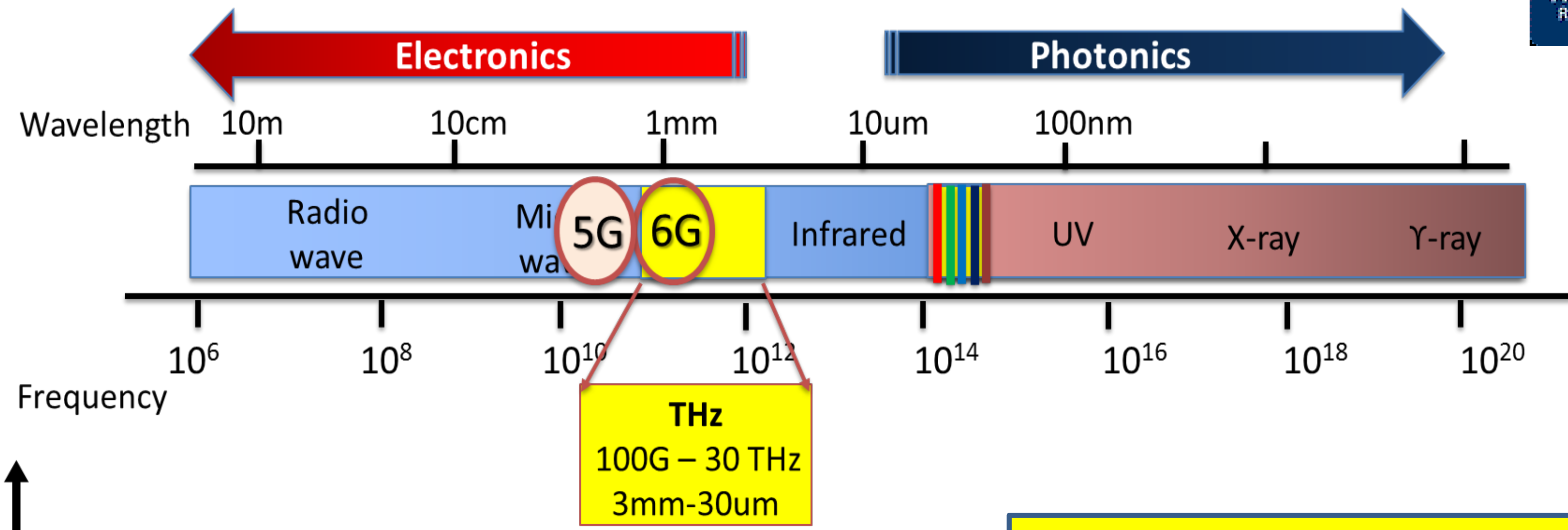
Outline

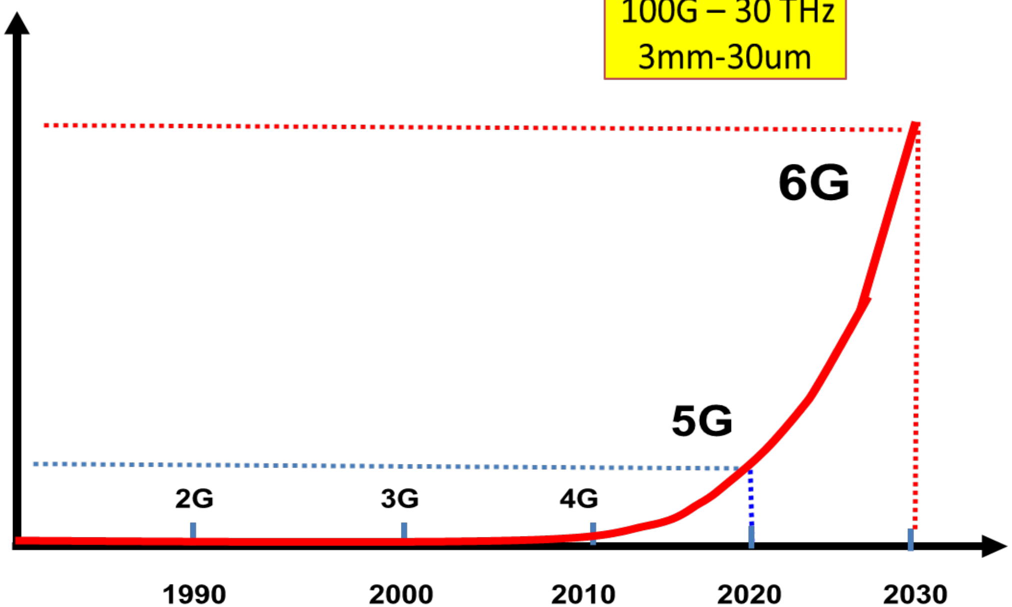
- Goals & Objectives
- State-of-the-arts
- Technical Approach
- Results & Key Accomplishments
- Comparison with Prior Art
- Schedule
- Summary

Goals & Objectives

- Explore low loss organic **laminates** and **dielectrics** for 6G application
- Develop the best suitable processes at low cost
- Material Characterization - Extraction of Dk and Df upto 170GHz
- Design, fabrication, testing and benchmarking→ Microstrip Lines, CPWs, SIWs etc (ultra-thin and miniaturization)

What is 6G?



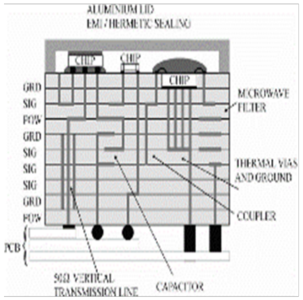


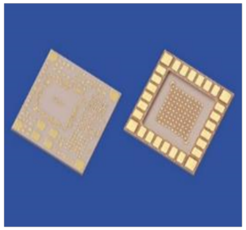
6G will provide an

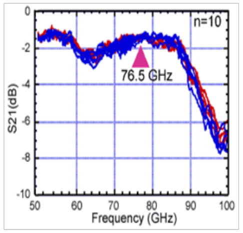
- **Ultra high speed**
- **Ultra low delay/high response (μ-second)**
- **Wireless interconnection platform**

State Of the Art

Ceramic (LTCC)







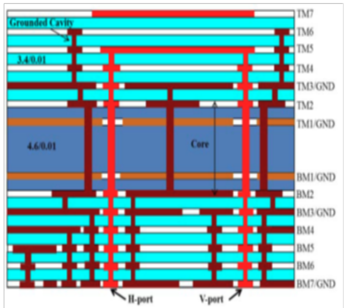
KYOCERA

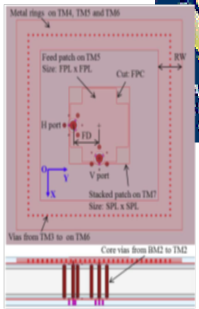
Insertion loss of full link ~3dB at 60 GHz

- ❑ **Thickness: Large**
- ❑ **System Component Density: Low**
- ❑ **Thermal: Flip Chip/Thermal Vias**

Low-loss Laminate

IBM



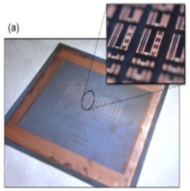


- 3 dBi/element
- Buildup: Dk=3.4, Df=0.01

- ❑ **Thickness: Medium**
- ❑ **System Component Density: Medium**
- ❑ **Thermal: Flip Chip/Thermal Vias**

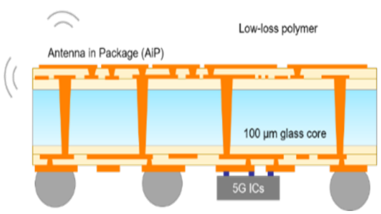
Fanout PLP Glass Substrates

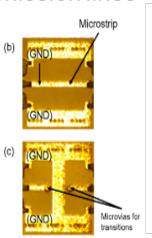
Georgia Tech

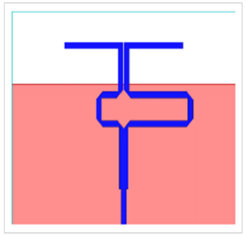


Low-loss transmission lines

Yagi-Uda antenna





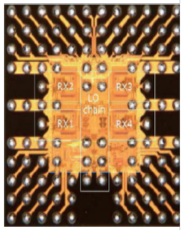


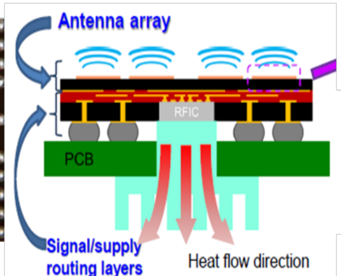
- ❑ **Thickness: Ultra-thin (Fine RDL)**
- ❑ **System Component Density: High**
- ❑ **Performance: High**
- ❑ **Double Sided**
- ❑ **Thermal: High thermal conductivity interfaces**

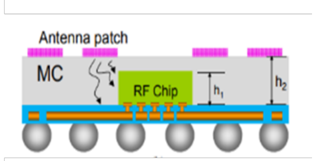
Fanout WLP

infineon

tsmc







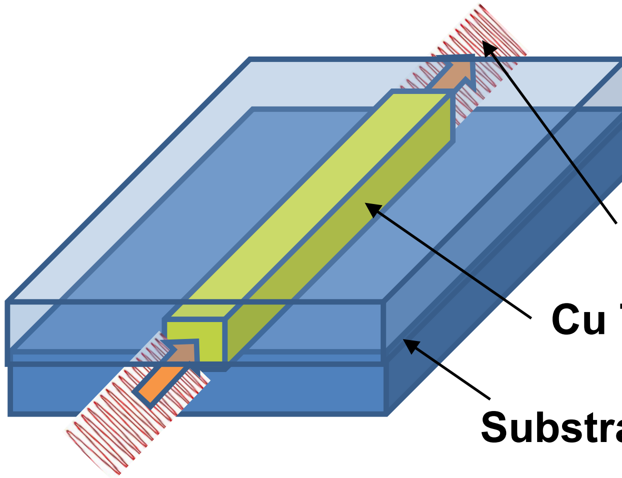
- ❑ **Thickness: Thin (Fine RDL)**
- ❑ **System Component Density: High**
- ❑ **Performance: Limited**
- ❑ **Single Sided**
- ❑ **Thermal: Limited by TIM**

M. Swaminathan et al, IMS Workshop, 2019

Strategic needs

(1) Low loss interconnects
- – Ultra Low Loss Organic materials
- - Precise and smooth conductive traces

(2) Low cost large panel process
(3) Thin & compact, and
(3) Cost low

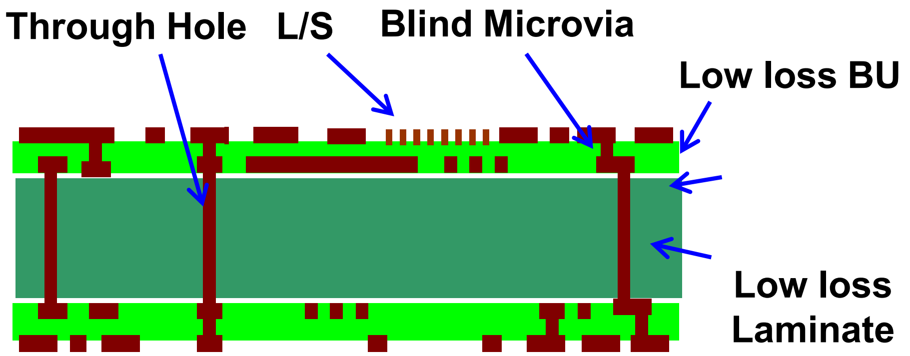


Ultimate dielectric: air, ε = 1, Df ~ 0

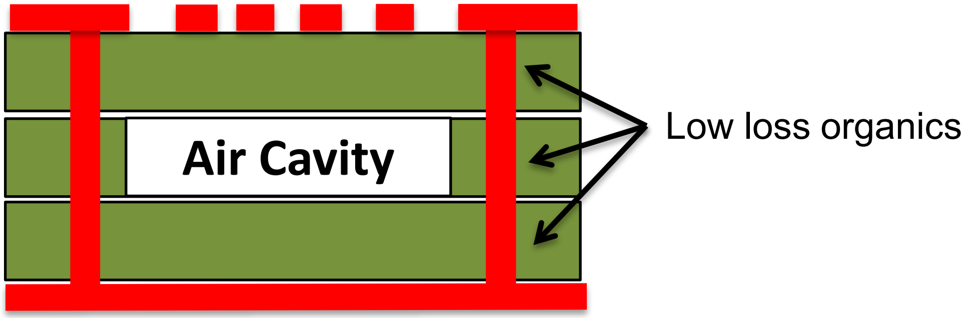
Technical Approach

1) Multilayer stackup without air cavity

- Low loss laminate core
- Low loss thin dielectric layer
- Small footprint (fine L/S/vias)
- Small TPV
- High definition features
- Smooth copper surface



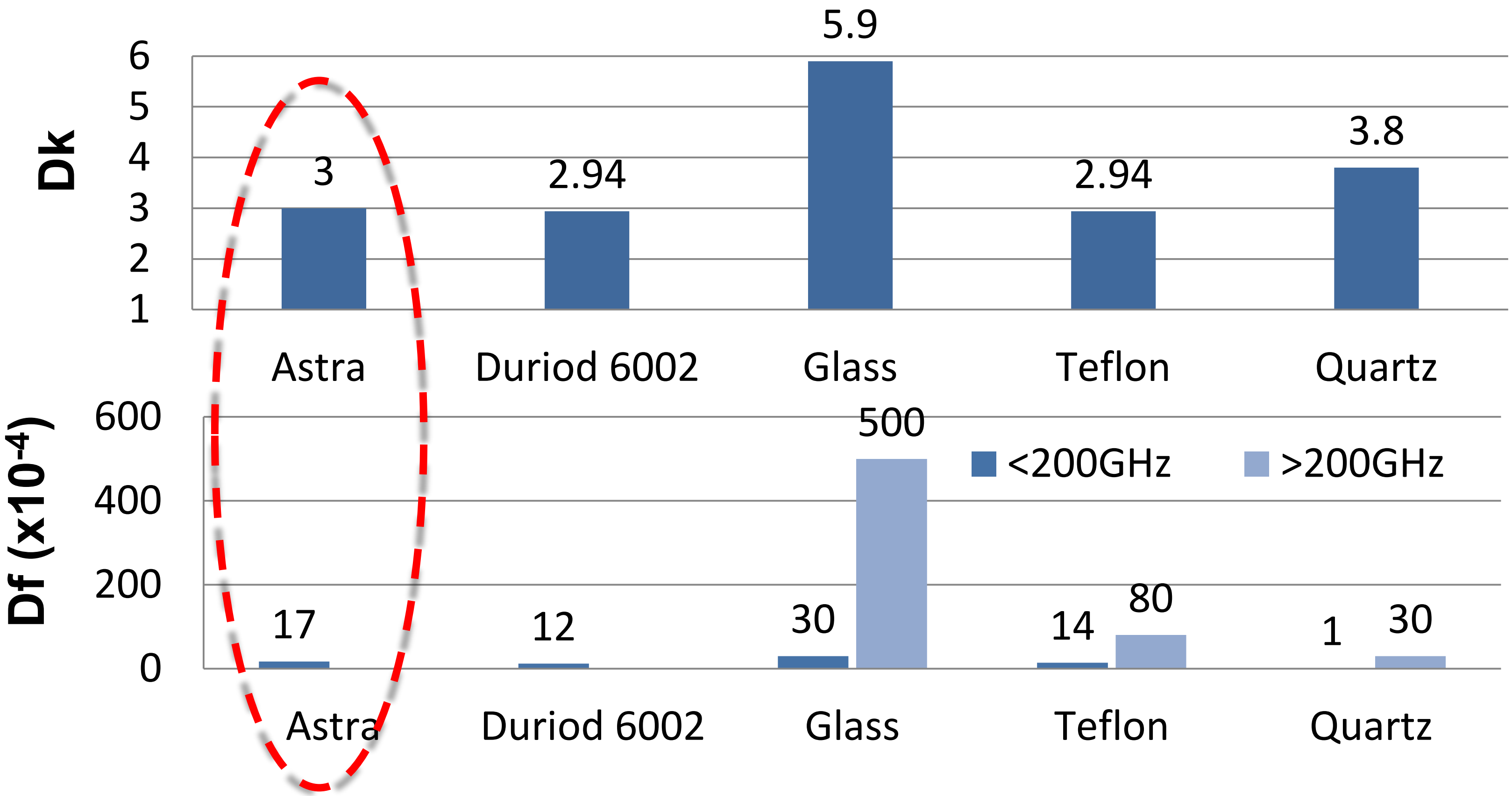
2) Air cavity integration



Challenges @ THz

- Low dielectric constant and low tangent materials
- Cu surface roughness (Skin Depth = 0.19 μm @ 140 GHz)
- Fine line fabrication and precise dimensional control
- Air cavities with quality control

Materials Exploration: Laminates

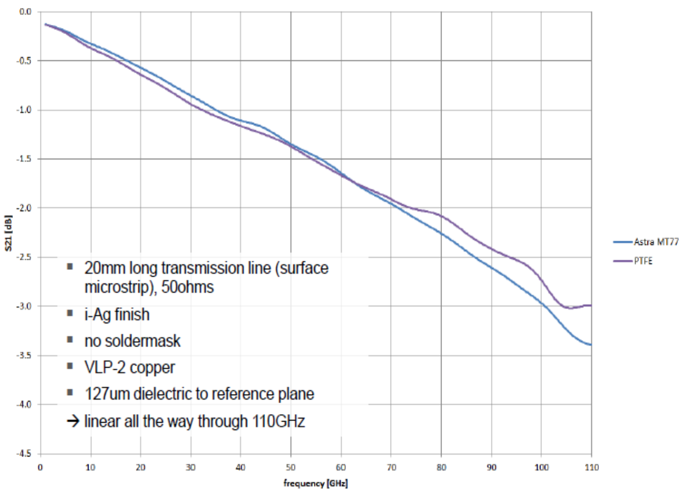


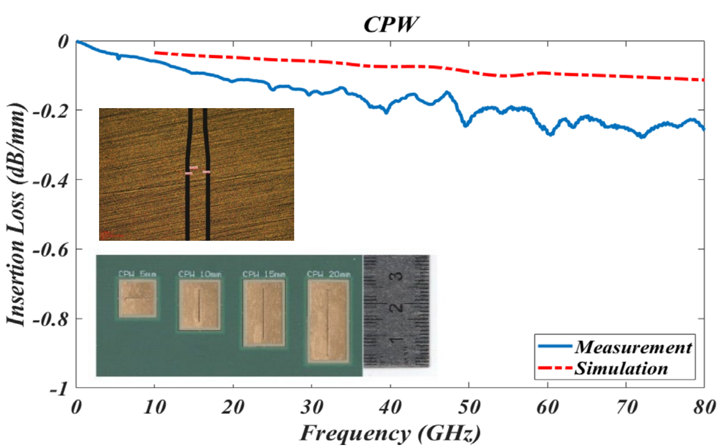
- Quartz, Teflon, Duroid 6002 – Cost, Process difficult
- Glass – loss at high frequency
- Astra (Isola) - property similar to Teflon, use standard PCB process

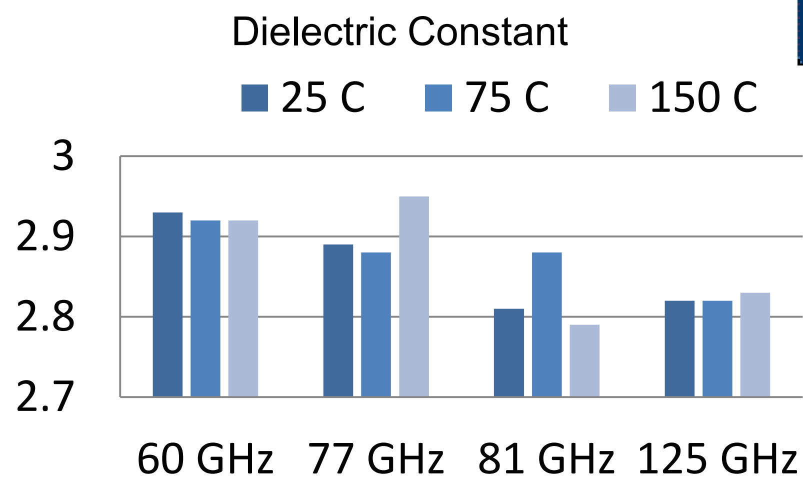
Properties of Astra

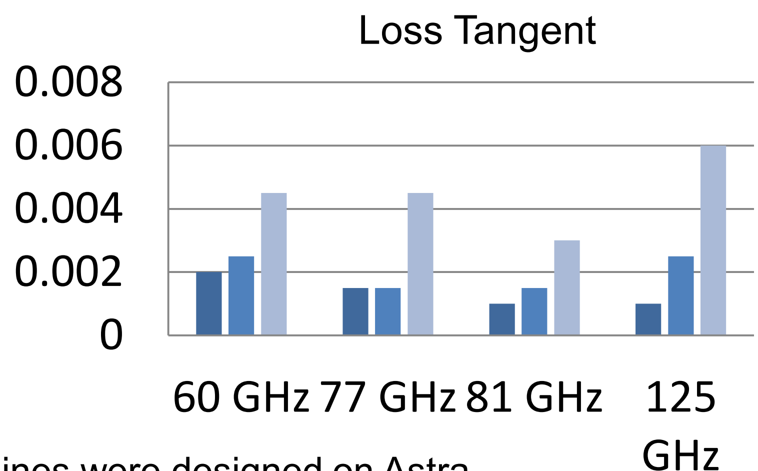
- Replacement to Teflon
- Stable Dielectric Constant and loss tangent
- Easier processing

Insertion Loss Comparison of Teflon and Astra









- CPW Lines were designed on Astra
- Insertion Loss : 0.25dB/mm at 80GHz
- Further Characterization on the way

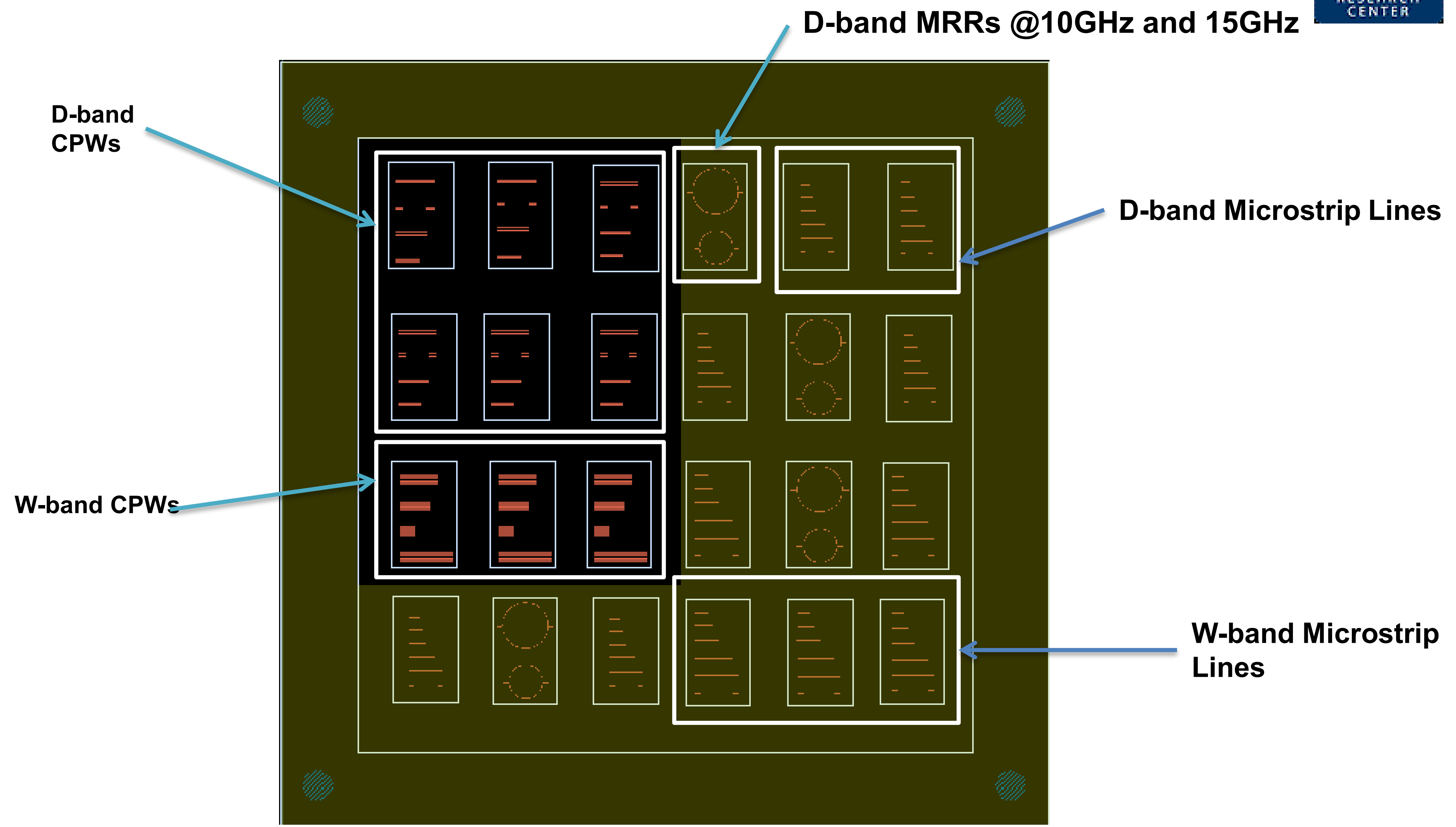
Source: Isola

Materials Exploration: Dielectric thin film

Zaristo thin Dry Film from Taiyo Ink

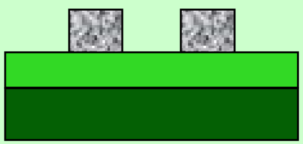
Test Items	Unit	Zaristo 125	Zaristo 517X	In development
Tg (TMA)	^{0}C	165-175	165-175	
CTE	ppm	25-30	17	
Young/s Modulus	GPa	7-8	11-12	
Dk (10GHz)		3.4	3.4	
Df (10GHz)		0.015	0.004-0.005	0.0025
Ra (after desmear)	um	0.25-0.40	0.2-0.25	
Peel test	N/cm	>5.0	4.0	

Test Vehicle for W-Band and D-band Characterization



Development of the best Patterning and Metallization process for low cost high performance mm-wave circuits

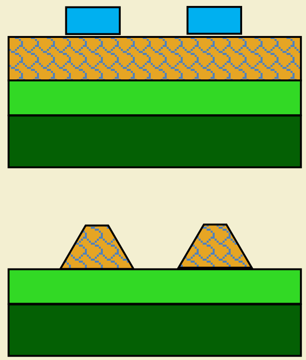
1. Printing



- Conductive ink or paste
- Screen or Inkjet

Cheap
L/S ~ 50 um
Ink or paste
Resistance high
Quality low

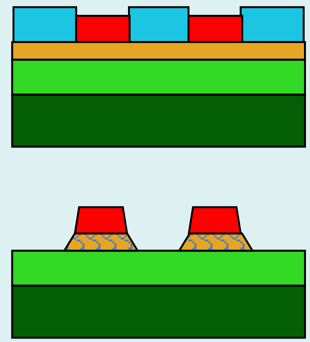
2. Subtractive



Chemical Etch

Cost low
L/S ~ 40 um
Cu Foil
Trapezoid
Rough Cu Foil

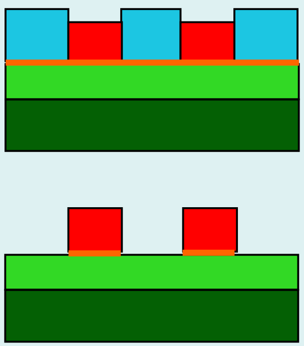
3. m-SAP



Modified-SAP w/thin Cu foil

Cost mid
L/S ~ 20 um
Cu Foil + Plating
Micro etching
Quality: mid

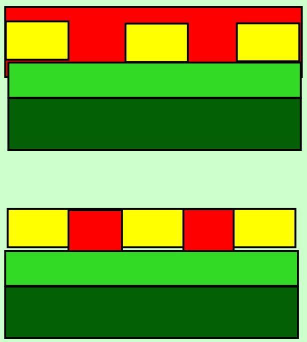
4. Semi-Additive Process (SAP)



Seed Layer & Pattern Plating

Cost high
L/S ~ 10 um
Plated Cu
Micro etching
Quality: good

5. Organic Damascene

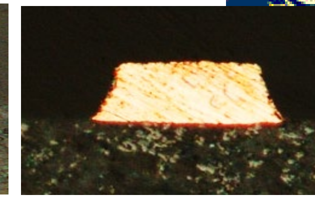


Trench & plating

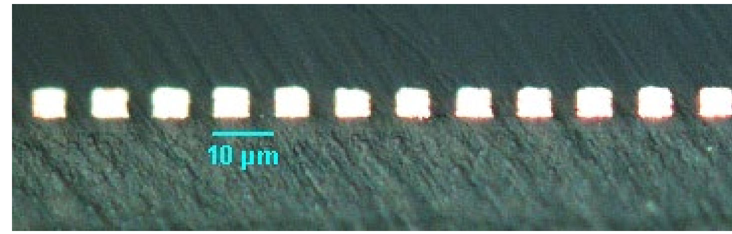
Overburden removal

Cost mid-high
L/S ~ <10 um
Plated Cu
Overburden
Quality: high

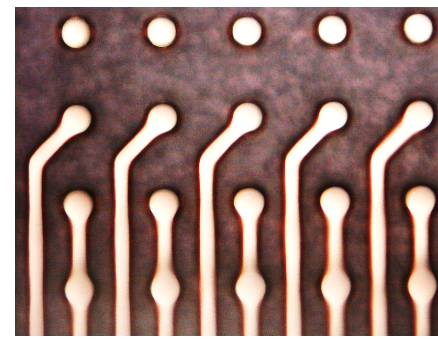
Capabilities



- Print & Etching (40 µm) – standard copper foil and profile free copper

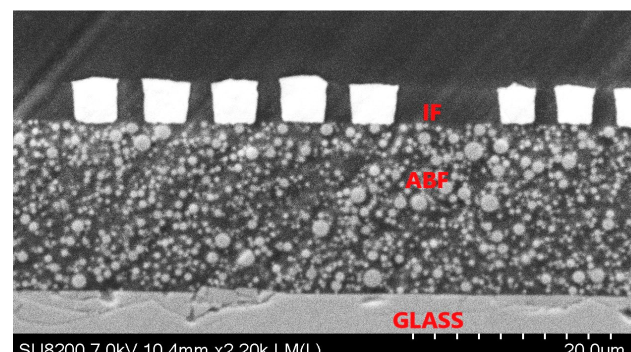


- SAP - 5 µm L/S on smooth dielectric layer



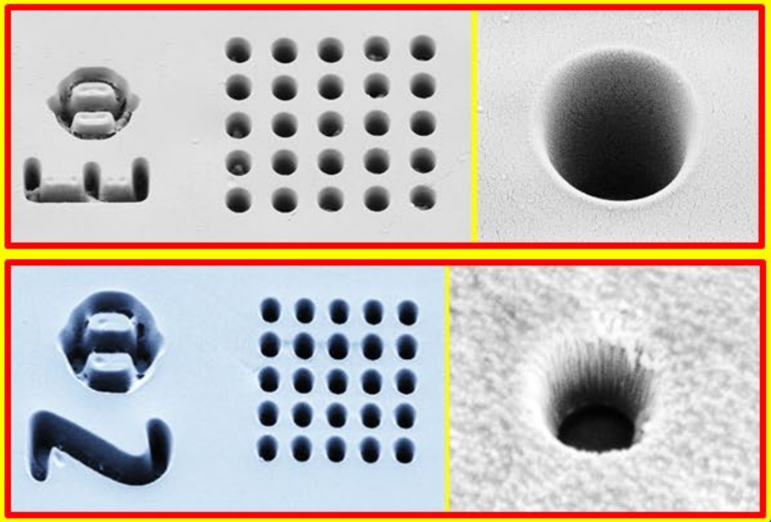
- Plated copper traces (10 µm) with smooth surface

Organic Damascene (2.5-3.0 µm)

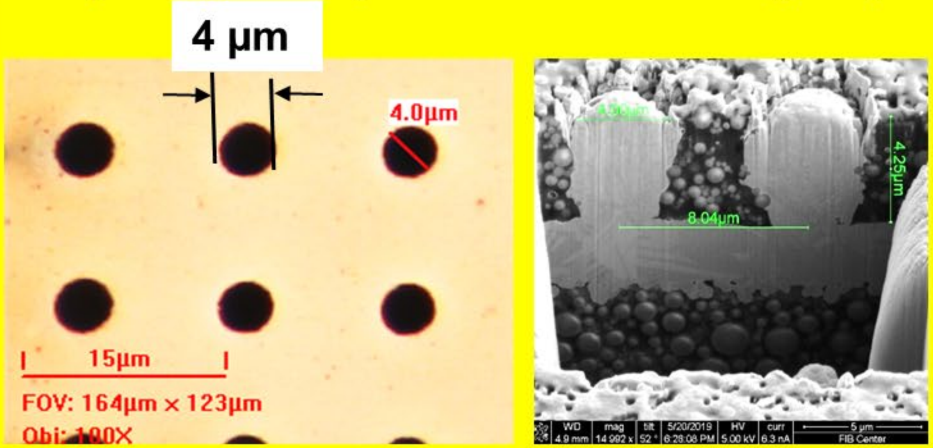


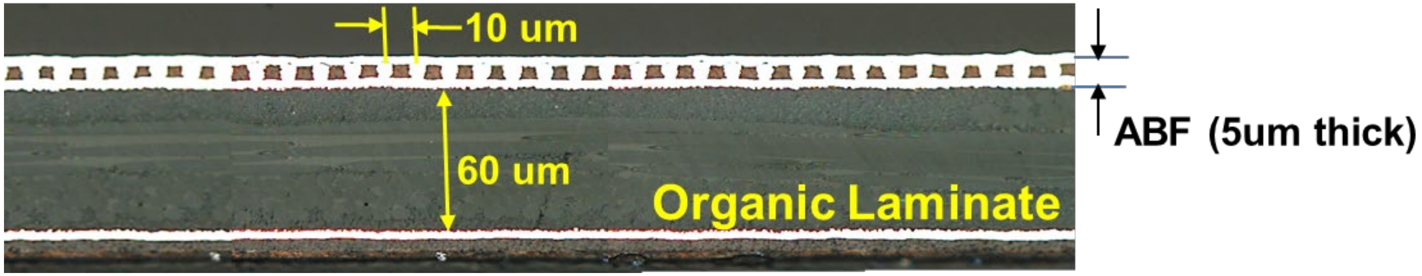
Capabilities: Microvia technologies

Photovias in TOK's PID (2 & 3 µm)

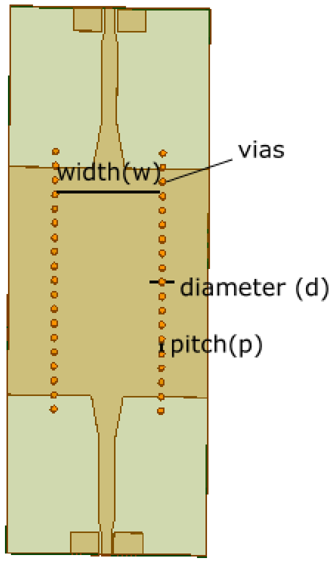


Picosecond UV laser Vias in Ajinomoto's ABF (4 µm dia. 8 µm pitch, SOA – 20/50 µm)

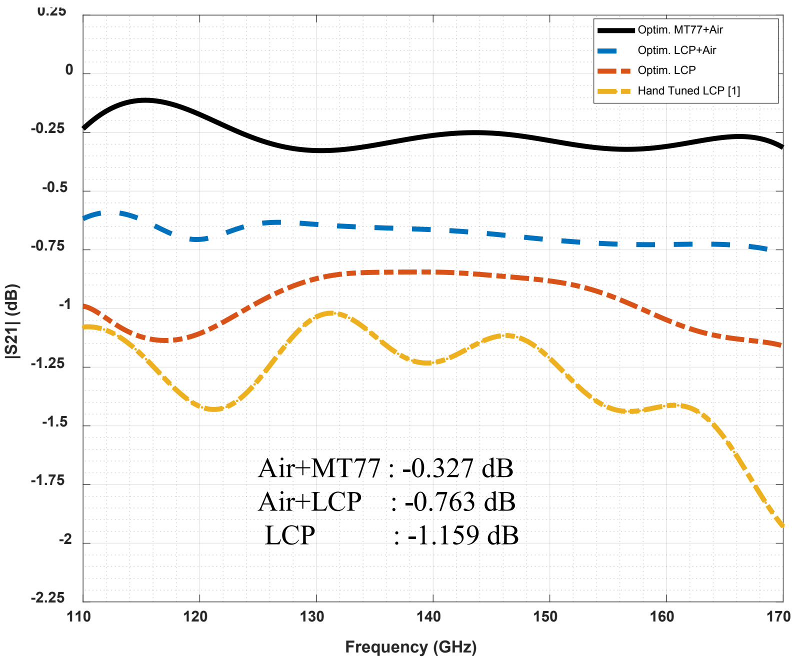




Substrate Integrated Waveguides (SIWs)



- Microstrips & CPWs → performance limitations @ high frequencies
- SIWs →promising alternative
- Can be used as the basic building block for all passive components
- Fundamental Limitation→ Material's loss tangent, surface roughness

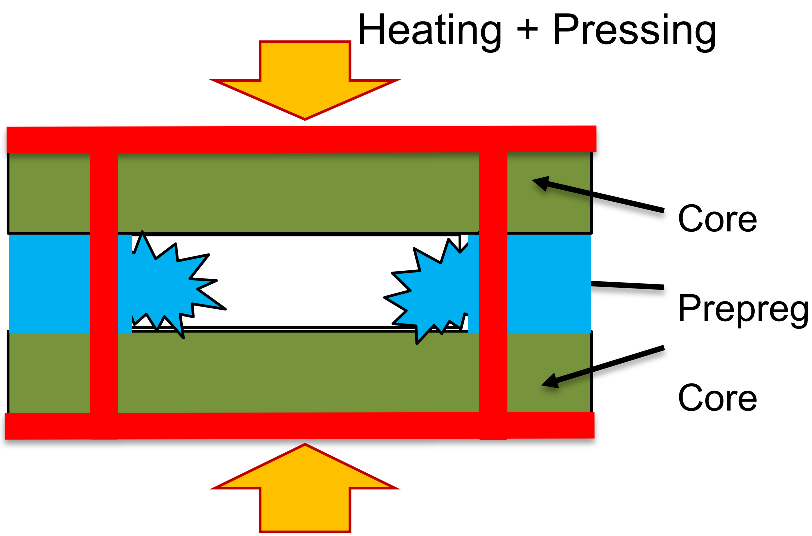


- Air → Best dielectric constant
- Using air filled cavities within laminates stack up can enhance performance of SIWs
- Precise formation of air cavities is essential

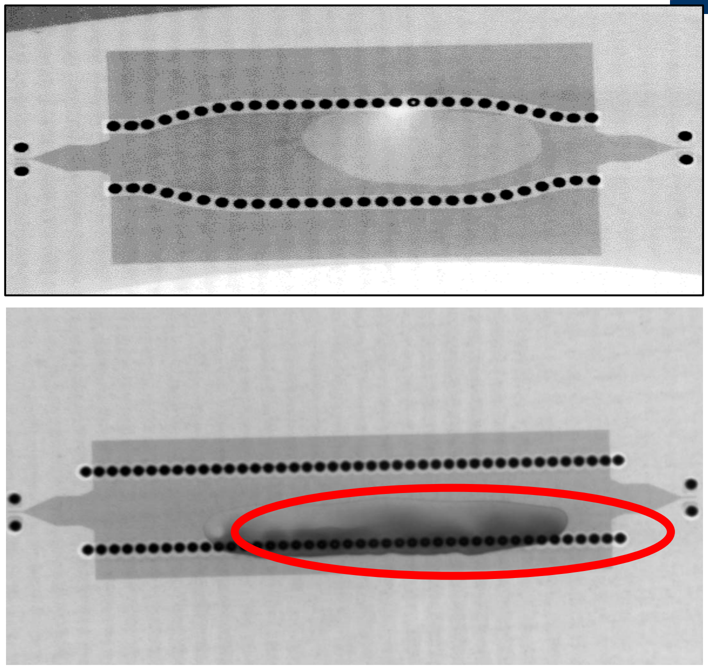
Material Stack Up

H. M. Torun and M. Swaminathan, "High-Dimensional Global Optimization Method for High-Frequency Electronic Design," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 6, pp. 2128-2142, June 2019.

Air Cavity Integration Challenges



Standard multi-layer board (MLB) process challenges



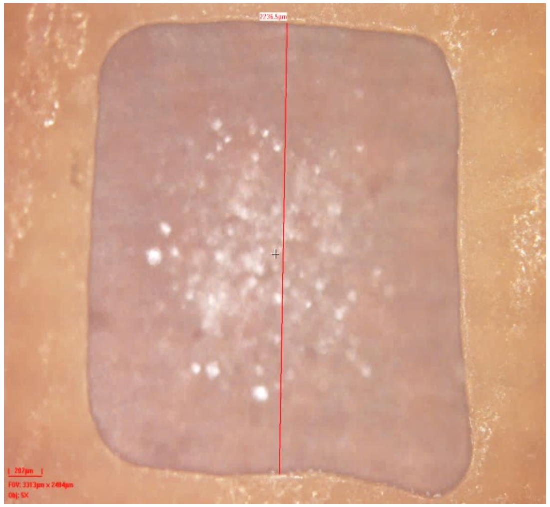
SIW with air cavity fabricated by Vendor company

- ❑ Shape of the cavity is deformed
- ❑ Placement of the cavity is not precise
- ❑ Vendor processes are unable to cater this sort of designs
- ❑ ***In house process development is essential***

Preliminary Results

Cavity drilling and comparison

- Material: Astra laminate 63um thick with 20um thick copper foil on both sides
- Femtosecond laser, 4 W power
- Cavity Size: 2000um x2000um square



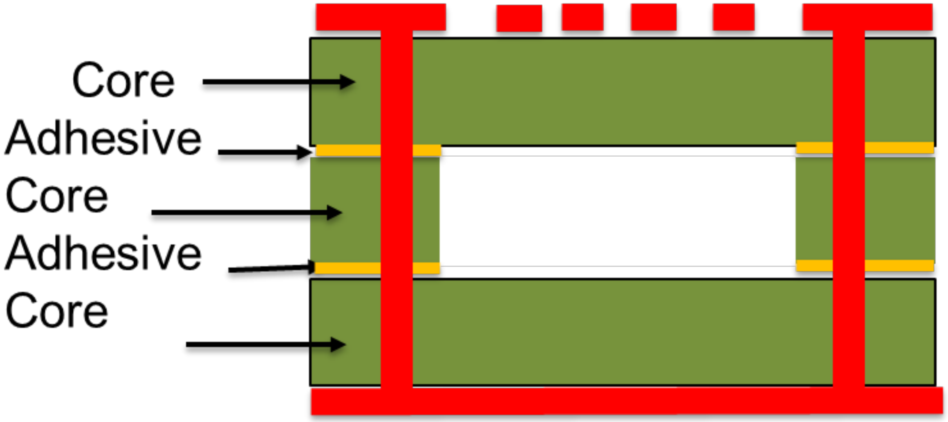
Mechanical drilled, non-uniform

Femtosecond laser drilled, precise

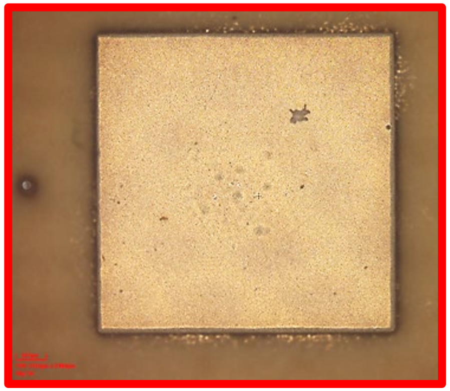
Preliminary Results

❑ Modified Fabrication Process

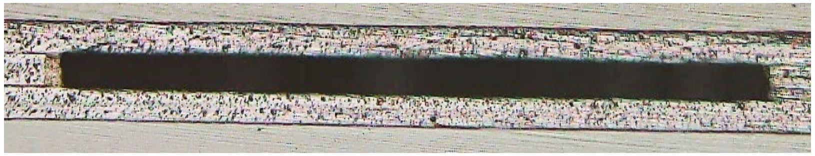
- Use laminate core replace prepreg
- Use thin adhesive layer (5 μm dielectric) for bonding
- Laminate them together
- Curing in an Oven at 180 ^{0}C for 1 hour



Modified stack-up for cavity fabrication

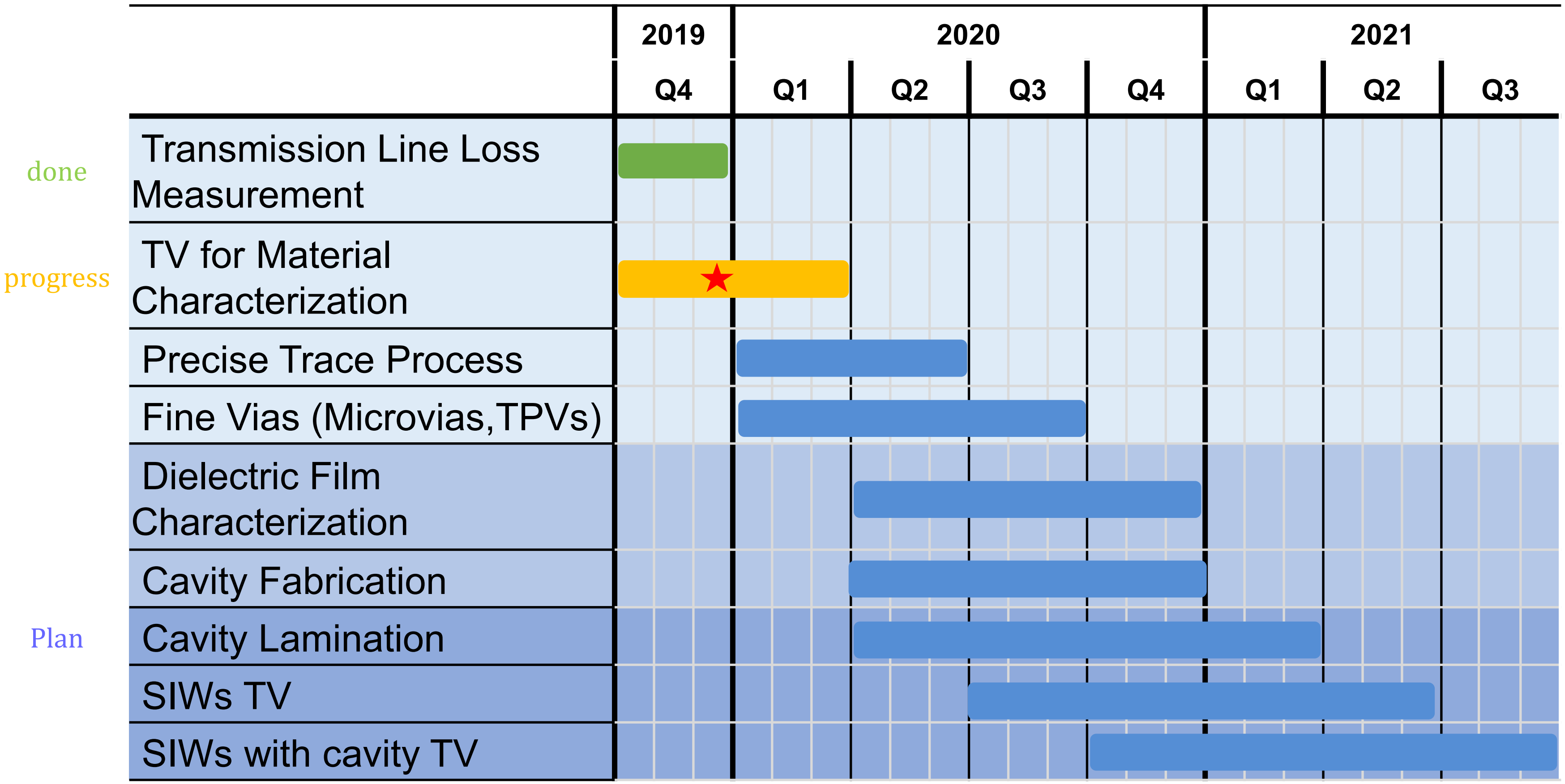


One side cavity (top view)



Double sides cavity laminated (Cross section)

Schedule


2019
2020
2021
Q4
Q1
Q2
Q3
Q4
Q1
Q2
Q3
done
Transmission Line Loss Measurement
progress
TV for Material Characterization
Precise Trace Process
Fine Vias (Microvias,TPVs)
Dielectric Film Characterization
Cavity Fabrication
Plan
Cavity Lamination
SIWs TV
SIWs with cavity TV

Summary

- Next Generation Radios

  High Data Rates→ Sub-THz Carrier Frequencies (140GHz,220GHz,340GHz etc)

- Use of low loss materials→ Critical

  Our choice : Astra (Df=3.0, Dk=0.0017)

- Measured Insertion Loss **0.25dB/mm at 80GHz**
- Test Vehicle for Material Characterization

  Microstrips, CPWs, Ring Resonators

- Process development for precise air cavity fabrication

  Femtosecond laser cut cavities