Photonics in the Package for Extreme Scalability in Heterogeneous Systems

Faculty: Ali Adibi

Students: TBD

Outline

- ☐ Goals & Objectives
- ☐ Prior Work
- ☐ Technical Approach
- ☐ Results & Key Accomplishments
- ☐ Comparison with Prior Art
- ☐ Schedule
- ☐ Summary

Goals and Objectives

- ☐ **Goal:** Develop an ultrafast monolithic optical link for optical interconnection between chiplets in module using individually modulated comb signals in the hybrid Si/SiN/III-V material platform.
- ☐ **Vision:** Combine wide bandwidth, fast dynamics, and robustness of optical frequency combs with fast low-power modulation techniques in miniaturized CMOS-compatible integrated nanophotonic structures to form optical links on a single substrate with ultra-high data rates.
- ☐ **Major Building Blocks:** The proposed research builds on extensive developments in 1) high-quality hybrid CMOS-compatible material and device platforms and novel techniques for realization of low-power high-speed modulators, 2) realization of wideband frequency combs in CMOs-compatible platforms, 3) state-of-the-art glass interposer packaging technology at PRC.
- ☐ **Enabling Technology:** The proposed platform addresses the major interconnection needs of system on package (SoP) while providing potential solutions for chip-to-chip, board-to-board, and rack-to-rack in terms of data rate, power consumption, and bit density.

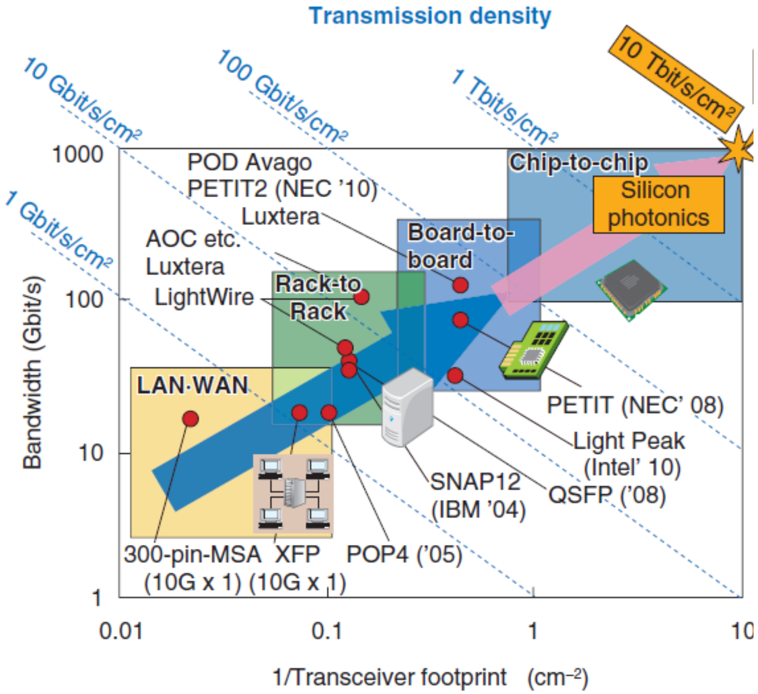
Prior Work: Application of Si Photonics

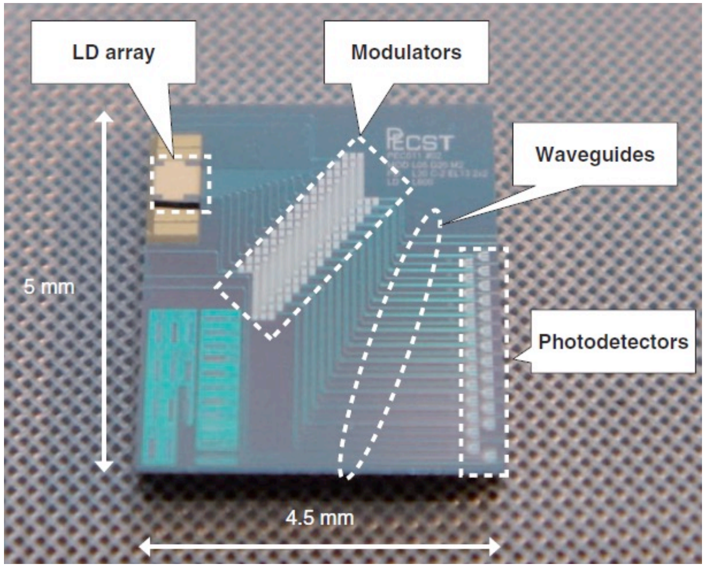
☐ **Optical links and interconnects**

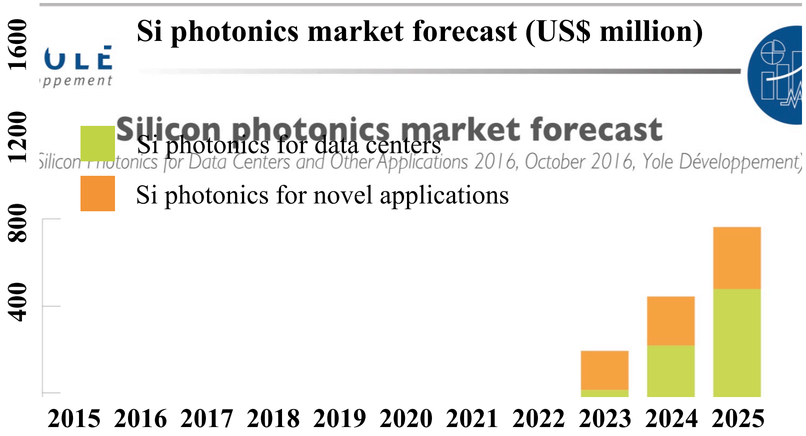
☐ Computing, Lidar, sensing

☐ **Trends**

- Size and density
- Power efficiency
- Bandwidth and speed
- Cost

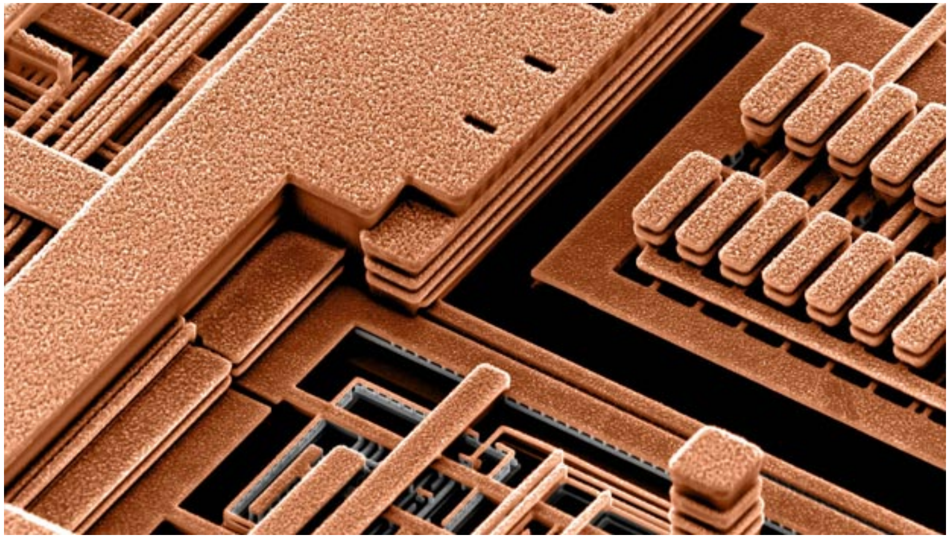





Si photonics market forecast (US$ million)

Optical Interconnects

- ☐ Challenge: Interconnection accounts for a large portion of power consumption in data centers and multi-core processors
- ☐ Need for lower power, higher speed communications and higher information density
    - ☐ Low power, high-speed modulators
    - ☐ Low-power, fast switching for signal routers



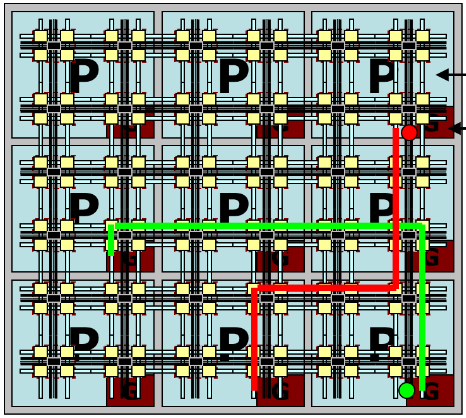
www-03.ibm.com/ibm/history

https://computing.llnl.gov/tutorials

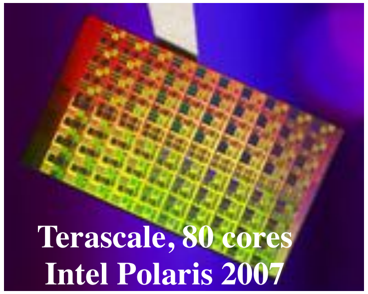
Optical Interconnect: Requirements

- I/O Bandwidth density >> 11 Pbps/cm^2
- High-capacity optical router
- Modulation
  - Operation voltage < 1V
  - Power consumption 1-10 fJ/bit
  - Speed > 50GHz
  - Multiplexing through WDM
- Optical routers
  - Wideband tuning for channel switching
  - Fast (< 10 ns) for packet switching

Optical interconnection for Data centers

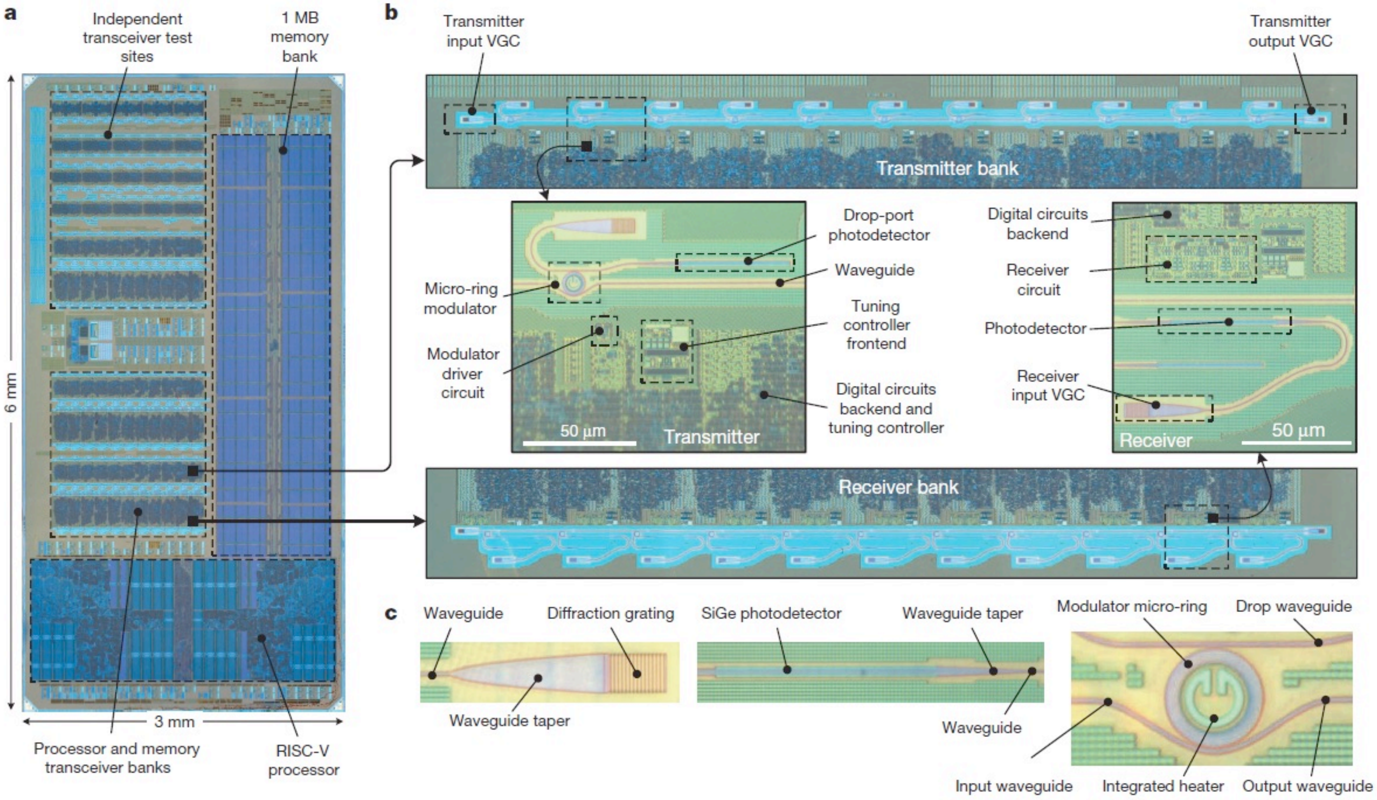


Processing Core
(on processor plane)
Gateway to Photonic NoC
(between processor & photonic planes)

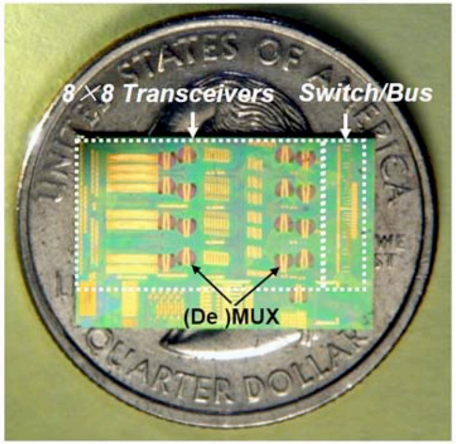


Optical interconnection for multi-core processors

Si Photonic Interconnect



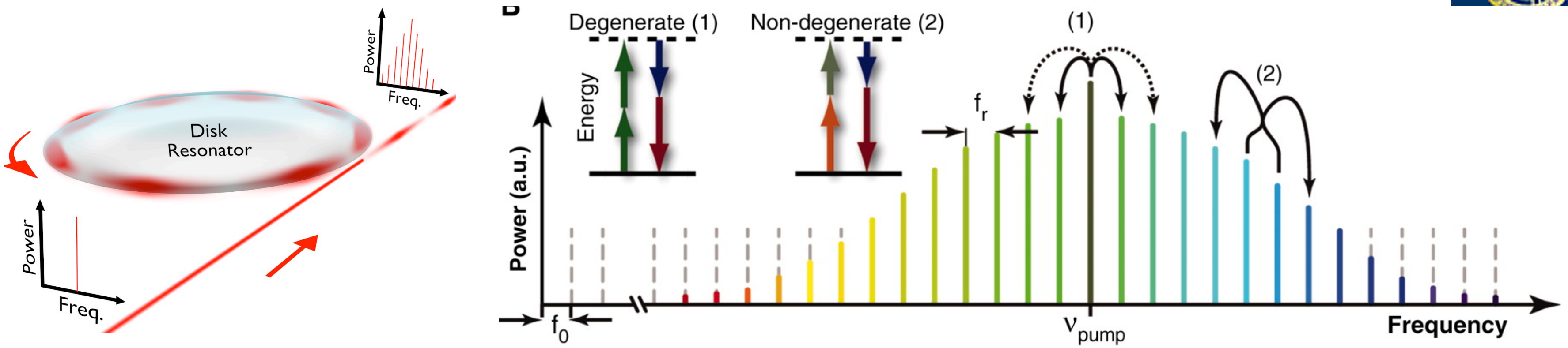
Sun et al., Single-chip microprocessor that communicates directly using light, *Nature* (2015)



Zhang et al., 8 × 8 × 40 Gbps fully integrated silicon photonic network on chip, *Optica* (2016)

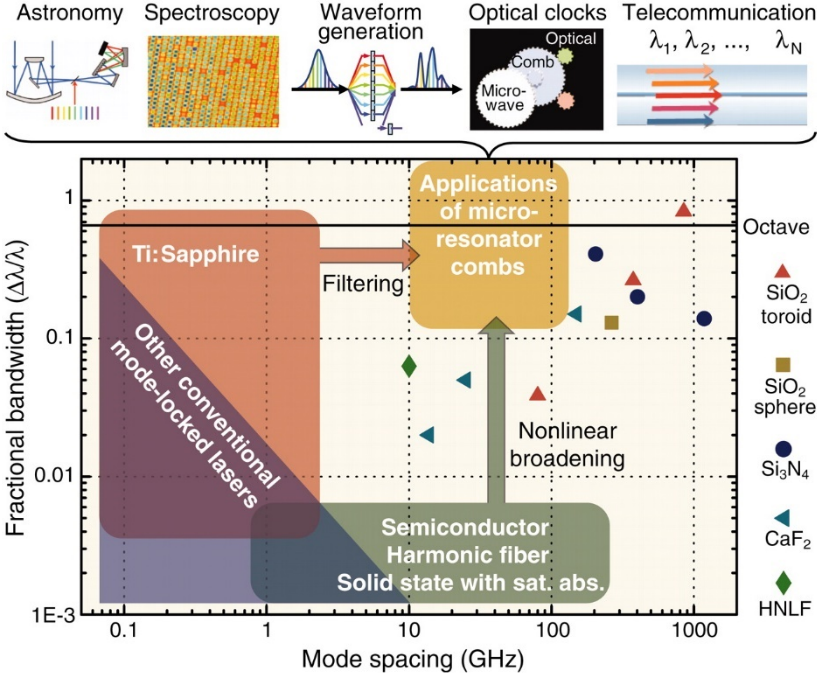
Large enhancements in the performance of the nanophotonic devices are required to meet the requirements for next-generation optical interconnects

WDM Source: Optical Frequency Combs

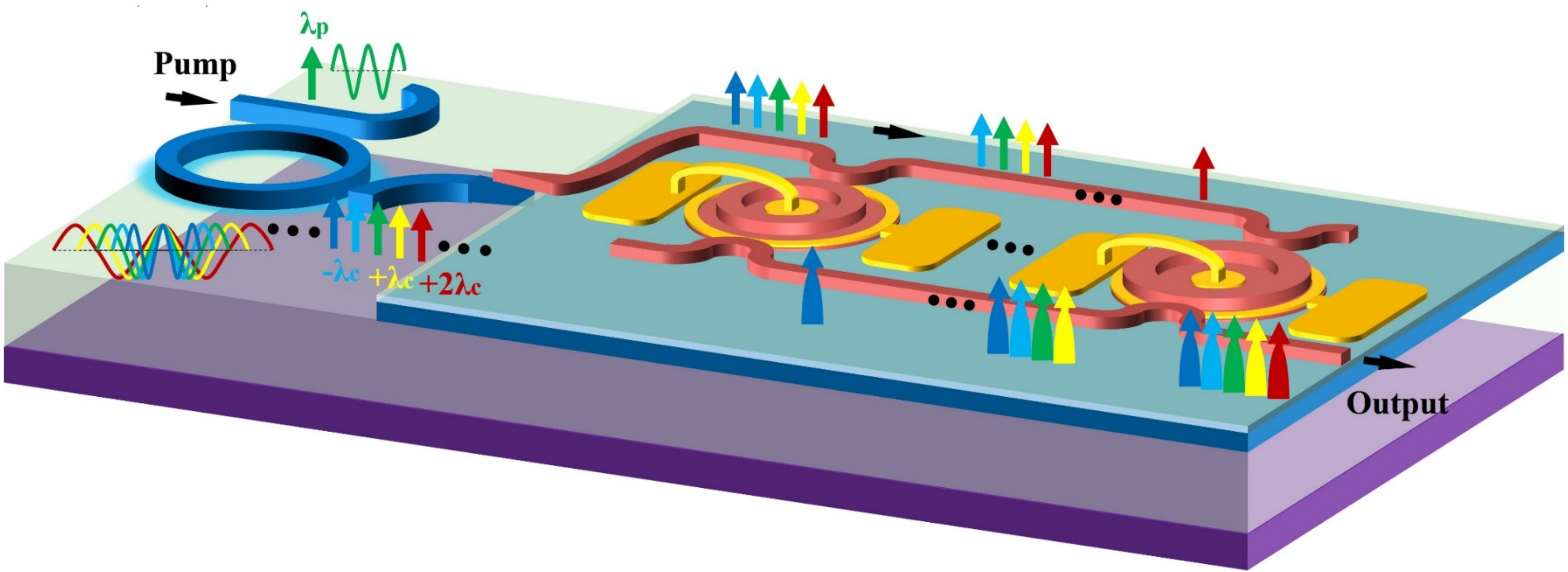


T. Kippenberg et al., "Microresonator-based optical frequency combs" , *Science* (2011)

- Ultrashort optical pulse train
- Four-wave mixing principle
- Advantages:
  - High degree of coherence
  - Uniform spacing between adjacent lines (defined by the free-spectral range of the resonator)
  - CMOS-compatible fabrication



Ultrafast Heterogeneously Integrated Optical Link



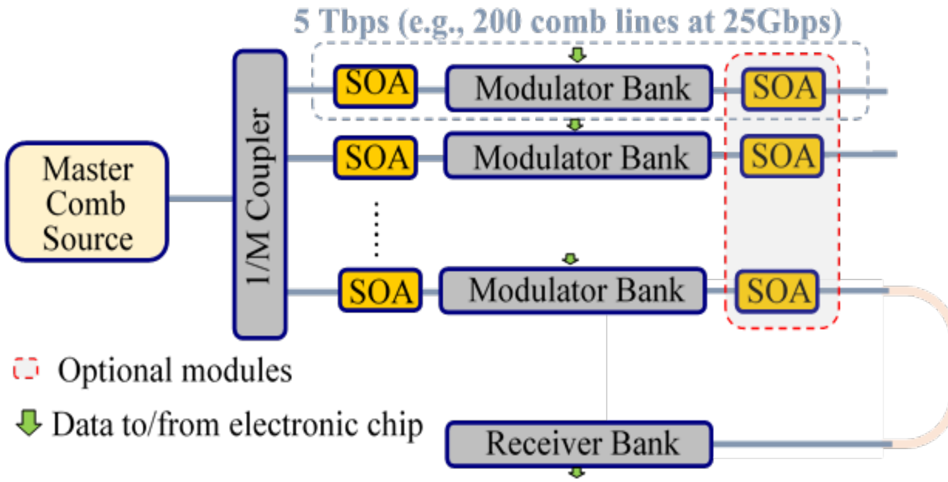
- Comb generation in SiN microresonator
- Adiabatic coupling into Si
- Microresonator add-drop filters simultaneously select and modulate each comb line
- The proposed modulating schemes can be employed for low-power/high-speed performance

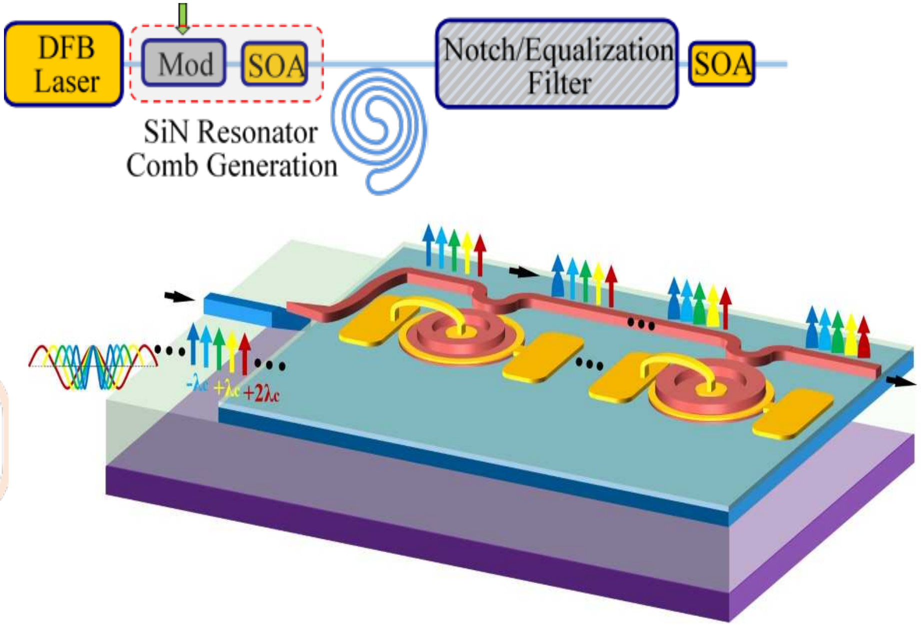
Broadband On-chip Optical Interconnect

On-chip optical interconnect: expected specifications	
Communication bandwidth	*5-10 Tbps / waveguide (80-160 DWDM channels)*
Optical bandwidth	*> 100 nm (O-band or C&L band)*
Latency	*1-10 ns*
Power Consumption	*<1 fJ/bit*
Size (Each modulator)	*< 50 µm^2*

Technical Approach

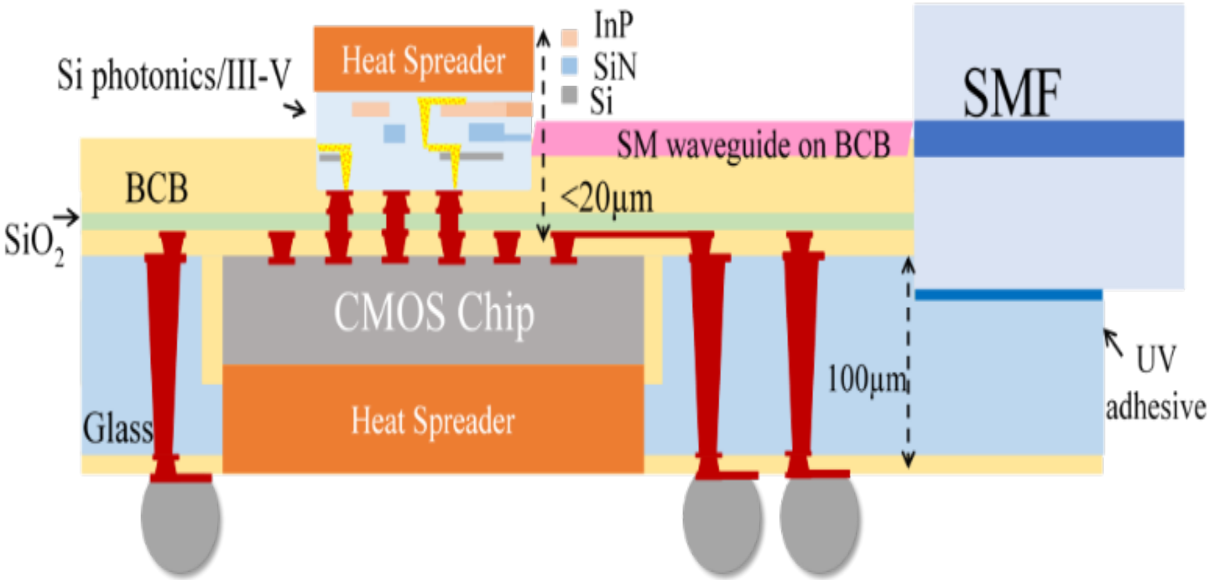
- Using an optical frequency comb source and filtering/modulating its individual tones using an array of Si mincroresonators
- Comb generation in SiN, modulation in Si, and lasing, SOA, and detection in III-V
- Operation wavelength: around 1300 (bandwidth: 40 nm); 100-200 comb lines with 25-50 Gbps modulators for a 5 Tbps modulated signal (or port)
- Future goals: 1) increasing the modulation efficiency/speed to achieve a 10 Tbps port; 2) use multi-ports for ultra-high data rates (e.g., ten 10 Tbps ports for 100 Tbps)





Technical Approach: Photonic-electronic System-on-Package for Ultra-high-speed and Low-power Interconnection

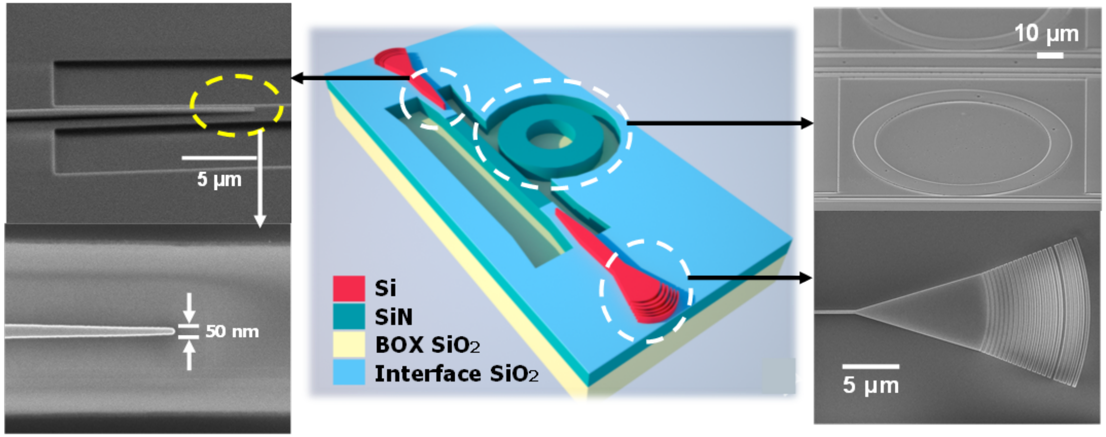
- Bonding III-V layer to the Si/SiN hybrid platform to form a complete photonic subsystem; tapered waveguide couplers for coupling light between different layers (including BCB glass)
- Integration with CMOS electronics using PRC's glass packaging technology
- Optical I/O through coupling glass waveguides to fibers



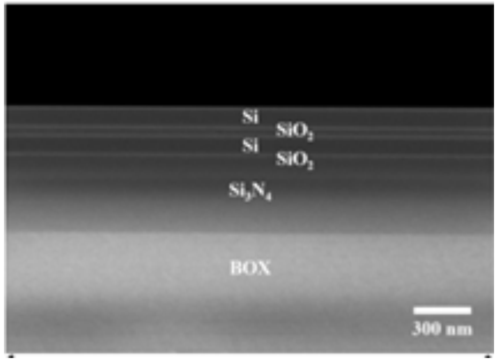
Builds on initial proposal submitted to Intel, Oct '19

Results & Key Accomplishments: Hybrid Platforms

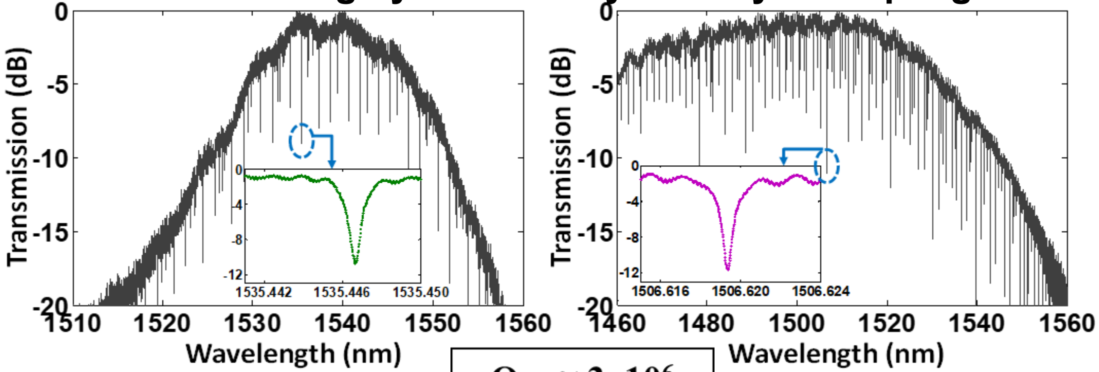
- Realization of several hybrid material platforms (e.g., double-layer Si, Si-on-SiN, SiC-on-SiN) with world-record performance
- Demonstration of several CMOS-compatible device architectures for ultra-fast low-power modulation, routing, and switching



Si-Si-SiN hybrid

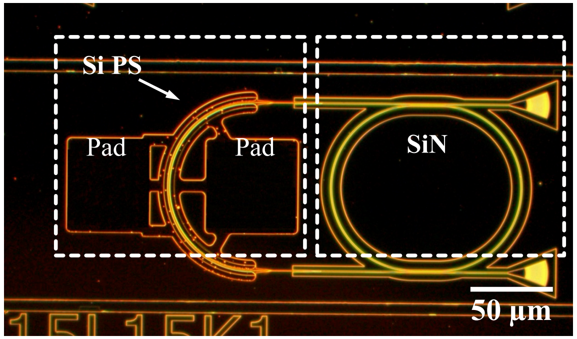


Highly efficient layer-to-layer coupling

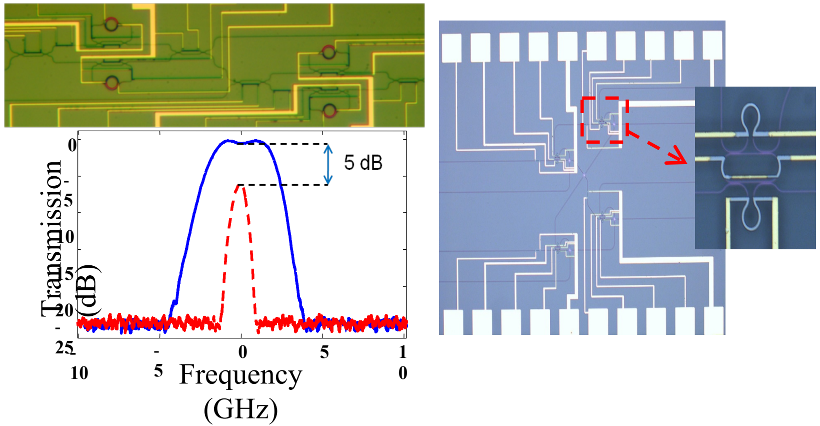


$Q_{int} \approx 3x10^6$

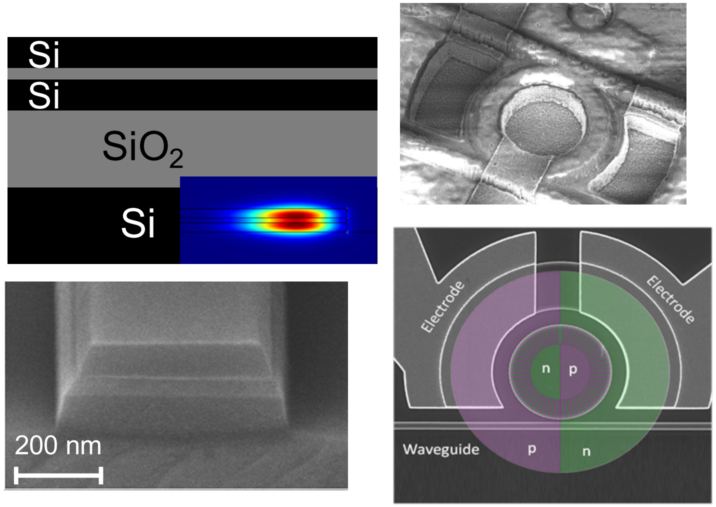
Coupling modulator



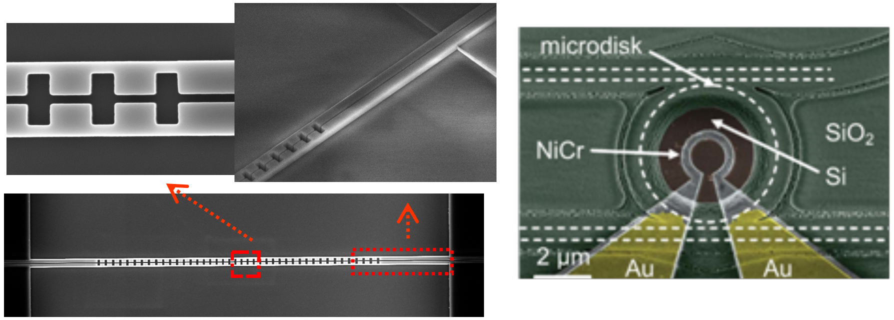
Results & Key Accomplishments: High-performance Devices



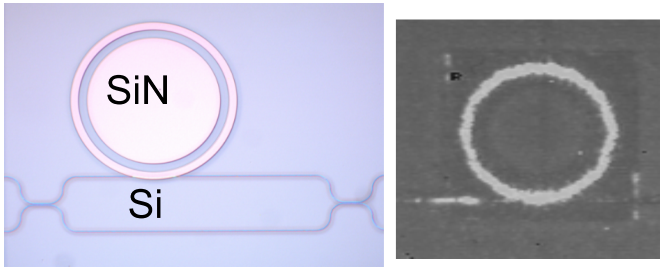
Reconfigurable photonic subsystems: High-order system for **reconfigurable filters** and **MIMO signal processing**



Fast modulator and switch devices based on depletion-mode PN junction and carrier accumulation in multi-layer silicon on isolator (SOI)devices



Low-power and wide-band tunable reconfigurable photonic devices based on **thermal and electro-static tuning**.



Hybrid Si/SiN material platform and devices: Enables low-loss and low-nonlinearity systems

Adibi's group has developed several high-performance material platform, device technology, and subsystems that can be used for millimeter-wave communication

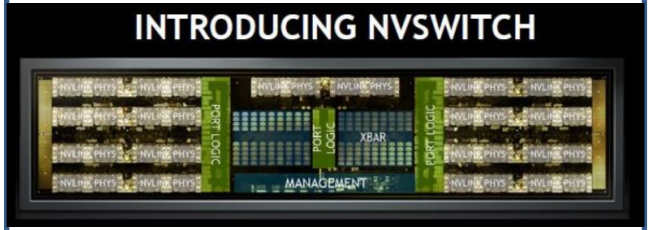
Comparison with the State-of-the-art : Photonic vs. Electronic Interconnects

Board-to-board

On-chip

Electronic

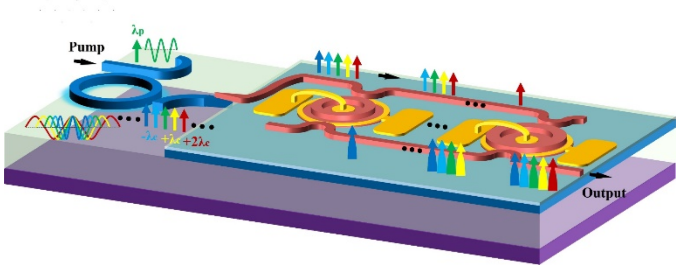
NVLink 2.0
8 Line @ 50 Gbps
2mm size port
200 Gbps/mm
2-8 pJ/bit
25-100 Gbps/mm/(pJ/bit)



2 PJ/bit @ 10 cm
50 Gbps/line
0.2 mm wire pitch
~500 Gbps/mm/(pJ/bit)

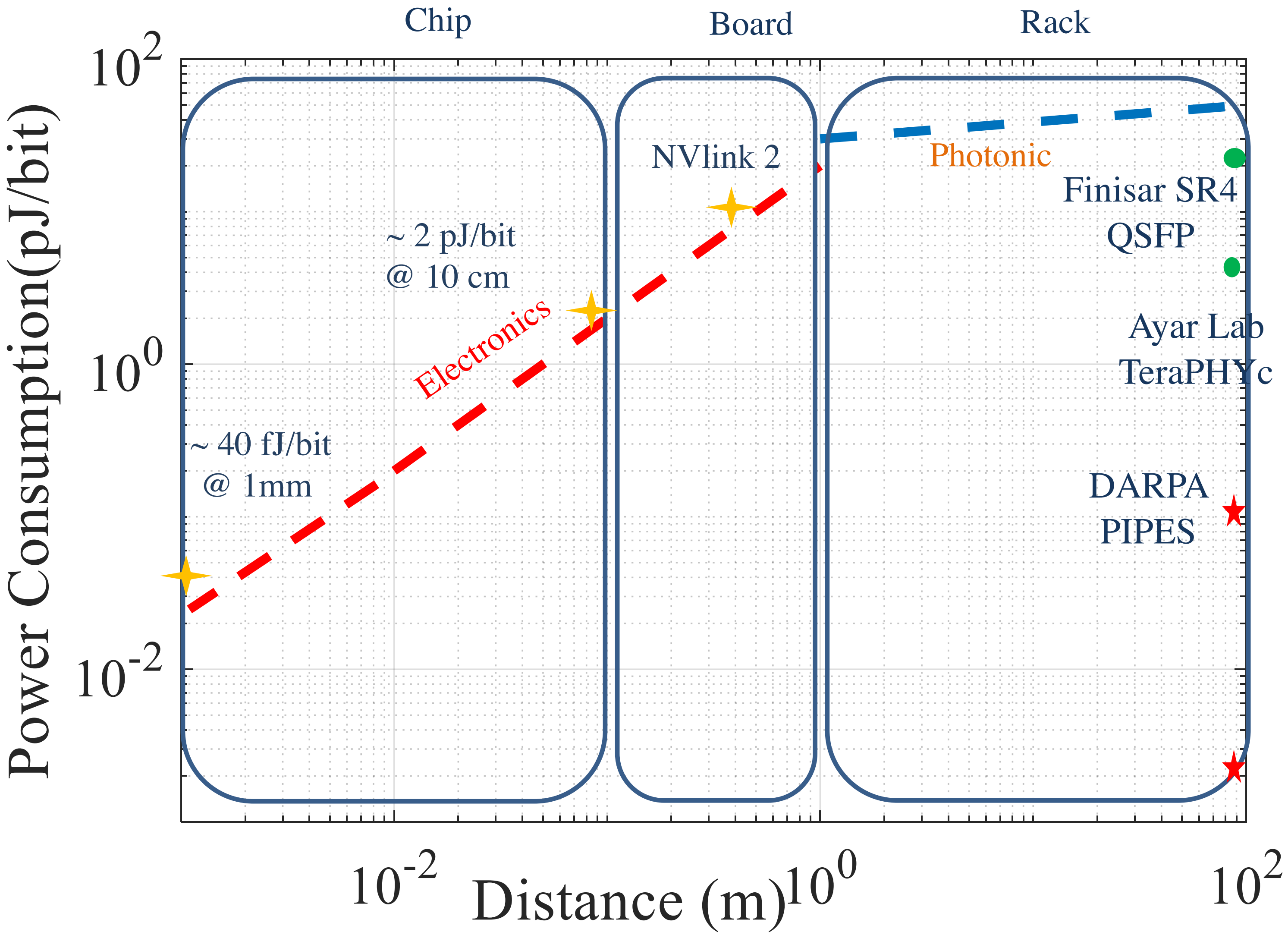
Photonic

DWDM
50 Gbps/Wavelength
50-100 fJ/bit
(Modulator share < 5fJ)
100 - 200 wavelengths (O-band)
250 μm fiber pitch
2×10^5-8×10^5 Gbps/mm/(pJ/bit)



0.1 PJ/bit @ 10 cm
50 Gbps/line
< 0.01 mm waveguide pitch
100 wavelengths/waveguide
~5×10^6 Gbps/mm/(pJ/bit)

Comparison with the State-of-the-art : Photonic vs. Electronic Interconnects



Summary

- ☐ We have demonstrated a variety of CMOS-compatible platforms with devices showing world-record performance.
- ☐ The key elements of this research, including high-speed modulators and WDM filters along with dispersion engineering form comb generation have been achieved.
- ☐ If funded:
  - Year 1 milestones include the demonstration of the comb signal in a hybrid SiN/Si platform, realization of the Si-based modulator/filter WDM network, and demonstration of the glass-based packaging technology for the proposed chips.
  - Year 2 milestones include integration of III-V lasers, optical comb generation, and Si-based WDM network along with the necessary packaging technology to form the first single-port multi-channel comb-based WDM transceiver.