Demonstration of a High-Inductance, High-Density, and Low DC Resistance Compact Embedded Toroidal Inductor for IVR

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2021 IEEE 71st Electronic Components and Technology Conference (ECTC) | 978-1-6654-4097-4/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECTC32696.2021.00209

***Abstract*—Next-generation high-performance computing (HPC) platform requires to run at higher speed with higher power consumption levels. Integrated voltage regulators (IVR) with a conversion ratio of 12 V to 1 V can help to reduce the power distribution network (PDN) impedance, increase the voltage conversion efficiency, and increase the regulation bandwidth. In this work, we present a new package embedded inductor array for multi-phase IVRs with a DC resistance as low as 22.8 mΩ. Inductors with three magnetic materials are demonstrated. With one material a small signal inductance as high as 475 nH is obtained, suitable for 12 V to 1 V conversion at 2 MHz. Another material gives an inductance of 192 nH suitable for 12 V to 1 V IVRs at 5 MHz. Each inductor occupies less than 6.25 mm^2 and are built with 400 μm thick metal polymer composite magnetic sheets. The metric effective AC resistance per unit inductance or R_{acx} is used to predict the inductor performance.**

I. Introduction

System on Chip (SoC) and processors (CPU) for high-performance computing (HPC) applications requires to run at very high-speed and high-power consumption levels. High bandwidth and high-performance power supplies are required; however, on-board or printed circuit board (PCB) power supplies cannot meet these tight requirements. Power supplies built in the same SoC package, called Integrated Voltage Regulators or IVRs, can reduce the power distribution network (PDN) impedance and increase the regulation bandwidth as they operate at several MHz. Figure 1 shows a package IVR with embedded inductors. Typical SoCs are powered with 1.7 V, but with power consumption rising over 100 W the input current starts to go over 65 A which becomes a problem. The trend for next-generation HPC platforms is to supply the SoC directly with 12 V or 48 V. At these input voltages, the IVR is restricted to work between 2 to 10 MHz.

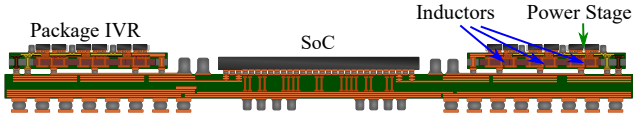

Figure 1: Package IVR with embedded inductors.

For high conversion ratio converters, the required inductance is over 400 nH at 2 MHz, which is reduced to around 100 nH at 10 MHz. At the same time, the DC resistance must be below 20 mΩ. Prior research has been focused on small inductors for low voltage conversion. Magnetic core thin-film inductors for high frequency tend to have a very low inductance of 20 nH or less [1]–[6] with DC resistances ranging from 20 mΩ to over 200 mΩ. Air core inductors [7] are only effective at a very high frequency over 100 MHz due to its low inductance of less than 10 nH. In [8], a solenoid embedded inductor is presented in a footprint larger than 7.25 mm^2 and inductance of 52 nH and DC resistance of 102 mΩ intended for 23 to 40 MHz IVRs. In [9], a PCB embedded toroid with a footprint of 110 mm^2 for 2 MHz Point-of-Load (PoL) converter is presented. It shows a small signal inductance of 925 nH, at 4 A its inductance decreases to 725 nH, and its DC resistance is 66 mΩ.

In this work, we have designed a new package embedded inductor targeted for high-conversion high-power integrated voltage regulators. It has a footprint of 6.25 mm^2, a DC resistance of 22.8 mΩ with a copper thickness of 28 μm, and small signal inductance as high as 475 nH. This work is structured as follow: section II describes the basic expressions used to determine the general inductor requirements, section III describes the new inductor structure, section IV describes the fabrication process and the fabrication results, and finally, section V shows the measurement results and presents the inductor's efficiency space where the inductor requirements become specific for each magnetic material.

II. Inductor Requirements

In [10], the metric R_{acx} or Effective AC Resistance per Unit Inductance was introduced as a metric of the inductor performance and is given by (1), where D is the converter duty cycle, f_s is the switching frequency, and R_{AC} and L are the inductor's inductance and resistance spectra.

$$R_{acx}(D, f_s) = \frac{2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} \frac{R_{AC}(nf_s)}{L(f_s)} \quad (1)$$

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The R_{acx} factor is related to the inductor power loss P_L according to (2).

$$P_L = P_{L,DC} + P_{L,AC} = I_L^2 R_{DC} + \Delta i_L^2 L(f_s) R_{acx}(D, f_s) \quad (2)$$

where R_{DC} is the inductor's DC resistance, I_L is the inductor's DC current, and Δi_L is the inductor's current ripple amplitude. The current ripple Δi_L and duty cycle are given by (3) and (4), respectively. The duty cycle expression assumes a two-phase series capacitor buck converter topology as shown in [11].

$$\Delta i_L = \frac{V}{2L}(1-D)T_s \quad (3)$$

$$D = \frac{2V + I\left(R_L + R_{LS}\right)}{V_g - I\left(R_{HS} + R_{fly} + \frac{R_{LS}}{2}\right)} \cdot \frac{1}{\eta_e} \quad (4)$$

where R_L is the inductor power-related equivalent resistance, R_{HS} and R_{LS} are the on-resistance of the high-side and low-side MOSFETs of the buck converter, R_{fly} is the flying capacitor ESR, and η_e is the MOSFET's efficiency (not considering the output capacitance, gate charge, and reverse recovery losses).

For a required inductor efficiency η_L, output voltage V, and load current I_M, it can be shown that for maximum efficiency at I_M the inductor DC losses are equal to its AC losses. This allows to solve for the optimal inductor parameters R_{DC}, L, and R_{acx} given by (5) and (6) given a target inductor efficiency, where $P_L = I_M V(1/\eta_L - 1)$.

$$R_{DC} = \frac{P_L}{2}\frac{1}{I_M^2}\,[\Omega] \quad (5)$$

$$\frac{\widetilde{R}_{acx}}{L} = \frac{P_L}{2}\frac{4f_s^2}{V^2(1-D)^2} = M(D, f_s)\left[\frac{\Omega}{\mathrm{H}^2}\right] \quad (6)$$

Here $\widetilde{R}_{acx}$ is the maximum value that the fabricated inductor can have, so that $R_{acx} < \widetilde{R}_{acx}$, where R_{acx} is the measured value. When the measured R_{acx} is larger, the inductance needs to be increased to reduce the current ripple and therefore, the losses.

Considering the next parameters: maximum inductor DC current of 2.5 A, current at peak efficiency of $I_M = 1.875$ A, output voltage of 1 V, inductor efficiency $\eta_L > 95\%$, and conversion ratio of 12 V to 1 V using a two-phase series capacitor buck converter [11] using GaN MOSFETs (which including the MOSFET losses gives a duty cycle around $D = 0.1834$), we obtain a maximum power loss of $P_L = 99$ mW, a DC resistance $R_{DC} < 14$ mΩ, and the relation of $\widetilde{R}_{acx}$ and L shown in Figure 2.

From Figure 2 we can extract the required inductor parameters, to obtain a current ripple $\Delta i_L = 0.5$ A, which are summarized in Table I. If the values of R_{acx} obtained with the fabricated inductors are higher than those in Table I or if the DC resistance is higher than 14 mΩ, then the inductance should increase as much as required to decrease the current ripple to keep the power loss, given by (2), below the maximum for the target inductor efficiency.

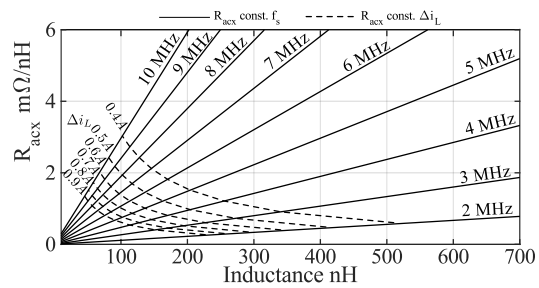

Figure 2: Required R_{acx} to inductance L ratio for 12V to 1V conversion, duty cycle of $D = 0.1834$, and $\eta_L = 0.95$.

V_{in}	D	f_s MHz	L nH	$\widetilde{R}_{acx}$ mΩ/nH
12	0.1834	2.0	408	0.485
12	0.1834	5.0	163	1.211
12	0.1834	10.0	81	2.423

Table I: Inductor requirements with $\Delta i_L = 0.5$ A and , $R_{DC} = 14$ mΩ.

III. Inductor Model

In [10] a new inductor structure was presented, which is also shown in Figure 3(a). This inductor when fabricated with a magnetic core substrate of thickness of 400 μm, and relative permeability of $\mu' = 180$, can only achieve a maximum small signal inductance of 190 nH. In this work we present an optimized inductor that doubles the small signal inductance density with only a small increment of the DC resistance, and it uses the same fabrication process shown in [10]. Inductors fabricated in the previous work and this work are shown in Figure 3. The inductor of

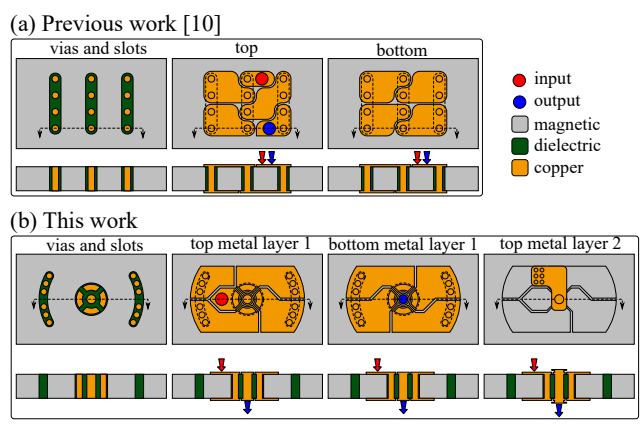

Figure 3: Inductors of previous work [10] and this work.

this work has 3 main changes with respect to the previous inductor: (i) the central vias are re-arranged to reduce the magnetic path length to increase the inductance, (ii) use of additional vias on the sides and non-cylindrical vias in the center to reduce the DC resistance, and (iii) an additional return via in the center. The inductor in Figure 3(a) has both ports (input and output) on the same side. However, for a package IVR as shown in Figure 1 there must be a connection to the SoC package using through vias. The

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return via in this inductor can serve a dual purpose of increasing inductance and connecting the input and output ports on different planes.

In addition, in this inductor structure all the magnetic field is confined inside the inductor structure no matter how large the magnetic sheet substrate is. Figure 4 shows an array of 16 inductors arranged in a 4×4 matrix in a square of length of 1 cm.

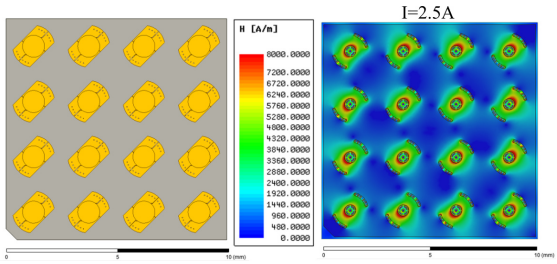

Figure 4: Inductor array with zero coupling between adjacent inductors.

IV. Fabrication Process

The array of 16 inductors shown in Figure 4 was fabricated with three different magnetic materials with thickness of 400 μm. Two inductor arrays with material HPE1, one with HPE2, and one with RM4A were fabricated at the same time by embedding a square of 1 cm width for each material in a 60×60 mm FR4 substrate. The small signal permeability spectra of the three materials are shown in Figure 5.

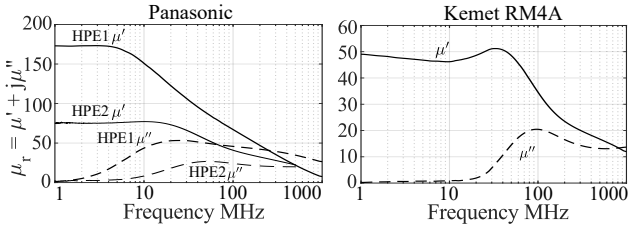

Figure 5: Small signal permeability spectra.

A modified process based on [10] was used to fabricate the inductors on thicker high permeability magnetic substrate. The materials HPE1, HPE2 (courtesy Panasonic) and RM4A (Commercially available KEMET sheet) had comparable coefficient of thermal expansion (CTE) to FR4 board and they were cut and embedded in 400 μm thick FR4 substrate as shown in Figure 6(a), by vacuum laminating a 5 μm thick ABF^{TM} dielectric material on both top and bottom. In this way the fabrication of various materials was carried out at the same time with no change in process conditions since all materials are now in the same substrate. However, the drilling parameters (power, speed, repetitions, etc.) need to be adjusted accordingly for each material. Then as shown in Figure 6(b), the first metal layer is fabricated following the process shown in [10]. Finally, Figure 6(c) shows a second metal layer fabricated to expose the connection in a Ball Grid Array (BGA) pattern.

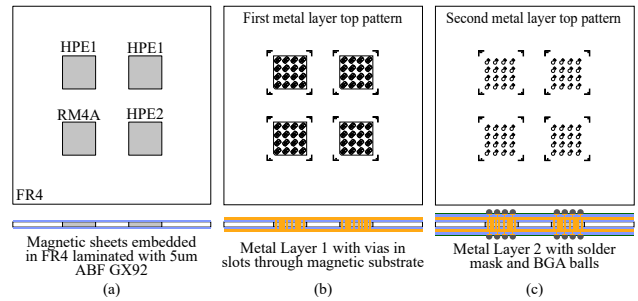

Figure 6: Overall fabrication steps. (a) three different materials embedded in 6×6 cm FR4 substrate, (b) metal layer 1 process as describe in [10], (c) second metal layer.

To drill slots in the 400 μm thick magnetic sheet, an IR femto-second laser was used. Figure 7 shows the result of trying to drilling through this thickness from one side only. To reduce the tapering, a two-sided (top and bottom)

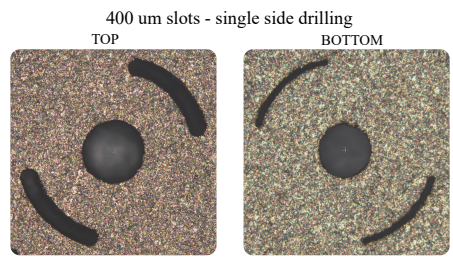

Figure 7: Result of single-side drilling in 400 μm thick magnetic sheet.

drilling was employed. In addition, the drilling process on each side was divided in to three steps, as shown Figure 8. First an *opening* operation with lower power is used to define the feature shape and size, followed by a *drilling* process with higher power but smaller feature size to not affect its dimension, finally, a *de-tapering* process is performed were only the borders are ablated. Then, the three steps are repeated on the other side of the sample.

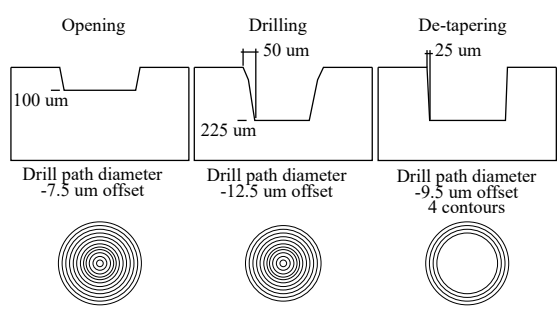

Figure 8: Three step drilling process to obtain accurate dimensions.

This double-side three-step drilling process produces well defined slots as shown in Figure 9(a). The slots were then vacuum laminated with 30 μm thick ABF^{TM} dielectric sheet on both top and bottom under pressure. The dielectric sheet

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was heated to its viscoelastic temperature to ensure filling the slots with no voids. After the sample was cured, another 15 μm of the dielectric sheet was vacuum laminated on either side to planarize the surface and the sample was cured again. Vias were drilled in the slots also using the two-sided process. A thin seed layer of copper was deposited using an electroless copper plating bath as shown in 9(b).

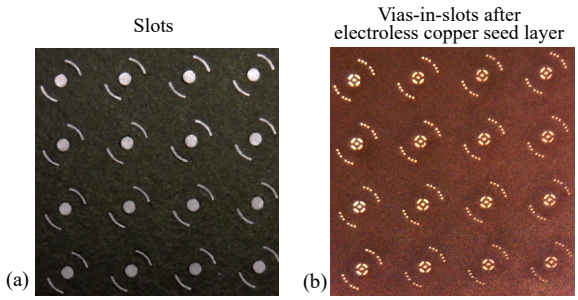

Figure 9: Results of slots, via drilling, and electroless copper seed layer deposition.

The samples were then annealed at 180 °C for 30 minutes in Nitrogen environment. After annealing, a 50 μm thick negative photoresist was laminated on each side of the sample and a positive photomask was used. A contact ultraviolet lithography system was used to transfer the mask features onto the sample. After the sample was developed, it was subjected to O_2 plasma etch to remove any photoresist debris. After the sample was dipped in 5% concentration H_2SO_4 (to improve wettability for electroplated copper and remove any oxide that might have formed), it was electroplated in a copper bath. The sample was again annealed at 180 °C for 30 mins in nitrogen environment to remove any residual stresses in the electroplated copper. A 2-step process was used to strip the photoresist. An amine-based stripper (to remove fine line features) is used followed by a hydroxide stripper to completely remove the photoresist.

Figure 10 shows the fabrication results for the first and second metal layer of a single array, the entire sample with the four materials and the solder mask, and the cross-section of the central vias. A copper thickness of 28 μm has been platted to obtain a low DC resistance of 22.8 mΩ. The inductor bounding box has a size of 1.9×1.1 mm, and and the thickness of the fabricated inductor with the first metal layer is 600 μm. Each inductor is spaced 2.5 mm from each other.

Using Ansys Maxwell to simulate the DC resistance with a copper thickness of 28 μm, we have to set the copper conductivity to 4.2 S/m (resistivity of 2.35 Ωm) to obtain the measured DC resistance. This conductivity is consistent with electroplated copper resistivity experiments as shown in [12]. With a copper thickness of 50 μm the DC resistance would be reduced to 15.7 mΩ.

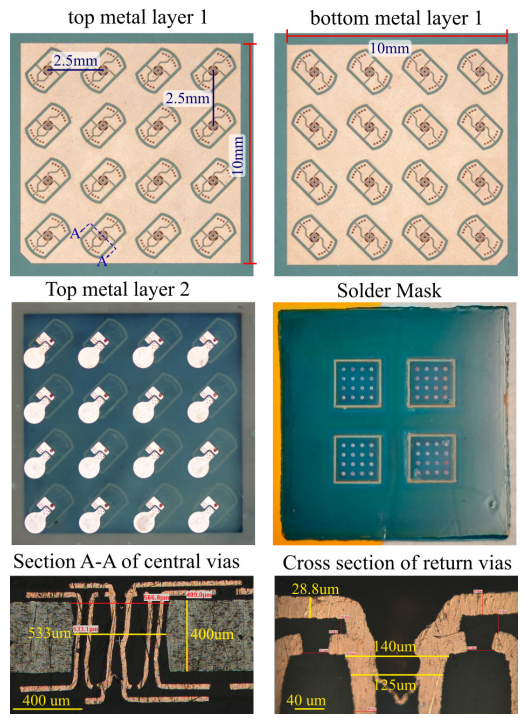

Figure 10: Fabrication results.

V. Measurements

The small signal inductance and resistance were measured from 1 MHz to 20 MHz with an open source low frequency VNA, and from 21 MHz to 1 GHz using a VNA from Agilent Technologies™ model E8363B. The DC resistance was measured with a 4-wire method using a multimeter from Hewlett Packard model 34401A.

Since at 1 MHz an inductor with 100 nH has an impedance of just 0.6283 Ω, which is much less than $Z_0 = 50\Omega$, a shunt measurement method from 1 MHz to 20 MHz was used. From 21 MHz to 1 GHz a series measurement method was used. Figure 11 shows the inductance and resistance equation extracted from S-parameter measurement.

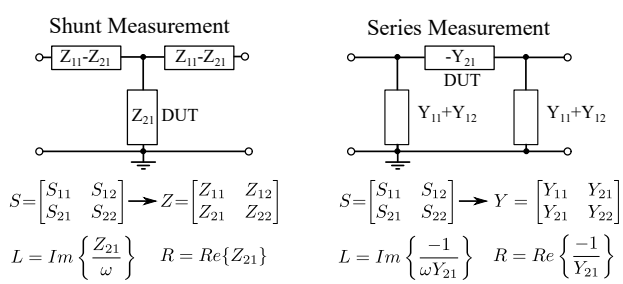

Figure 11: Shunt and series measurement models.

The measured small signal inductance is shown in Figure 12 where 10 inductors with HPE1, 6 with HPE2, and 4 with

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RM4A were measured. There is a good correlation between

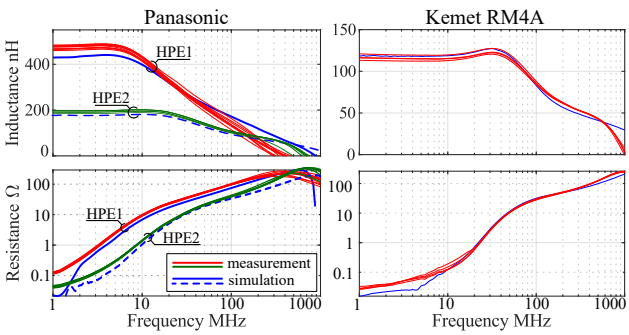

Figure 12: Measurement results. Several inductors were sampled.

the simulations and measurements. The discrepancies in the resistance near 1 MHz are due to low measurement accuracy of the permeability.

Table II shows the summary of properties for HPE1 material. We observed that the losses have a constant offset by a factor of 1.29 which means the imaginary part of the HPE1 permeability used in simulation is 23% lower. Similarly, the real part of the permeability used in simulation is on average 6% lower below 10 MHz.

f_s [MHz]	L_{sim} [nH]	L_{meas} [nH]	$\frac{L_{\text{meas}}}{L_{\text{sim}}}$	R_{sim} [Ω]	R_{meas} [Ω]	$\frac{R_{\text{meas}}}{R_{\text{sim}}}$
2	442	475	1.074	0.138	0.344	2.49
5	447	474	1.061	1.713	2.518	1.47
10	406	423	1.042	6.973	9.468	1.36
25	299	301	1.003	22.05	28.52	1.29
50	231	213	0.924	41.24	53.42	1.29
75	198	169	0.854	58.89	76.41	1.29
100	175	138	0.786	76.22	98.47	1.29

Table II: Inductor properties with HPE1 material

Table III shows the summary of properties for HPE2 material. At low frequencies the simulation is over-optimistic, whereas at high frequencies the measured losses seem to be related to a higher permeability, where the actual permeability is on average 7% higher.

f_s [MHz]	L_{sim} [nH]	L_{meas} [nH]	$\frac{L_{\text{meas}}}{L_{\text{sim}}}$	R_{sim} [Ω]	R_{meas} [Ω]	$\frac{R_{\text{meas}}}{R_{\text{sim}}}$
2	179	193	1.08	0.037	0.074	2.01
5	181	195	1.07	0.186	0.295	1.58
10	184	197	1.07	1.071	1.390	1.29
25	166	177	1.07	7.693	8.201	1.07
50	129	140	1.08	19.21	20.94	1.09
75	108	118	1.09	27.58	31.07	1.13
100	96	105	1.10	34.303	39.96	1.17

Table III: Inductor properties with HPE2 material

To show how the R_{acx} parameter looks like, using the average of the measurements for HPE1 and HPE2 and the expression in (1) we can obtain the R_{acx} curves for different frequencies and duty cycles. Figure 13 shows the R_{acx} values for HPE1 material, and Figure 14 shows the R_{acx} for HPE2 material.

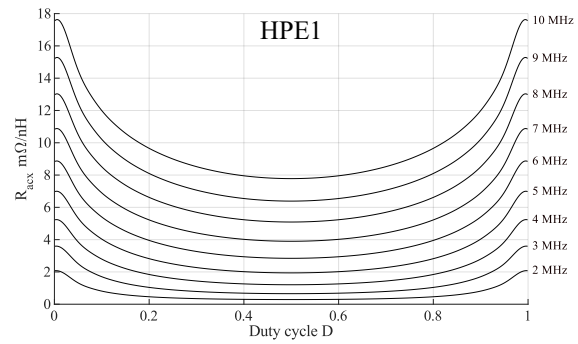

Figure 13: R_{acx} curves for material HPE1.

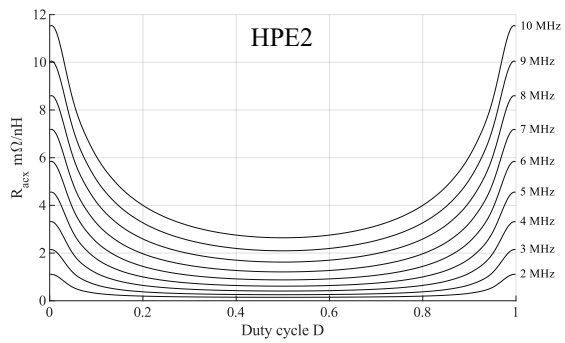

Figure 14: R_{acx} curves for material HPE2.

We observe that for duty cycles less than 20% the inductor losses increase drastically exposing the challenge of high conversion ratio IVRs. Comparing the curves on Figures 13 and 14 to the values on Table I we see that HPE1 can only match the required R_{acx} up to 2 MHz, and HPE2 up to 5 MHz.

We can calculate the required inductance for a material to achieve a target inductor efficiency using the material's R_{acx}. With the same IVR conditions as given in Section II we can compute the ratio M given by (6), then for the specific switching frequency f_s and duty cycle D we can extract the material R_{acx} from the curves shown in Figures 13 and 14 to finally compute the inductance as $L = R_{acx}/M$. Figures 15 and 16 shows the inductor space efficiency for material HPE1 and HPE2 where the inductance L, current ripple Δi_L, duty cycle D, and R_{acx} are plotted with respect to frequency, and different curves are plotted for inductor efficiencies from 92% to 96%. It must be noted that at each target efficiency a different maximum DC resistance is required. The efficiency space is a design aid that gives the requirements for a particular material.

When the copper thickness is increased to 50 μm the DC resistance is reduced to 15 mΩ, and the inductor with

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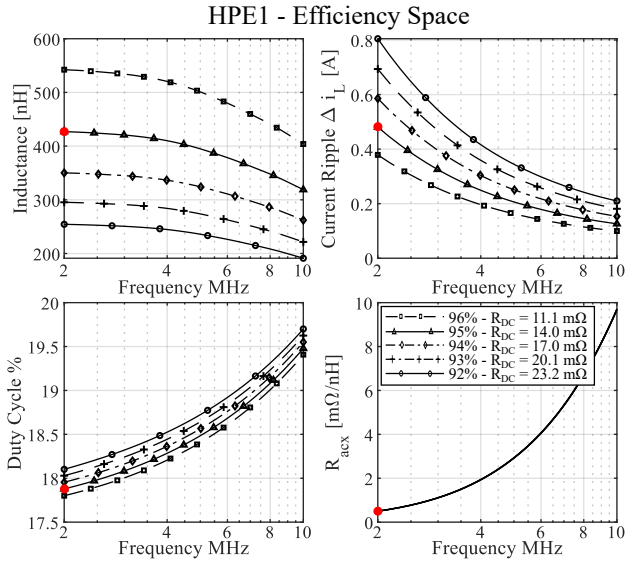

Figure 15: R_{acx} curves for material HPE1.

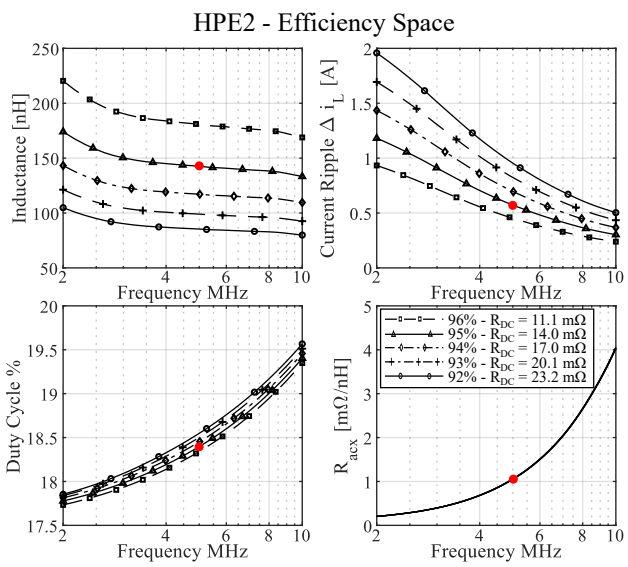

Figure 16: R_{acx} curves for material HPE2.

material HPE1 can work for 12 V to 1 V at 2 MHz, and material HPE2 can work for 12 V to 1 V at 5 MHz.

VI. Future Work

So far, the R_{acx} metric only considers the small signal inductance and resistance. However, it is required to consider the large signal and saturation current effects. Future work includes the large signal and saturation current measurements and include them in this design framework.

VII. Conclusions

A new inductor structure was presented that can achieve an inductance of 475 nH with HPE1 and 195 nH with HPE2 with a DC resistance of 22.8 mΩ. The implemented inductance density with HPE1 is 76 nH/mm^2 and 127 nH/mm^3, and with HPE2 it is 31.2 nH/mm^2 and 52 nH/mm^3. The measured inductance and resistance indicate that HPE2 can be used for 12 V to 1 V IVR at 5 MHz and HPE1 for 12 V to 1 V at 2 MHz.

Acknowledgment

This work was supported in part by ASCENT, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA and the 3D Systems Packaging Research Center (PRC).

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