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Multiphysics Challenges and Opportunities for Integrated Voltage Regulators in Power Delivery Architectures

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***Abstract*—Integrated voltage regulator (IVR) based power delivery architectures have become a growing trend in high performance computing systems. Integrated power delivery architectures typically feature high-frequency switching devices and embedded passive components, which can be integrated either inside the die or in the package. However, dense functional integration in such architectures though necessary brings a new set of challenges to system designers. In this paper, we study the impact of heterogeneous integration on the design of power delivery architectures that addresses issues related to electrical, thermal, and electromagnetic domains through test cases. The key design problems arising out of heterogeneous integration and the solutions for each of the domains are identified. Although the electrical impedance profile seen by the load becomes flatter in the frequency domain with fewer resonances, noise coupling at the load increases due to the close proximity of noise sources. The electromagnetic interference (EMI) levels are higher and therefore more EMI and noise mitigating filters are needed for judicious placement at the package and die-level. High thermal resistance associated with embedded passives results in a threshold for power losses in embedded inductors beyond which the conventional top-level cooling is insufficient and a local cooling solution is needed.**

***Index Terms*—DC-DC converters, heterogeneous integration, power delivery, thermal management, electromagnetic compatibility, conducted EMI.**

I. Introduction

WITH Moore's law for transistor-scaling slowing down, the semiconductor industry is looking at other avenues for performance scaling of electronic systems. Heterogeneous integration provides such an avenue for system and performance scaling. Heterogeneous integration aims to bring miscellaneous components fabricated at different technology nodes onto the same packaging platform. Heterogeneous integration of step-down switching voltage regulators (VR) [1], for example, has become a recent trend for high-performance computing (HPC) applications. The switching-type regulators feed periodically switching drive signals into the power FET devices to reduce the high input voltage along with a passive LC output filter to smooth the output to obtain a lower voltage DC source, as shown in Fig. 1. Traditionally, discrete power delivery architectures are employed. For the discrete case, voltage regulator power delivery circuit components are oftentimes bulky and placed on the printed circuit board, as shown in Fig. 2. To improve the spatial efficiency and/or power density, power delivery architectures [2] need to move and integrate the voltage regulator power delivery circuits closer to the chip and reduce the distance between the power source and load, as illustrated in Figs. 1 and 2. The shorter distance (shown as distance l in Fig. 1) results in a shorter interconnect with lower parasitics, which can have multiple performance benefits [3] [4] at the system level, including lower power losses in the interconnect and a faster transient response.

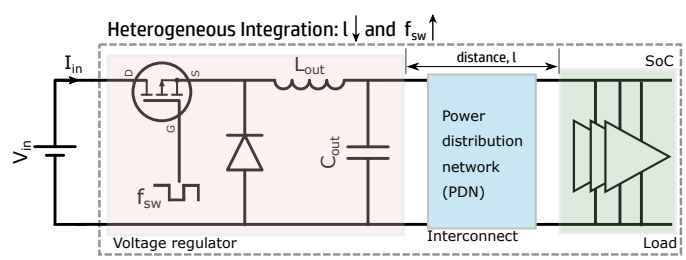

Fig. 1. Typical switching voltage regulator based power delivery architecture and the impact of heterogeneous integration.

Power delivery is fundamentally a multiphysics design problem. Delivering power involves the interplay between electrical, electromagnetic, and thermal domains, which is shown in Table I. Integrated power delivery architectures can pose significant challenges to the system designer. For the integration to be feasible, the components of the voltage regulator have to be made compact and placed in close proximity to the system-on-chip (SoC). To make the LC filter components compact, the switching frequency has to be increased to reduce the voltage and current ripple [5] of the voltage regulator. This trend of increasing switching frequency with integration is shown in Fig. 2 and allows for reduction in the size of the inductor and capacitor components used. The compactness and proximity of the passive components to the SoC, however, exacerbate thermal management problems. If the inductors are embedded in the package, they need a magnetic core to reduce

This work was supported in part by ASCENT, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

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size and increase inductance density, where Joule heating and temperature dependence of the magnetic material can reduce IVR efficiency. The increased conductor resistance of the embedded inductors increases their self-heating effect. Due to large signals involved in voltage regulators, the hysteresis loss of the magnetic core increases, thereby limiting the saturation current, which can represent a major problem. Also, the embedded inductors can suffer from thermal coupling from other high heat generating sources such as the high-power silicon devices residing above it. The combination of self-heating and thermal coupling of the inductors adversely impacts their AC and DC electrical resistances, conduction loss, and hence, the overall power efficiency of the voltage regulator. To avoid overheating, designers often implement a thermal gate [6] in the architecture, which senses overheating and turns off the hot phases for cooling. However, such thermal gating results in system performance throttling and impacts how long the system can sustain its peak performance. From the noise perspective, the high switching frequency results in higher levels of EMI and switching noise, requiring more filtering capacitors [7] at the input stage. Heterogeneous integration, therefore, accentuates the multi-physics design challenges [8] that generally arise in a power delivery architecture. The thermal, electrical, and EMI related issues are coupled together whereby the geometrically compact power delivery solution does not help in either the EMI or thermal solutions. This strong coupling between the domains makes heterogeneous integration for power delivery a challenging multiphysics problem.

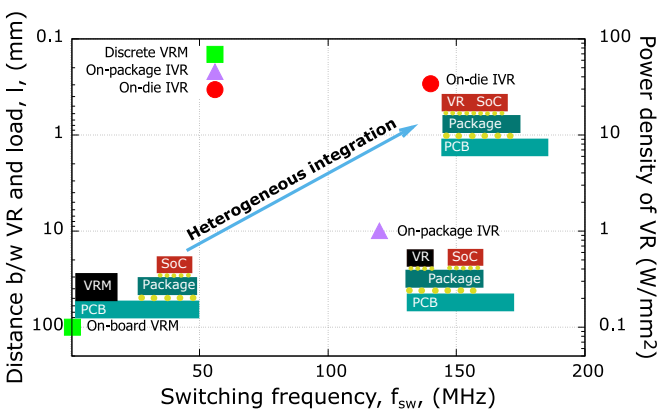

Fig. 2. Heterogeneous integration of power delivery architectures, showing the progression from discrete on-board to integrated voltage regulators on-package and on-die.

In this paper, the impact on the solution space for heterogeneous integrated power delivery architectures is presented. In the past, analysis and design space exploration have been conducted mostly in individual domains. For the thermal domain, higher SoC temperatures [9] [10] and inductor temperatures [11] have been observed for higher level integration. The impact of placement of embedded inductors on thermal performance has been studied [12]. For power delivery solution, design exploration of voltage regulator placement has been done for various power delivery architectures [13] and compared for their voltage droop performances. In the electromagnetic domain, higher EMI levels [14] have been observed for fast-switching Gallium Nitride (GaN) FET-based DC-DC converters. Also, the impact of the placement of voltage regulators [15] on radiated EMI level has been studied. This paper, on the other hand, provides a comprehensive coverage of system design in the multiphysics domains of thermal, power, and EMI along with their interactions. It expands our earlier work [10], which highlighted the benefits and challenges associated with integration of voltage regulators, and explores the solutions required. In each of the domains, the fundamental trends and limits of the solutions resulting from integration of voltage regulators are analyzed. For EMI, the impact of integration on conducted noise and EMI filter design are covered. For thermal, the need for a local cooling solution is analyzed. For power, the effect of integration on the size and shape of the resonances, and thereby the time and frequency domain responses of the PDN are analyzed.

TABLE I
MULTIPHYSICS PARAMETERS FOR THE DESIGN OF POWER DELIVERY NETWORK [a]

Domain	Figure of merit	Design goal
Thermal	Temperatures of SoC, VR, and inductors	$110°C$, $100°C$, and $85°C$
Electrical (frequency)	Impedance seen, Z_{in}	below the target impedance [16]
Electrical (time)	Voltage droop [17]	single and low droop
Electromagnetics	EMI levels	CISPR 11/22/25 compliance

[a] not specific to a particular system or materials or components.

The rest of this paper is organized as follows. In Section II, the impact of heterogeneous integration on design complexity and solution space in the multiphysics domains are analyzed. Section III verifies the analysis using examples of regulators with and without integration in each of the respective domains. Section IV discusses the results in terms of the observed trends and limits for the solutions, followed by conclusions in Section V.

II. MULTIPHYSICS DESIGN FOR INTEGRATED POWER DELIVERY ARCHITECTURES

The heterogeneous integration of power delivery architectures fundamentally reduces the distance, l, between the power source and load, as shown in Fig. 2. At the same time, the switching frequency, f_{sw}, is increased to lower the LC output filter requirements for the IVR design and hence their respective component sizes. With compact passive components and close proximity between components, the foot print area of the regulator is reduced, thereby increasing the power density or power delivered per unit area of the regulator. The length of interconnect, switching frequency, and power density have direct impact on the electrical, EMI, and thermal domains respectively. Their impact on the performance and the corresponding solutions space in these areas are covered in this section.

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A. Electrical power delivery

For power delivery, the impedance seen by the load die in the frequency domain, or equivalently the voltage droop caused by a current surge by the device in time-domain, are critical design parameters for achieving silicon performance. This impedance or voltage droop represents an important design metric. The power distribution network (PDN) generally has various components such as power planes in the package with connectivity to the printed circuit board (PCB). The other components are vias, solder bumps, and a power grid in the silicon device. If the VR is incorporated on the PCB, the PDN will have various other components as well, such as sockets, capacitors, etc. The wide variety of components and the available design choices make the performance of a PDN design specific. Therefore, to obtain general trends with respect to integration, this section relies on the fundamental concepts of transmission line theory and standing wave resonance modes.

TABLE II
POWER DELIVERY COMPARISON OF DISCRETE AND INTEGRATED POWER DELIVERY ARCHITECTURES [a]

Parameter	On-board VRM [18]	On-package IVR [19]	On-die IVR [1]
Switching frequency, f_{sw}	$300KHz$	$120MHz$	$140MHz$
Number of phases, N	4	8	16
Closed-loop bandwidth, f_c	$40KHz$	$10MHz$	$80MHz$
Sense point location	Socket	Package	On-die

[a] values specific to the architectures considered.

1) Impact of integration on interconnect performance: The impedance profile, Z_{in}, seen by the SoC while looking towards the voltage regulator determines the voltage droops due to sudden changes in the current inside the die. The typical PDN has multiple resonance peaks coming from various locations of the network, particularly for on-board VRM designs. The impact of integration on the magnitude and locations of the resonance peaks in the impedance response is discussed in this section.

To understand the impact on the scale or magnitude of impedance, let us consider the PDN as a power transmission line (PTL) [20], shorted at the source side where the voltage regulator resides, as shown in Fig. 3. This one-dimensional representation of PDN, although an approximation, provides an easier understanding of the power delivery network that may include complex geometries for power and ground planes. The impedance seen by the load depends on the length of the transmission line. For an electrically short transmission line, $\gamma l << 1$, the impedance seen by the load can be approximated, as:

$$Z_{in,OL} = Z_0 tanh\left(\gamma l\right) \approx Z_0 \gamma l \tag{1}$$

where $Z_{in,OL}$ is the open-loop input impedance seen by the die, γ is the propagation constant of the PTL, l is the length of the PTL, and Z_0 is the characteristic impedance of the PTL.

Eq. 1 above shows that Z_{in} is proportional to the length of PTL or the distance between source and load, l. Due to integration, the impedance Z_{in} becomes smaller [1] in general

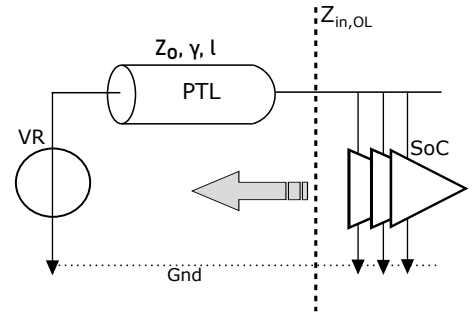

Fig. 3. Representation of PDN as a power transmission line and the impedance seen by the SoC, Z_{in}.

with this reduced length scale between the SoC and voltage regulator. Z_{in} can be reduced further through any built-in Metal Insulator Metal (MIM) capacitance that is available for decoupling and also through the intrinsic switching capacitance available in the die. Also, from eq. 1, we can infer that the interconnect's parasitic inductance is smaller for the integrated power delivery architecture due to reduced length, making its voltage droop smaller [10] [21].

To analyze the impact of integration on the locations of resonances in the impedance profile, let us consider the standing-wave resonances of the PTL shown in Fig. 3. The first resonance in the impedance profile seen by the die is the half wavelength standing-wave resonance of the transmission line at the frequency:

$$f_{res1} = \frac{c_0}{\sqrt{\epsilon_r \mu_r}} \left(\frac{1}{2l}\right) \tag{2}$$

where c_0 is the speed of light in free space; ϵ_r and μ_r are the relative permittivity and permeability of the PTL medium.

For a board-level VRM powering a load at a distance of 11 inches, the PDN has the first antiresonance frequency at 268 MHz. For an on-package IVR, where the source and load are separated by 30mm, the antiresonance frequency occurs at 2.5 GHz.

Thus, fundamentally, with integration, the PDN interconnect offers smaller impedance, less parasitic inductance, and fewer resonance frequencies over a broad spectrum. With less parasitic inductance in the PDN, less decoupling capacitance is required [22] [23] to achieve a low valued and flatter impedance profile. To make use of these benefits, the trend is therefore towards moving the power stages closer to the die. The placement of the power stage output analog filter capacitor, C_{out} in Fig. 1, has evolved from using the traditional on-board capacitor for the VRM to an on-package/interposer [19] capacitor and finally to the on-die MIM capacitor [1].

2) Impact of integration on closed loop performance: A feedback loop is used in the VR, which changes the duty cycle of the clock by sensing the voltage drop at some point in the PDN. Traditionally, the sense point of the voltage regulator is taken from a place along the PDN where the voltage fluctuates at a lower frequency. If the sense point is taken from the die where the voltage fluctuates with respect to chip-package resonance frequency, then instability can occur since the time constant to charge all the decoupling capacitors in the PDN

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can be larger than the voltage fluctuations. This trend of moving the sense point closer to the load is shown in Fig. 4. With integration, however, the low inductance interconnect makes the feedback loop response much faster, and the sense point can be connected closer to the die. The mathematical expression for the overall impedance seen at the sense point looking towards the VR is the closed-loop impedance [24]:

$$Z_{in,CL}(s) = \frac{Z_{in,OL}(s)}{1 + G_{loop}(s)} \tag{3}$$

where $G_{loop}(s)$ is the voltage regulator's control loop gain.

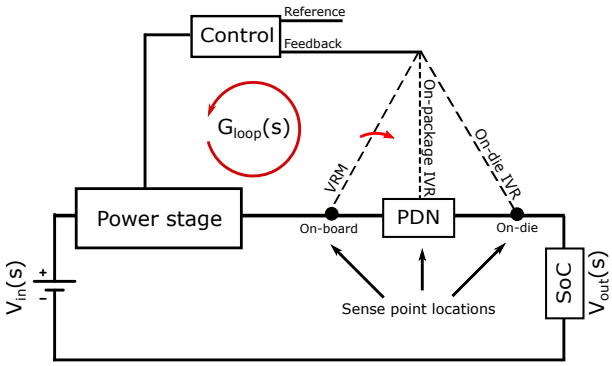

Fig. 4. Sense point locations of power delivery architectures for optimized performance of the feedback circuit, depending on the parasitics of the PDN.

Eqn. 3 shows that within the unity-gain bandwidth of the closed loop, the effective impedance seen is the scaled-down or reduced version of the open loop impedance. Increasing the loop bandwidth helps to mask the resonances of the interconnect and flatten the impedance profile. Consequently, high loop gain bandwidth is preferred in general for ensuring power integrity. The loop bandwidth, however, cannot be increased beyond the switching frequency:

$$\frac{f_c}{f_{sw}} < \alpha N < 1 \tag{4}$$

where f_c is the loop unity-gain bandwidth, α is a constant, and N is the number of phases.

The above relation shows that increasing the number of phases, N, can increase the upper limit αN and thereby, the achievable loop bandwidth. To practically achieve a high loop bandwidth, however, a low parasitic feedback loop is also necessary. Fully Integrated Voltage Regulator (FIVR) [1], for example, is a 16-phase design which has the sense point, VR, and load all on-die, making the feedback loop compact and thereby achieving the $\frac{f_c}{f_{sw}}$ ratio of $\frac{4}{7}$, which is higher than the theoretical, fundamental limit value of $\frac{1}{3}$ for a single-phase design [25].

3) Design and modeling for power integrity: To ensure the integrity of the PDN, designers often use the frequency domain-based approach, where the impedance profile below the minimum threshold target impedance [16] is sought and any excursions of the peak impedance above the target impedance are iteratively compensated by placing decoupling capacitors suitable for that frequency range.

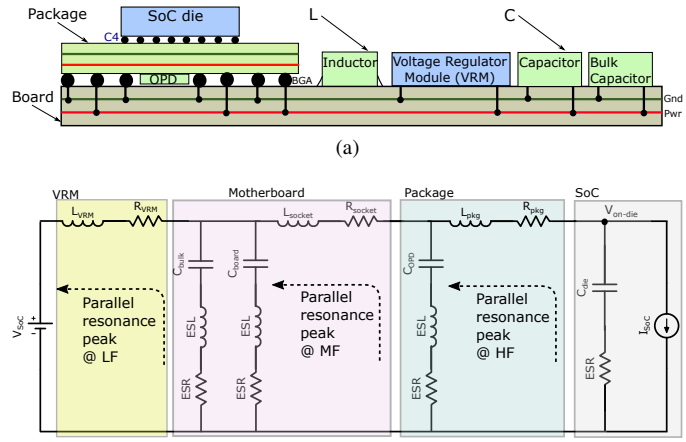

Fig. 5. Typical PDN of discrete VRM: (a) discrete VRM based power delivery architecture and (b) equivalent circuit representation of the PDN, showing the three resonance peaks at low, mid, and high frequencies.

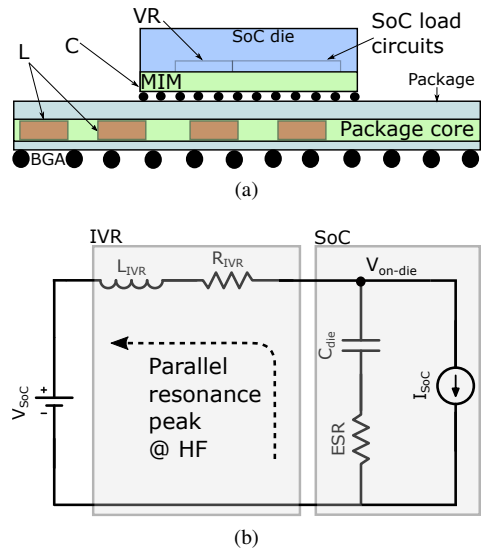

Fig. 6. Typical PDN of an on-die IVR: (a) integrated VR based power delivery architecture and (b) equivalent circuit representation of the PDN, showing the resonance peak at high frequency.

A discrete power delivery architecture and its PDN representation [4] are shown in Figs. 5a and 5b. The L_{VRM} in Fig. 5b is a measure of the time constant of the feedback loop [16] of the VRM. The typical value of L_{VRM} is in the range of nH for discrete architectures. The PDN has three distinct resonances in the frequency domain given by:

$$f_{peak1,VRM} = \frac{1}{2\pi\sqrt{(L_{pkg} + ESL_{OPD})\, C_{die}}} \tag{5}$$

$$f_{peak2,VRM} = \frac{1}{2\pi\sqrt{(L_{socket} + ESL_{board})\, C_{OPD}}} \tag{6}$$

$$f_{peak3,VRM} = \frac{1}{2\pi\sqrt{(L_{VRM} + ESL_{bulk})\, C_{bulk}}} \tag{7}$$

An on-die integrated power delivery architecture and its PDN representation are shown in Figs. 6a and 6b. While the

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discrete VRM architecture has the sense point on the board, the sense point of the IVR is on the die and the low inductance parasitic of the feedback loop allows it to capture any low and mid-frequency resonances in the PDN that fall within the loop bandwidth. Consequently, the PDN has only one resonance in the frequency domain given by:

$$f_{peak1,IVR} = \frac{1}{2\pi\sqrt{L_{IVR}C_{die}}} \tag{8}$$

The single-resonance peak and flat impedance profile of the on-die IVR has the best droop performance [26] for a load step current. On the other hand, a PDN with a multi-resonance peak impedance profile, (eqns. 5, 6, and 7), generates a multi-droop [4] voltage response that is susceptible to the Rogue wave effect [27]. With the on-die IVR, a single peak impedance profile can be achieved and therefore, the second and third droops can be eliminated [7] [28], making the on-die IVR-based power delivery architecture immune to the Rogue wave effect.

Multiple placement options for IVRs exist for an integrated power delivery architecture. An IVR can be placed on-die, on-interposer, and on-package. In determining the right placement for an IVR to ensure timely power delivery, the transient nature of the load current and the resulting voltage droop seen by the die play a critical role. A step current load profile [16] is widely used for the dynamic voltage droop analysis. Given the step current load, the first droop is typically the dominant droop and is associated with the chip package resonance peak in the frequency domain. An example first droop response waveform is shown in Fig. 7.

An analytical expression for the envelope of the PDN's voltage droop response can be obtained. In Fig. 7, the first dip is the worst and happens during the first quarter of the time period of the resonance, T_{res}, and the oscillations dampen out exponentially later. Therefore, the envelope traced by the minimas of the PDN's voltage response is approximated as a linear function during the first droop's fall time which lasts until a quarter of the time period of resonance associated with the on-die capacitance and package parasitic inductance, and the exponential rise happens after the droop with a time constant which also depends on the parasitics, L_p and R_p, given by:

$$V_{1e}(t) \approx \begin{cases} V_0 - \left(\dfrac{V_0 - V_{dr}}{T_1}\right) t & 0 \le t \le T_1 \\ V_s - (V_s - V_{dr})\, exp\left(-\dfrac{t - T_1}{\tau}\right) & T_1 < t \end{cases} \tag{9}$$

where V_0, V_{dr}, and V_s are the values of supply voltage, droop level, and final settled asymptotic voltage respectively; T_1 is the time to reach the first droop, which equals quarter of the time period, T_{res}, corresponding to the chip and package resonance frequency; $T_{res} = 2\pi\sqrt{L_p C_{die}}$; and τ is the relaxation time constant.

The parameters of the above equation, V_{dr}, V_s, and τ, depend on the parasitics and quality factor of the PDN. The droop voltage, V_{dr}, can be estimated for the underdamped case as $V_{dr} \approx I_0\sqrt{\frac{L_p}{C_{die}}}$, where I_0 is the amplitude of the step current. The relaxation time constant is dominated by parasitic inductance, $\tau \approx \frac{2L_p}{R_p}$, for an underdamped PDN [29]; for an overdamped case, the time constant is capacitor dominant, $\tau \approx R_{die}C_{die}$, where R_p, L_p, C_{die}, and R_{die} are the parasitic resistance, inductance, on-die capacitance, and resistance seen by the high-speed switching load. For the case of PDN shown in Fig. 5b, $L_p = L_{pkg} + ESL_{OPD}$ and $R_p = R_{die} + R_{pkg} + ESR_{OPD}$. The settled voltage, V_s is the final settled voltage after the droop. For the case of PDN shown in Fig. 6b, $V_s = V_0 - I_0 R_{IVR}$.

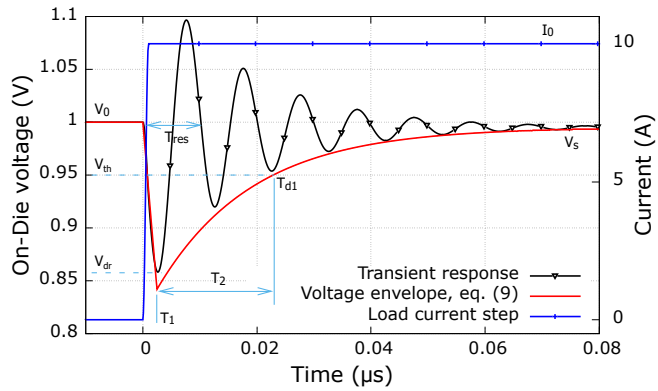

Fig. 7. An example voltage droop transient response and envelope model for 10A step current, showing the first droop duration. Supply voltage V_0 (1V), and the minimum die operating voltage V_{th} (0.95V) are marked. This waveform corresponds to and is obtained for the PDN of Fig. 6 with parameter values of Table IV.

The interconnect parasitics play a critical role in power delivery performance since the first droop cannot be avoided. Even when the IVR is inside the chip, there is always some parasitic inductance associated with the interconnect between the load and MIM capacitance in the chip. Therefore, the time taken by the voltage source to charge the die decoupling capacitance, T_{d1}, may still be larger compared to the switching speed or operating frequency of the chips, T_{clk}, as given by:

$$T_{d1} \approx T_1 + T_2 = \frac{T_{res}}{4} + \tau\, ln\left(\frac{V_s - V_{dr}}{V_s - V_{th}}\right) > T_{clk} \tag{10}$$

where V_{th} is the threshold or the minimum operating voltage tolerated by the die; T_{d1} is the duration of the first voltage droop if the droop is below the voltage threshold, V_{th}; T_{clk} is the clock period corresponding to the switching frequency of the load SoC, f_{clk}. The above equation is applicable for $V_{dr} < V_{th}$ and the saturation voltage, $V_s > V_{th}$. If V_s is smaller than V_{th}, then the duty cycle needs to be increased to get back to a larger voltage close to V_{th}. Under such conditions, the efficiency of the IVR will be poor.

For a CPU with clock frequency f_{clk}, the die is capable of changing current in time duration T_{clk} (for 3 GHz, the clock period is 333 ps). When the current changes, the voltage droops, but if the time to charge the decoupling capacitor from an external power supply is τ_R (=RC of the MIM cap for a fully integrated VR), which is in the range of μs, then the decoupling capacitor will not be charged during the 333 ps

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time duration. This lack of charging time can also be seen in Fig. 7, where the first droop time duration is around 22 ns, which is higher than the 333 ps of the clock period.

The amount of decoupling capacitance available on-die also impacts the IVR placement and design. The effective on-die capacitance seen by the load is typically a combination of MOS capacitance, MIM capacitance, and power grid capacitance. Ideally, the MOS capacitance would match the speed of the switching load, but its density is low [4] and inadequate for the decoupling needs of typical load currents or to be even considered as a bulk capacitor for the VR. This insufficiency of on-die decoupling needs to be considered when designing an IVR and its placement whether it's on die or package or board, so that it will have the best cost-effective solution for any heterogeneous design.

While the compact interconnects arising out of heterogeneous integration benefit the electrical power delivery performance, they come at the cost of increased coupling between the noise sources and victims. The loads for an IVR are distributed spatially on the die, and noise [30] from one load can interfere with another load. Similarly, feedthrough noise [30] can couple from the power stage high-voltage input side, V_{in}, to the output load side. These pose significant design challenges, requiring noise decoupling mechanisms such as the use of LC filters [31]. Also, sense point location [32] plays a critical role for the power delivery performance. For the on-die IVR, the sense point is localized, but the loads are distributed on the die. If the distance from the sense point to a load is far, the voltage droop seen by the load becomes worse [24].

Heterogeneous integrated power delivery architectures essentially transform design complexity from board-level to package and die-levels. In the traditional VRM-based discrete power delivery architecture, the regulator is on board and its regulated low-voltage output is routed from PCB through package to SoC die, needing a judicious choice of decoupling capacitor values, types, and their placements on the board and package [33]. With integrated power delivery architectures, the PCB has an unregulated high voltage feeding the package directly. Since the voltage regulator has a high tolerance for input voltage, the input side decap on the board can be reduced by 10x [34]. Thus, only minimal decoupling capacitors are required on-board for the integrated power delivery architectures and with heterogeneous integration of voltage regulators, the PDN design, traditionally done on-board, moves [35] to on-package and die.

B. Thermal management

Implementation of an IVR involves integration of miscellaneous components onto the same package or die of the SoC. The components of a voltage regulator generally include inductors, capacitors, high-voltage power MOSFET switches, and their drive circuits, as shown in Fig. 1. Among these components, inductors are the least friendly for integration. Their performance deteriorates with scaling [36]. They require more volume, as energy density of an inductor is lower [5] than that of a capacitor. Inductors, therefore, are harder to integrate on-die and are typically embedded on-package.

The dense functional integration of the IVR exacerbates the thermal management challenges. Inductor-based hard-switching power converter topology is widely used for its high load current delivery capability. With large current flow, inductors suffer from Joule heating or I^2R losses. Traditionally, heat is removed from the top side of the die, while the bottom active side of the die faces the flip-chip package. If the inductors are off-die and embedded in the package, they are thermally insulated. Consequently, special attention needs to be given to cool them. Electrical performance of a component is generally adversely impacted by high temperatures. Therefore, the temperatures of the SoC, VR, and inductors become critical figures-of-merit for thermal management as shown in Table I. The temperature depends on the local heat generation rate, thermal coupling, and the heat removal capability of the system, which are discussed in this section. The thermal management needs of an architecture depend on the level of integration. The IVR architectures can be broadly implemented as either 2D or 3D, as shown in Fig. 9c. The load current flow is lateral for 2D, while the flow is vertical for 3D [37]. The on-board and on-die architectures shown in Fig. 8 also belong to the 2D classification. Since air-based cooling is widely used for high-performance computing platforms, a typical power delivery architecture with heat spreaders and heat sinks, as shown in Fig. 10, is considered to assess the thermal management challenges.

1) Impact of VR integration on heat dissipation: Power losses inevitably occur during the power conversion, regulation, and delivery processes, and are dissipated as heat. The power regulation loss in a switching VR includes the losses related to the conduction and switching activity of its components, namely power FET switches and inductors, given by:

$$Q_{VR,loss} = Q_L + Q_{FET} \tag{11}$$

$$Q_L = I_o^2 R_L + Q_M \tag{12}$$

$$Q_{FET} = I_o^2 R_{DS} + C V_{in}^2 f_{sw} \tag{13}$$

where R_L, and R_{DS} are the parasitic resistances of the inductors, and power FETs; I_o is the load current drawn by the load SoC; C is the gate capacitance of the power FET switches; and Q_M is the total losses due to the AC resistance of the conductor, eddy current and hysteresis in the magnetic core of the inductor. The magnetic core losses are proportional to the frequency of operation [36].

The power distribution loss is the conduction loss in the interconnect:

$$Q_{PDN,loss} = I_o^2 R_{PDN} \tag{14}$$

where R_{PDN} is the parasitic resistance of the PDN interconnect.

The overall power efficiency, η, depends on the above losses during power regulation and distribution, $Q_{VR,loss}$ and $Q_{PDN,loss}$, and is given by :

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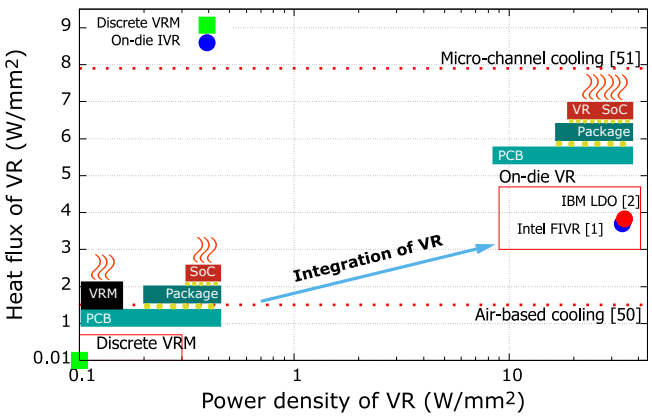

Fig. 8. Thermal challenges with heterogeneous integration, showing the impact of integrating voltage regulator on-die on the thermal solution space.

$$\eta = \frac{Q_{out}}{Q_{in}} = \frac{Q_{SoC}}{Q_{VR,loss} + Q_{PDN,loss} + Q_{SoC}} \tag{15}$$

After power regulation and distribution, a fraction of input power, ηQ_{in}, is finally delivered to the load and is also dissipated as heat in the load. For the case of a VR powering a load, SoC, as shown in Fig. 8, the heat dissipated in SoC, Q_{SoC}, is the same as the power delivered, Q_{out}.

TABLE III
COMPARISON OF THERMAL RELATED PARAMETERS OF DISCRETE AND INTEGRATED VOLTAGE REGULATORS [a]

Parameter	Discrete VRM	Integrated VR
Converter efficiency, η_{VR}	90 to 96%	70 to 90% [38]
Converter power density, q''_{VR}	0.1 W/mm^2	34 W/mm^2 [6]
Converter heat flux, $q''_{VR,loss}$	0.01 W/mm^2	4 W/mm^2 [6]
DC resistance of inductor, R_L	5 to 50 $m\Omega$	15 to 500 $m\Omega$ [38]
Resistance of interconnect, R_{PDN}	1.5 $m\Omega$	0.5 $m\Omega$ [4]

[a]typical values, not specific to a specific system.

Eqs. 12, 13, and 14 above indicate that the heat losses in a power delivery system depend on the parasitic resistances and frequency of operation. With integration, interconnects become compact, resulting in lower parasitic resistance, R_{PDN} and reducing the conduction or I^2R losses in the interconnect, $Q_{PDN,loss}$. Component heat losses in the VR, on the other hand, increase with integration, as the integration calls for compact components and high switching frequency, f_{sw}. The compact components are made with small cross-sectional area conductors. Consequently, their parasitic resistance, R_L, increases, as shown in Table III. The package embedded inductors, for example, typically have an order of magnitude higher resistance than the discrete inductors. Also, their electrical resistance increases with temperature due to Joule heating, given by:

$$R(T) = R_0(1 + \alpha(T - T_0)) \tag{16}$$

where $R(T)$ is the resistance at temperature, T; R_0 is the resistance at some initial temperature, T_0; and α is the temperature coefficient.

The temperature of a VR component impacts not only efficiency but also the reliability of the VR. Components self-heat due to their power losses, increasing their temperature. At a high temperature, its electrical resistance increases due to the Joule heating given by eq. 16. Higher resistance causes increase in the conduction loss component of the total heat loss. The electrothermal coupling and positive feedback makes the component run hotter and reach a much higher temperature. If the heat is not properly managed, thermal runaway can occur. Also, at such a high temperature, instability or change of mode of operation can take place for the inductor-based switching voltage regulators. Inductors made from magnetic materials such as Ferrite lose their magnetic properties beyond the Curie temperature. This drop in inductance at a high temperature can disrupt the normal continuous conduction mode (CCM) operation of the VR to the discontinuous mode.

Therefore, appropriate thermal solutions are necessary for a power delivery system to manage its losses and Joule heating effects. In identifying the kind of thermal solution needed, the metric of heat dissipation or flux density can be used, which is the heat generation rate per surface area of the heat source. The heat flux density of VR, $q''_{VR,loss}$, depends on its efficiency, η_{VR}, and its power density or power output per surface area of VR, q''_{VR}, written as:

$$q''_{VR,loss} = q''_{VR}\left(\frac{1}{\eta_{VR}} - 1\right) \tag{17}$$

With integration, as the components of VR become compact and distance between them reduces, the power and heat flux densities of the regulator increases. This trend of increasing heat flux density with integration, shown in Fig. 8 and Table III, poses challenges in using the traditional thermal solutions. The cooling capabilities for the traditional air-based solutions and advanced micro-channel solutions of 1.5 W/mm^2 [39] and 7.9 W/mm^2 [40] respectively have been demonstrated in the literature. The on-board discrete VRM typically occupies large areas on the board in the range of few hundreds of mm^2 with a lower power density around 0.1 W/mm^2, and a lower heat flux of 0.01 W/mm^2 [41], which can be cooled using an air-based forced convection. But, for on-die IVRs, most of the voltage regulator components such as power MOSFETs and their drive circuits are on die, and their footprint is small. Consequently, the power density of the integrated voltage regulator is much higher in the range of tens of W/mm^2. FIVR [1], an on-die buck regulator, for example, has a current delivery density of 31 A/mm^2 at an output voltage of 1.05V, resulting in 32 W/mm^2 [1] power density at an efficiency of 90%, which leads to 4 W/mm^2 heat dissipation density for the VR. Similarly, an on-die VR based on a linear low-dropout (LDO) topology [2] has 34 W/mm^2 power density and efficiency of 90%, resulting in 4 W/mm^2 heat flux. This is higher than the 1.5 W/mm^2 [39] cooling capability offered by typical air-cooled computing systems. Therefore, when the VR is integrated on die, its heat dissipation density creates local hot spots [42] on the SoC die when cooled using air.

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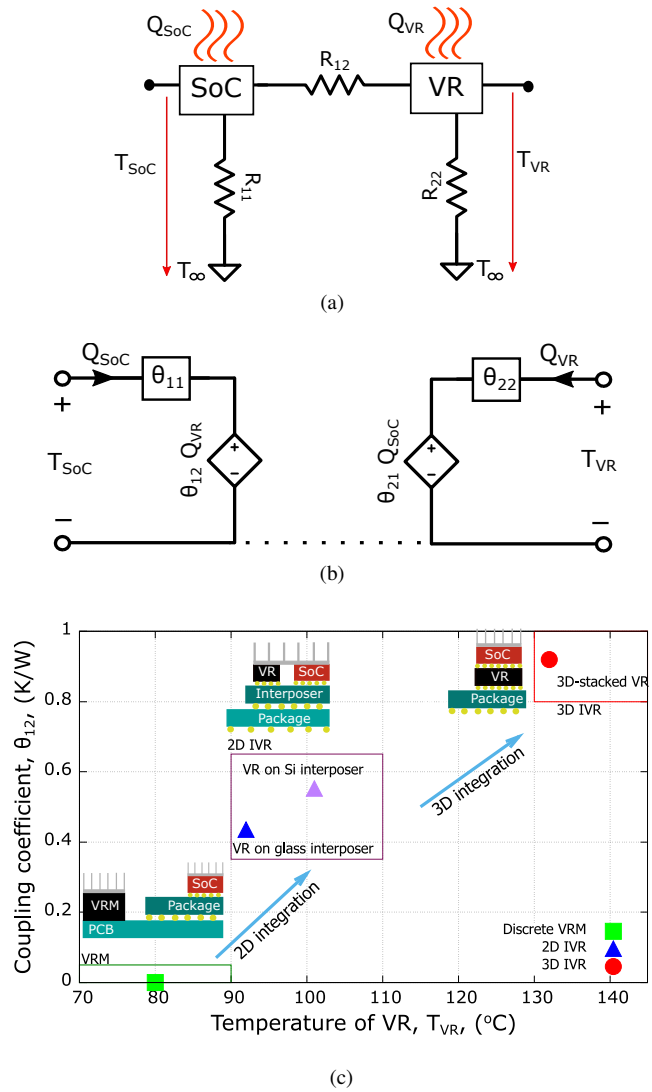

Fig. 9. Trend of thermal coupling in power delivery architectures: (a) thermal view of power delivery architecture, showing an equivalent thermal network, (b) two-port representation, and (c) impact of integration and package substrate on the thermal coupling, showing discrete, 2D and 3D power delivery architectures. In order to obtain the results above, a typical air-cooled configuration of SoC and VR, having power losses 100W and 10W respectively and separated by 0.5mm distance, was considered.

2) Impact of VR integration on thermal coupling: With integration, the distance between the power source and load reduces, as shown in Fig. 9c. As they come closer, thermal coupling between the power source and load naturally increases. To understand the variables that impact the thermal coupling effects between the SoC and VR, we can represent the SoC and VR in a power delivery system as a π network, as in Fig. 9a.

Let us generalize by considering the power delivery system as a two-port thermal resistance network [43], as shown in Fig. 9b, where their temperatures can be written as:

$$\begin{bmatrix} T_{SoC} \\ T_{VR} \end{bmatrix} = \begin{bmatrix} \theta_{11} & \theta_{12} \\ \theta_{21} & \theta_{22} \end{bmatrix} \begin{bmatrix} Q_{SoC} \\ Q_{VR,loss} \end{bmatrix} \tag{18}$$

where θ_{11} and θ_{22} are the self-thermal resistances of the SoC and VR respectively, capturing their self-heating effects, while θ_{12} or θ_{21} is the coupling or transfer thermal resistance related to mutual-heating effects between the VR and SoC.

For the π network representation, the transfer resistance, θ_{12}, can be derived as:

$$\theta_{12} = \frac{R_{11}R_{22}}{R_{11} + R_{12} + R_{22}} = \frac{R_{11}R_{22}}{R_{11} + \frac{l}{kA} + R_{22}} \tag{19}$$

In eqn. 19, assuming the VR and SoC are separated by a distance, l, with thermal conductivity, k, and cross-sectional area, A, the thermal resistance, R_{12}, equals $\frac{l}{kA}$.

Equation (19) shows that as the system becomes denser and more compact with heterogeneous integration, the reduction of distance, l, between the components increases the thermal coupling effect by increasing the transfer resistance, θ_{12}, thereby exacerbating the thermal management challenges. The trend towards increased thermal coupling with increased integration can be observed in Fig. 9c. A higher coupling coefficient also translates to a higher temperature of VR which can also be seen in Fig. 9c. In addition, since thermal coupling is proportional to the thermal conductivity of the medium, k, Si interposer-based integrated architectures increase thermal coupling between high heat flux devices such as SoC and heat-sensitive components such as IVR, thus needing advanced thermal isolation solutions such as the use of thermal metamaterials [44] or an air cavity [45], while low thermal conductivity package substrate materials like glass provide natural thermal isolation. The impact of a lower thermal coupling coefficient in a glass interposer and $10°C$ higher VR temperatures for Si-interposer can be observed in Fig. 9c.

3) Design for thermal management of embedded inductors: The temperature of the inductor is another critical figure-of-merit for the thermal management of voltage regulators, as the inductors carry current and can suffer from Joule heating losses. Joule heating in inductors and the corresponding reduction in power efficiency is a concern. Integrated voltage regulators use embedded inductors either on-die or package. For high-current carrying applications, the package-integrated inductors are more suitable [4], as they generally have thicker conductors and a higher magnetic core volume than the on-die inductors. From a thermal perspective, if the inductors are embedded in the package, they are thermally insulated from other heat sources and may need a local cooling solution. The on-die inductors, on the other hand, are thermally coupled to the die-level heat sources and therefore need judicious placement away from the heat sources. Therefore, embedded inductors always need special cooling solutions.

Traditional thermal solutions for electronic packages mainly rely on heat removal from the top. If we consider such a top-sided heat sink-based multi-phase IVR with multiple inductors embedded in the package substrate core, the inductor's thermal path to the ambient can be represented as a resistor network, assuming a one-dimensional heat flow, with a rejection path being dominant through the top, and a minimal thermal coupling between SoC and VR, as shown in Fig. 10. Note that a package-on-package (POP) type architecture is considered in Fig. 10. Other packaging architectures such as multi-chip-modules (MCM) where the inductors can be embedded in the

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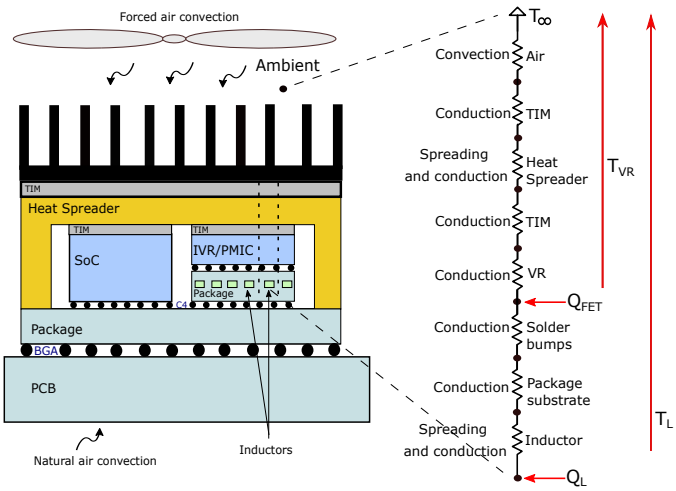

Fig. 10. Typical multi-phase integrated voltage regulator architecture with package-embedded inductors and its thermal view: unit thermal cell and the network representation of thermal resistance seen by an embedded inductor.

package of the SoC are feasible, but may not be viable from an electrical point-of-view as multiple electrical interconnect vias are required through the magnetic core of the inductor.

To assess the limits of a top-sided thermal solution such as a heat sink in keeping the embedded inductors cool, let us consider the case of a perfect heat sink at the top. In Fig. 10, SoC and VR are directly cooled from the top and their temperatures depend on the heat sink's heat removal capability. However, the temperature dependence is not linear. As we increase the performance of a top-sided heat removal solution, temperatures of SoC and VR reach asymptotically [46] to their respective minimum saturated temperatures. Therefore, for high-performance heat removal from the top, the lower limit for the inductor's temperature can be written as:

$$T_{L,min} = R_{in} Q_L + T_{VR,sat} \tag{20}$$

$$R_{in} = R_L + R_{pkg} + R_{bump} = R_L + R_{pkg} + R_{\theta JB} \tag{21}$$

where R_{in} is the overall thermal resistance seen by the inductors to the closest heat source (VR); R_L, R_{pkg}, R_{TIM}, and R_{bump} are the thermal resistances corresponding to the inductor, package substrate, thermal interface material (TIM), and solder bump layers, respectively; $R_{\theta JB}$ is the junction to the board thermal resistance parameter of the IVR/PMIC IC; and $T_{VR,sat}$ is the limiting or minimum possible temperatures of the IVR.

The above analysis shows that there exists a lower bound for the temperature of embedded inductors, independent of the heat removal capability of the conventional top-sided cooling solutions. The sufficiency of a top-side cooling solution for embedded inductors depends on the rate of heat dissipation in the inductors Q_L, the maximum operating temperature of inductors, $T_{L,th}$, which is $85°C$ [47] in Table I for example, and the resistance of the thermal path between inductors and VR, R_{in}. For a given thermal setup and cooling solution, there exists an upper bound on heat dissipation rate, Q_L, such that the inductor's temperature stays below the threshold limit given by:

$$Q_{L,max} = \frac{T_{L,th} - T_{VR,sat}}{R_{in}} \tag{22}$$

For low-heat dissipating inductors [1] [48] with power losses below $Q_{L,max}$, the inductor's temperature is below the threshold, $T_{L,th}$, and the conventional top-sided cooling solution is sufficient. For high voltage conversion VRs with high-heat dissipating embedded inductors with power losses above $Q_{L,max}$, the minimum temperature can be above the threshold and therefore a conventional top-sided cooling solution becomes insufficient, thereby requiring a local cooling solution.

C. Electromagnetic Interference

The switching pulse-width modulated (PWM) voltage regulators are often employed for their power efficiency. However, the inherent switching nature of the power FETs draws discontinuous currents from the high-voltage input side, causing EMI problems. The effect of IVR's high switching frequency on EMI and the resulting filter design are covered in this section.

1) Impact of integration on the EMI levels: Step-down voltage regulators convert energy from a high voltage form at its input to that of a low voltage at its output. A switching voltage regulator that typically powers a high-performance CPU or SoC, draws pulsed currents from its input side [49] as shown in Fig. 11a. If we consider a generic trapezoidal pulse, as shown in Fig. 11b, its Fourier analysis results in a frequency spectrum [50] enveloped at two corner frequencies, as shown by dashed lines in Fig. 11c. The fundamental, 20dB/decade, and 40dB/decade roll-off corner frequencies are given by:

$$f_o = f_{sw} \tag{23}$$

$$f_{c,1} = \frac{1}{\pi\ \tau_{on}} = \frac{f_{sw}}{\pi\ \alpha_{on}} \tag{24}$$

$$f_{c,2} = \frac{1}{\pi\ \tau_r} = \frac{f_{sw}}{\pi\ \beta_r} \tag{25}$$

where τ_{on} is pulse duration and τ_r is its rise time; α_{on} is the duty cycle or the voltage conversion ratio, $\alpha_{on} = \frac{\tau_{on}}{T_{sw}} = \frac{V_{SoC}}{V_{in}}$; β_r is rise time in unit intervals of time period, $\beta_r = \frac{\tau_r}{T_{sw}}$; and f_{sw} is the switching frequency of the voltage regulator.

The amplitude of the conducted and radiated electromagnetic interference (EMI) from a switching voltage regulator depends on the frequency spectrum of its switching signals. The spectrum is characterized by the corner frequency, $f_{c,2}$, which depends on the switching frequency and the rise time of the signals, as given by eq. 25. Since integrated voltage regulators typically operate at a higher switching frequency and have a faster rise time than a VRM, the corner frequency increases, thereby shifting the spectrum of the VRM to higher frequencies for the IVR. This shifting of the spectrum causes the EMI emissions to be generally higher [51] [10] for IVR than VRM.

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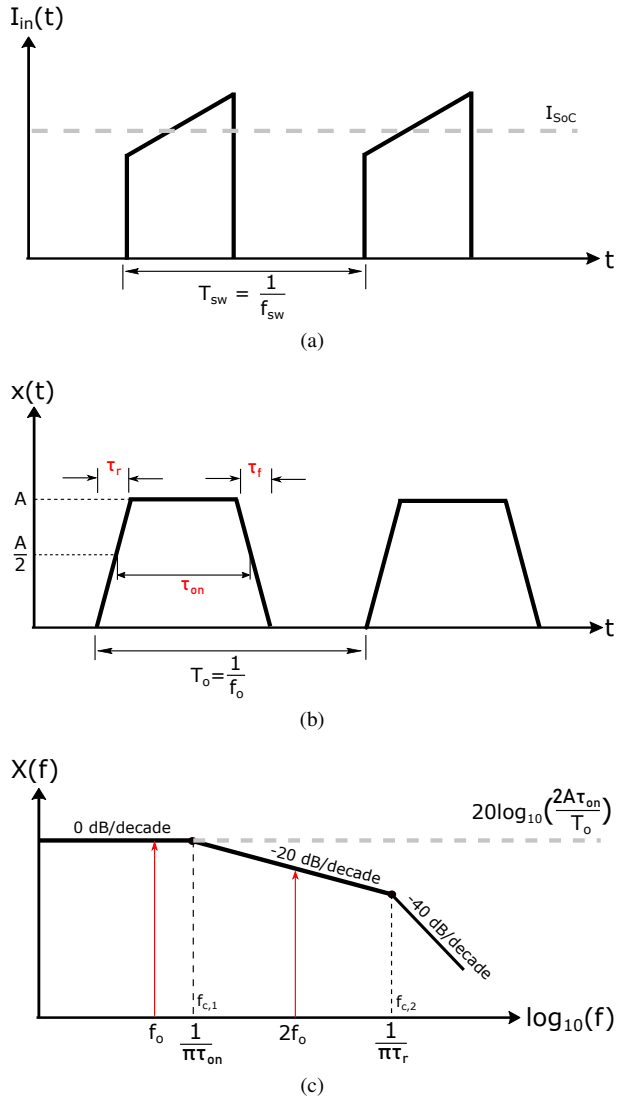

Fig. 11. Pulses at the input side of a switching voltage regulator: (a) the current profile in the switch of the buck converter, (b) a periodic trapezoidal waveform, and (c) the envelope of the frequency spectrum of the trapezoid waveform for the special case when rise and fall times are the same.

2) Design for EMI filtering: EMI filters are often used to mitigate the conducted EMI at the input side of the power stage. An example EMI filter topology [52] and its package implementation are shown in Figs. 12a and 12b. The values of the components, L_f, C_f, and C_d depend on the input current and the filter cutoff frequency, given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{26}$$

The cutoff is usually at one-tenth of the regulator's switching frequency, f_{sw}. The high switching frequency of the IVR makes the filter component sizes smaller. For high conversion ratio voltage regulators, the input current drawn is smaller, thereby needing smaller L_f.

III. Results

Multiple test cases of IVR and VRM architectures are considered here to verify the multi-domain analysis of section

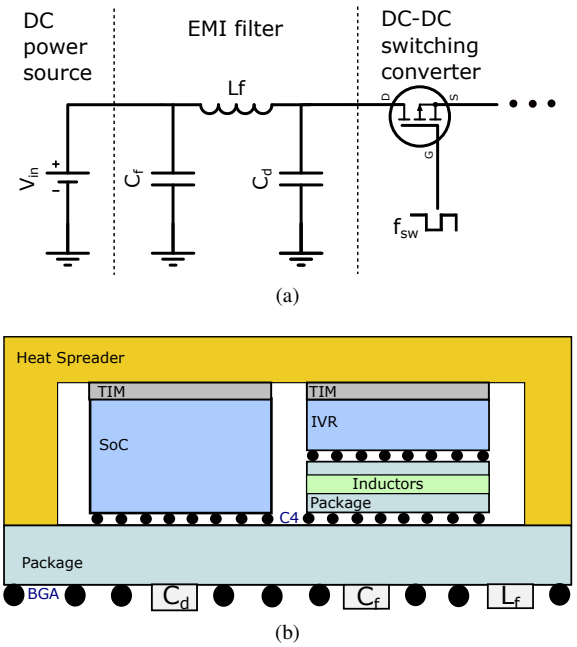

Fig. 12. Typical EMI filter for mitigating the conducted EMI of a VR: (a) EMI filter topology and (b) integrated EMI filter on the landside of the package.

II. For electrical power delivery, voltage droops in PDNs of typical microprocessors are compared. The excitation load step current, I_{die}, is assumed to be a 0A to 10A step in 1 ns and the supply voltage, V_{SoC} is set at $1V$. The values in Table IV correspond to the PDN circuitry in Figs. 5 and 6. The voltage droop results are shown in Fig. 13. For thermal analysis, thermal solutions for a package-on-package (POP) IVR architecture with forty embedded inductors as shown in Fig. 15 are considered. The heat generation rates were assumed to be 100W, 10W, and 10W for the SoC, IVR, and inductors respectively. The ambient temperature for the thermal analysis is 40°C. Effective heat convection coefficients are applied to emulate the performance of heat removal devices, as shown in Table VII. A high-performance cold plate was considered and correspondingly a high convection coefficient value of $10,000$ W/m^2K was used. The vapor chamber is modeled using an anisotropic thermal conductivity as shown in Table V. For the μCooler, an equivalent thermal resistance model for package embedded micro-channels [53] was used to arrive at the convection coefficient. The solder ball interconnection layer of the IVR was modeled after a typical chip-scale packaged power MOSFET integrated circuit [54]. The bottom surface was considered exposed to air and a convection coefficient of 20 W/m^2K, obtained from the Nusselt number correlation for a flat horizontal surface, was applied. The thermal analysis included Joule heating and was computed using ANSYS IcePak. The thermal results are shown in Fig. 16 and Table VIII. The design goal for thermal management is that the inductor's temperature be less than 85°C, which is the operating limit of most magnetic cores [47] used for fabricating the inductors. The results of the thermal analysis under typical and limiting conditions are shown in Figs. 16 and 17. For EMI analysis [55], two 1.8V-to-1V regulator buck circuits switching at 10 MHz for IVR and 250 KHz for VRM are used. The EMI

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attenuation filters are designed for these regulators such that they meet the conducted emission limit of the CISPR 11 standard. The filter design and attenuation performance are tabulated in Table VI and the results are shown in Fig. 14.

TABLE IV
PDNs COMPARED[a]

Test case	Component values
VRM	$L_{VRM} = 1nH$ $R_{VRM} = 1m\Omega$ $ESL_{bulk} = 1nH$ $ESR_{bulk} = 2m\Omega$ $C_{bulk} = 1500\mu F$ $ESL_{mb} = 300pH$ $ESR_{mb} = 0.5m\Omega$ $C_{mb} = 100\mu F$ $R_{skt} = 0.2m\Omega$ $L_{skt} = 50pH$ $ESL_{OPD} = 30pH$ $ESR_{OPD} = 1m\Omega$ $C_{OPD} = 20\mu F$ $L_{pkg} = 10pH$ $R_{pkg} = 0.2m\Omega$ $ESR_{die} = 2.5m\Omega$ $C_{die} = 100nF$
IVR	$L_{IVR} = 25pH$ $R_{IVR} = 0.5m\Omega$ $ESR_{die} = 2.5m\Omega$ $C_{die} = 100nF$

[a]Typical values corresponding to the configurations in Figs. 5 and 6

TABLE V
THERMAL MATERIAL PROPERTIES [a]

Component	Description	$k_{\parallel}/k_{\perp}$ (W/m-K)	Dimensions: L/W/H (mm)
Heat spreader	Cu-SiC composite	306	30, 30, 2
Heat spreader	Vapor chamber	417, 1669	30, 30, 2
TIM	Thermal Grease	5	10, 10, 0.15
SoC	Silicon	148	10, 10, 0.75
IVR/PMIC	Silicon	148	10, 10, 0.5
Package	Substrate with thermal vias	2, 20	30, 30, 2
Inductor	Magnetic core	2, 20	1, 1, 0.1
C4 layer	100 μm diameter and 200 μm pitch	10	10, 10, 0.1
Solder bumps layer	SAC305 250μm solder balls	1	10, 10, 0.15

[a] $k_{\parallel}$ and $k_{\perp}$ are in-plane and out-of-plane thermal conductivity values.

TABLE VI
EMI FILTER COMPARISON [a]

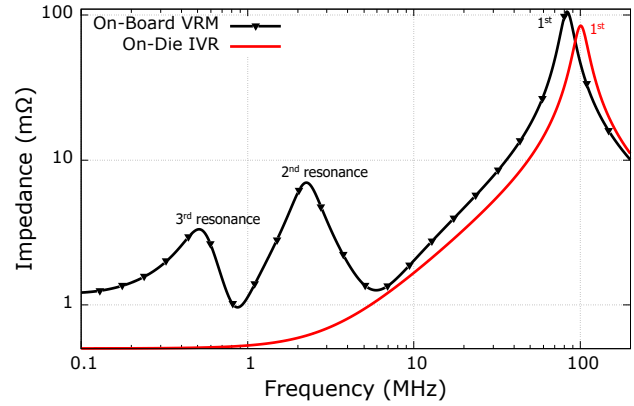
Test case	Required attenuation	Design of the filter: $L_f/C_f/C_d$
VRM with f_{sw} of 250 KHz	90 dB	100 μH, 133 μF, 133 μF
IVR with f_{sw} of 10 MHz	115 dB	10 μH, 4.5 μF, 4.5 μF

[a]Designed to meet the CISPR 11 conducted EMI emission limit.

TABLE VII
THERMAL SOLUTIONS COMPARED AND THEIR EFFECTIVE CONVECTION COEFFICIENTS[a]

Thermal solution	Top	Bottom	Local
Forced air-cooled Cu-SiC heat spreader (Fig. 15a)	2500	20	NA
Forced air-cooled vapor chamber (Fig. 15a)	2500	20	NA
Forced water-cooled cold-plate on the vapor chamber (Fig. 15a)	10000	20	NA
μCooler and forced air-cooled Cu-SiC heat spreader (Fig. 15b)	2500	20	6000

[a]The convection coefficient values are in W/m^2K.



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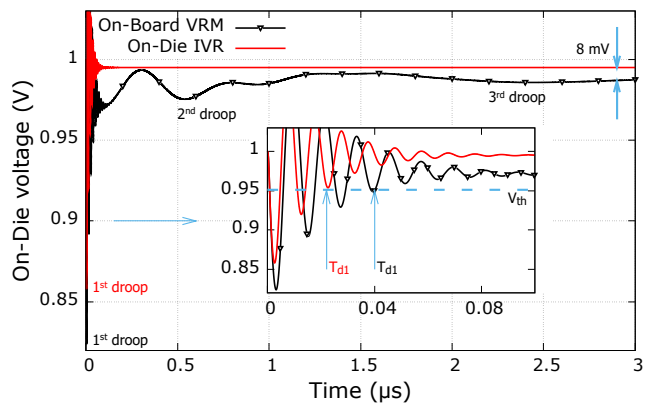

(b)

Fig. 13. Impact of integration on the electrical power delivery domain: (a) frequency domain comparison between the on-board and on-die regulators and (b) time-domain comparison between the on-board and on-die regulators for a 10A step current load.

TABLE VIII
DESIGN SPACE EXPLORATION OF THE IVR'S THERMAL SOLUTIONS BASED ON THE TEMPERATURE OF THE EMBEDDED INDUCTORS[a]

Thermal solution	Temperature map	$T_{inductor}$
Forced air-cooled Cu-SiC heat spreader (Fig. 15a)	Fig. 16a	135°C
Forced air-cooled vapor chamber (Fig. 15a)	Fig. 16b	130°C
Water-cooled cold-plate on the vapor chamber (Fig. 15a)	Fig. 16c	90°C
μCooler and forced air-cooled Cu-SiC heat spreader (Fig. 15b)	Fig. 16d	85°C

[a]The ambient temperature is 40°C.

IV. DISCUSSION

The results of section III confirm the trends which were analyzed in section II. For electrical power delivery, the two extreme ends of the integration are compared, on-board VRM and on-die IVR. The sense point for the VRM is on the board while it is ondie for IVR, reducing the IVR inductance, L_{IVR}, to the pico-henry range, as shown in Table IV. The frequency domain characterization result in Fig. 13a shows that multi-peak resonances become a single-peak resonance with integration. The time-domain comparison shows a similar trend in Fig. 13b: multiple droops become a single droop

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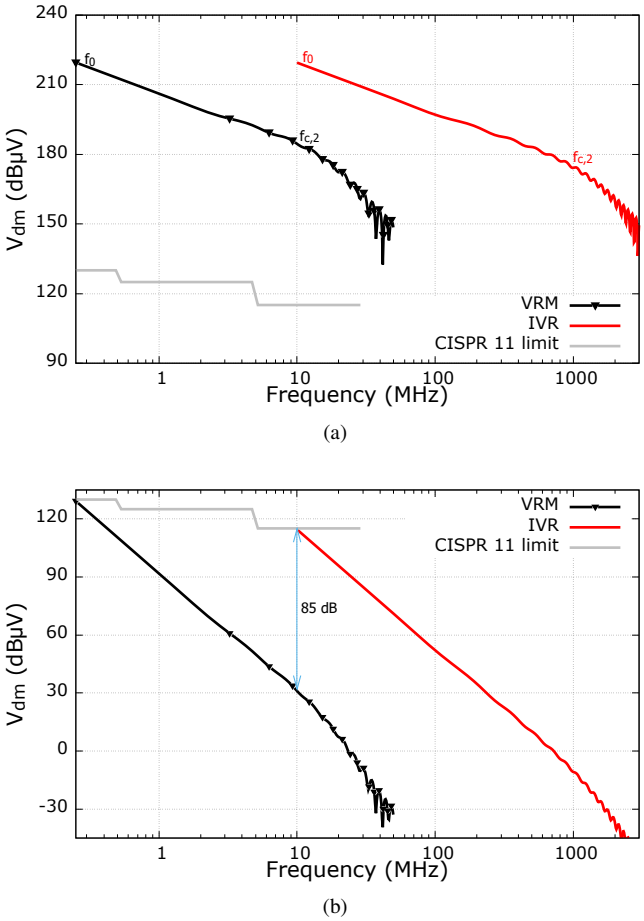

Fig. 14. Impact of integration on the electromagnetics domain: (a) conducted EMI comparison between the discrete and integrated regulators without an EMI filter and (b) conducted EMI comparison between the discrete and integrated regulators with an EMI filter.

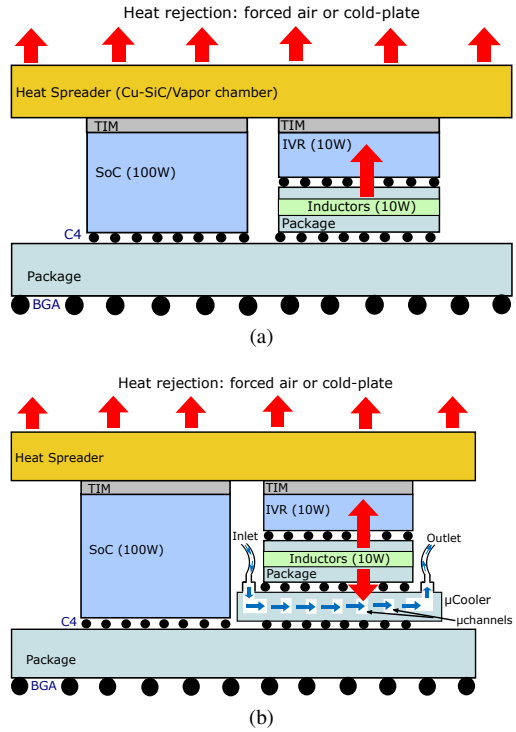

Fig. 15. Thermal solutions for the IVR architecture: (a) typical top-level thermal solution having a Cu-SiC or vapor chamber heat spreader and the top-sided heat removal by either forced air or water-cooled cold plate and (b) μCooler as a local cooling solution along with the traditional top-level heat removal, allowing bi-directional heat rejection from inductors. Note: red arrows indicate primary heat flow paths and small blue arrows represent the fluid flow in μCooler. Heat dissipation rates in each of the components are also shown.

with integration where the VRM has three droops, while the IVR has only one. The IVR performs better than VRM due to its shorter PDN interconnect length. IVR's 1st voltage droop, V_{dr}, is smaller than that of VRM by 35 mV and the IR drop is 8 mV lower, as shown in Fig. 13b, which can impact the clock frequency by around 18 MHz assuming a rate of 2.275 MHz/mV [56] based on the product lines of the microprocessor across several generations. The 8 mV DC offset can be corrected using the feedback loop of the discrete regulator by increasing its duty cycle, but its power efficiency will suffer. Also, the first droop duration, T_{d1}, given in eq. 10 can also be observed in Fig. 13b. For the VRM, the droop duration is around 40 ns, while the droop duration is 22 ns for the IVR architecture. Thus, with the lower droop level, droop duration, and IR drop, IVR in general improves both the DC and AC noise of the PDN and performs better for timely power delivery to the load.

For the EMI domain, the conducted EMI levels are higher and worse for the IVR than the VRM, as shown in Fig. 14. The shift of the EMI envelope due to the high switching frequency of the IVR can be seen in Fig. 14a. Also, both the IVR and VRM configurations have higher EMI levels than the conducted emission limit specified by the CISPR 11 Class A standard [57], needing EMI attenuation filters. The filter design requirements for IVR are more stringent than VRM. From Table. VI, for example, the required filter attenuation needed for the IVR is 115 dB, which is 25 dB higher than VRM, but the IVR EMI filter's component sizes are smaller due to its high switching frequency. The filter's inductance, L_f, and capacitance, C_f, have reduced from 100 μH to 10 μH and 133 μF to 4.5 μF. With the filters, both meet the compliance, but the IVR's conducted EMI levels still exceed the VRM by 85dB, as highlighted in Fig. 14b. Therefore, the IVR needs even more EMI filtering to match the VRM's EMI levels. This filtering requires judicious placement with low parasitics and additional real estate space on the package, which can pose a challenge for heterogeneous architectures.

From the thermal perspective, the first three cases in Table VIII have inductors above the 85^oC temperature threshold level in Table I. The heat map results of these solutions in Figs. 16a, 16b, and 16c show that the embedded inductors become hot spots. The air-based thermal management with the Cu-SiC heat spreader is insufficient, as the inductors reach 132°C. Using a better heat spreader solution such as a vapor chamber, although helpful for the SoC, as shown in the thermal map of Fig. 16b, doesn't help in reducing the inductor's temperature. Replacing forced-air removal with a water-cooled cold plate on the vapor chamber reduces the temperature of the embedded inductors to 90°C, which is still above the 85^oC threshold. This is due to the saturation of the VR's temperature at 65°C and

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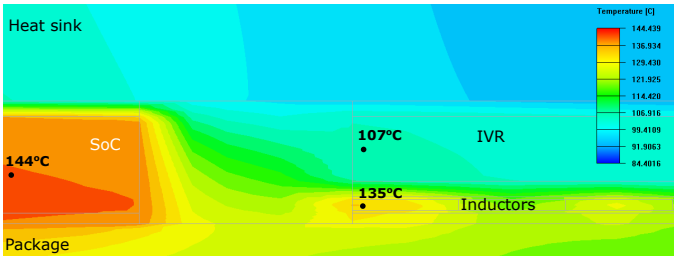
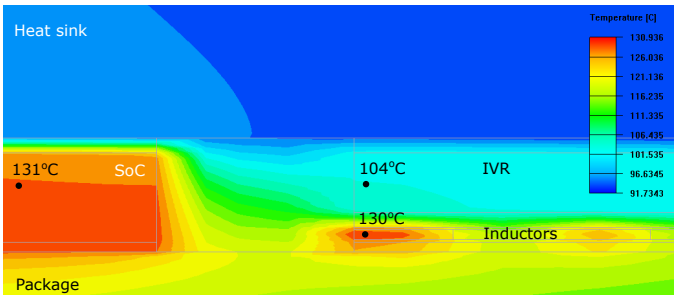
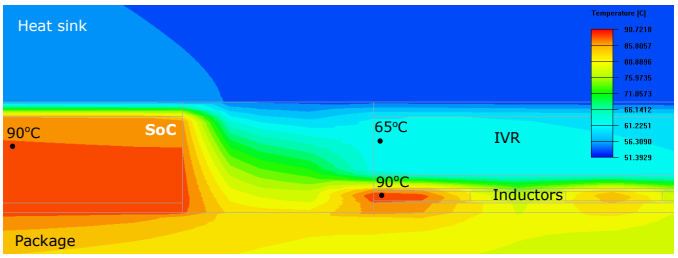


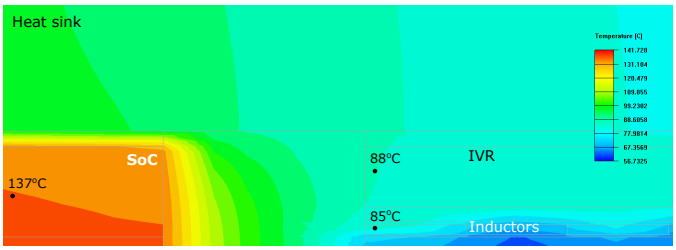
(a)



(b)

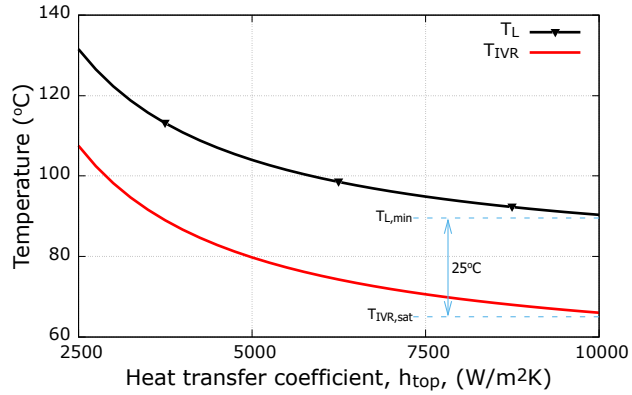


(c)

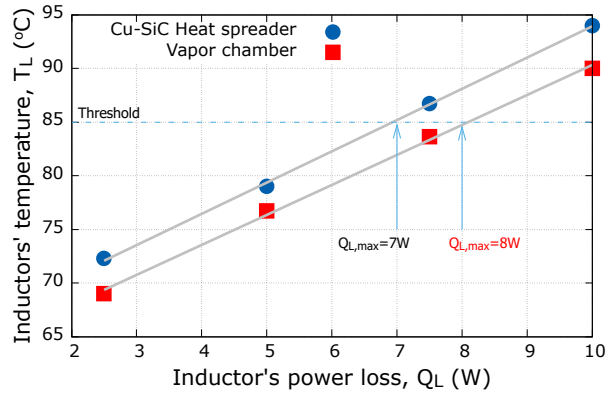


(d)

Fig. 16. Thermal analysis of the solutions for the IVR under typical conditions of Table VII: (a) forced air-cooled Cu-Sic heat spreader, (b) forced air-cooled vapor chamber heat spreader, (c) forced water-cooled cold plate on vapor chamber, and (d) μCooler as a local cooling solution along with the air-cooled Cu-Sic heat spreader as the global cooling solution.



(a)



(b)

Fig. 17. Thermal analysis of the solutions for the IVR under limiting conditions: (a) thermal performance of vapor chamber heat spreader with varying heat convection rates at the top, showing the saturation or bottoming out of the temperatures of VR and inductors and (b) comparison of thermal performance of Cu-SiC and vapor chamber heat spreaders given high-performance cooling from the top, showing maximum power losses allowed for inductors under respective heat spreaders in order to keep the inductor's temperature under the threshold of 85°C.

the 2.5 K/W of thermal resistance existing between the $10W$ heat-dissipating inductors and VR, resulting in an additional 25°C temperature difference for the inductors. Therefore, the combination of 65°C and 25°C, in eq. 20, results in the minimum temperature bound for the inductors to be 90°C, which is highlighted as $T_{L,min}$ in Fig. 17a. To lower the minimum temperature bound further, the 25°C additional temperature difference needs to be reduced. To reduce the 25°C additional temperature difference or gap, either the thermal path between the VR and inductors needs to have a lower thermal resistance or the heat losses in the inductors need to be lower. The power management IC (PMIC) or power FET ICs, however, typically tend to have a high junction to board, $R_{\theta JB}$, thermal resistance values in the range of 2.5 K/W to 1.0 K/W [54] [58]. To reduce the $R_{\theta JB}$ values for the PMICs or IVRs, their solder interconnections need to be thermally improved by increasing the interconnect density and solder bump diameter [46]. Alternatively, with the addition of a local cooling solution, using a μCooler, the inductor's temperature comes down to 85°C, satisfying the threshold. To eliminate the μCooler solution, the power loss in the inductors has to be reduced below 7 W or less, as shown in Fig. 17b, increasing challenges for the inductor design. In addition, thermal coupling has a direct impact on electrical and electromagnetic domains. For example, the electrical integrity of high-speed communication links is temperature dependent. As temperature increases, the total jitter of the transmitting device and the loss tangent of the dielectric material increase [59], causing the signaling performance of high-speed serial links to degrade. Thermal coupling to electromagnetic domain, on the other hand, arises from electromagnetic radiation in large heatsinks. The large metal heatsink structures have parasitic mutual capacitance

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with other nearby conductors such as a metal case. Through the mutual capacitance, displacement currents can couple and cause radiated EMI. Therefore, proper electrical grounding [60] of the heatsink is necessary to mitigate EMI.

Finally, the coupling between multi-physics domains generally becomes stronger in heterogeneous integration architectures. Therefore, for an efficient realization of integrated voltage regulators, multi-physics optimization [61] [12] is necessary. In finding the right balance among the multi-physics metrics, numerical models such as the finite element method are often used. However, the traditional numerical methods use time-stepping procedures and face time-scale challenges in the coupled multi-physics analysis. For example, the typical time constant of computational problems in the electrical domain is in the nanoseconds range, while it is in seconds for the thermal domain [11]. Harmonics-based frequency-domain numerical methods [62] [8] are time-scale agnostic and can alleviate the computational complexity associated with the multi-physics modeling and analysis. Multi-physics modeling is an active area of research and recent developments in computer architecture such as parallel multiple-cores on graphics cards [63] can be exploited in solving the modeling challenges efficiently.

V. Conclusion

Heterogeneous integration is a possible pathway to continue Moore's law performance of electronic systems. In power delivery, the heterogeneously integrated voltage regulator is a promising candidate. In this paper, we assessed the design complexities resulting from integrating the voltage regulator and the resulting solutions space in three domains - electrical, thermal, and electromagnetics. Test cases in these domains show that IVR benefits electrical power delivery performance while deteriorating noise coupling, thermal, and EMI. To manage such complexities, co-design and optimization at the chip/package/system level are necessary. The main findings of this work can be summarized as follows:

1) In the electrical domain, a new metric as a measure of timely power delivery, the first droop duration, T_{d1}, was defined and its closed form expression was given. It is indicative of the time duration which an under par voltage, below the voltage threshold, is seen by the load during a step of current. The case study showed that integration improves this metric by nearly 50%. (40ns for VRM vs. 22ns for IVR)
2) The amount of EMI filtering required increases with integration and advanced packaging of the filter components with low parasitic inductance is needed. The case study showed that the filter attenuation requirement increases by nearly 30%. (90dB attenuation required for VRM vs. 115dB for IVR)
3) In the thermal domain, there exists a threshold for heat dissipation in the embedded devices, above which they cannot be managed by traditional top-level thermal solutions and therefore need an additional local cooling solution. For an integrated power delivery architecture test case with the Cu-SiC heat spreader delivering 100W to the load, this thermal design decision threshold for power losses in the embedded inductors was found to be 7W. Also, the μCooler solution with package-integrated micro-channels was found to be an effective local cooling solution for high-heat dissipating embedded passives.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCPMT.2021.3124248, IEEE Transactions on Components, Packaging and Manufacturing Technology

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